

# 9-Bit latched bidirectional Futurebus transceivers (open-collector)

74F8962/8963

## FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to  $10\Omega$
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 futurebus standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity

- Multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation

## DESCRIPTION

The 74F8962 and 74F8963 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 150mV threshold region.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower

power consumption and a series diode on the drivers to reduce capacitive loading.

Incident wave switching to  $9\Omega$  is guaranteed. The voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F8962 and 74F8963 A ports have TTL 3-state drivers and TTL receivers with a latch function.

The 74F8963 is the non-inverting version of 74F8962.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8962	6.5ns	90mA
74F8963	5.5ns	90mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
44-pin Quad Flat Pack <sup>1</sup>	N74F8962Y, N74F8963Y
44-pin Plastic Leaded Chip Carrier	N74F8962A, N74F8963A

### Note to ordering information

1. Flatpack package is not available at this time.

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A10 – A18	PNP latched inputs	1.0/0.167	20 $\mu$ A/100 $\mu$ A
B0 – B8	Data inputs with threshold circuitry	5.0/0.167	100 $\mu$ A/100 $\mu$ A
$\overline{OE}A\overline{B}$ , $\overline{OE}B\overline{A}$	Output enable inputs (active low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{LE}A\overline{B}$ , $\overline{LE}B\overline{A}$	Latch enable inputs (active low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
AO0 – AO8	3-state outputs	150/40	3mA/24mA
B0 – B8	Open collector outputs	OC/166.7	OC/100mA

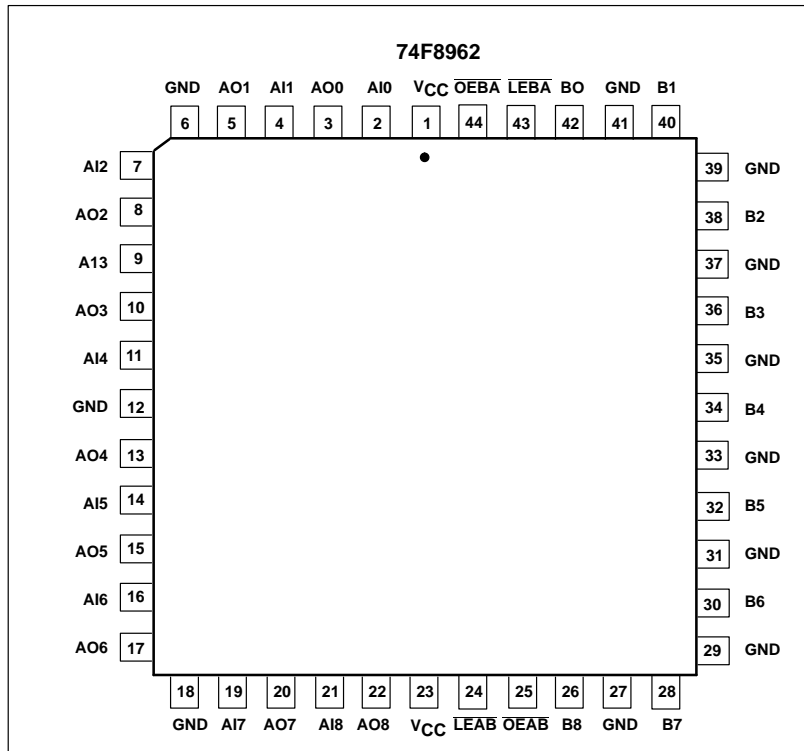
### Notes to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20 $\mu$ A in the high state and 0.6mA in the low state.
2. OC = Open collector.

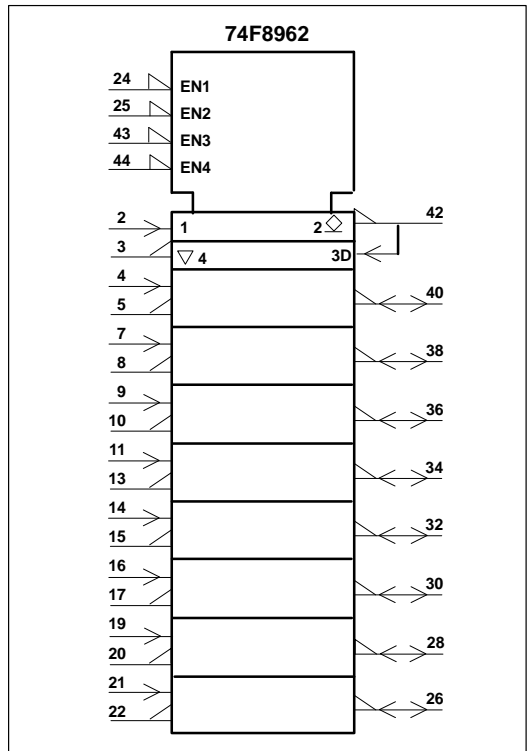
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## PIN CONFIGURATION FLATPACK AND PLCC



## IEC/IEEE SYMBOL



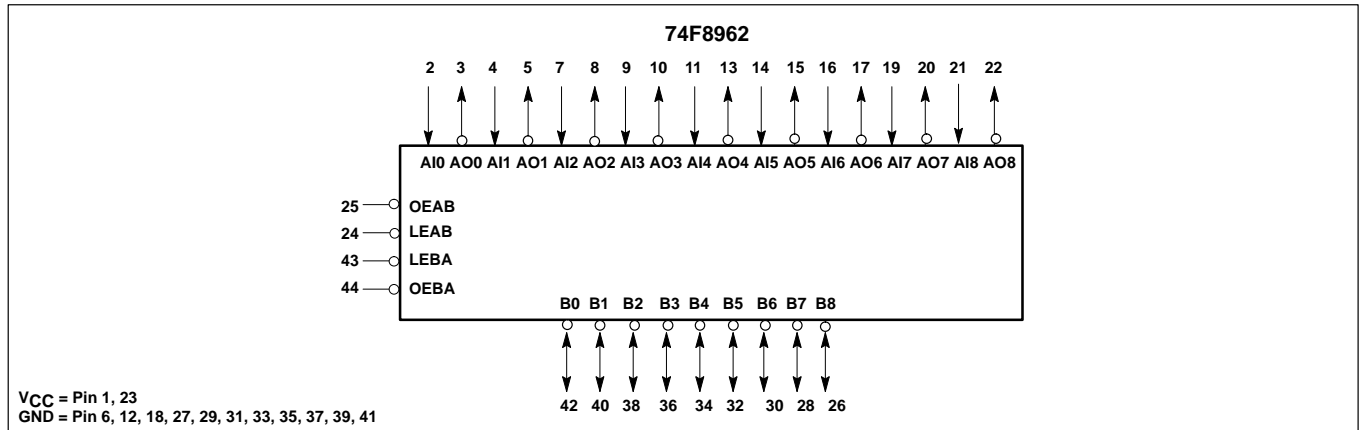
## PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
AI0 – AI8	2, 4, 7, 9, 11, 14, 16, 19, 21	Input	PNP latched inputs.
B0 – B8	42, 40, 38, 36, 34, 32, 30, 28, 26	I/O	Data input / open collector output, high current drives.
$\overline{OEAB}$	25	Input	Output enable input. Enables the B outputs when low.
$\overline{OEBA}$	44	Input	Output enable input. Enables the A outputs when high.
$\overline{LEAB}$	24	Input	Latch enable input. Enables the AB latches low.
$\overline{LEBA}$	43	Input	Latch enable input. Enables the BA latches low.
AO0 – AO8	3, 5, 8, 10, 13, 15, 17, 20, 22	Output	TTL 3–state outputs.
GND	6, 12, 18, 27, 29, 31, 33, 35, 37, 39, 41	Ground	Grounds
V <sub>CC</sub>	1, 23	Power	Positive supply voltages

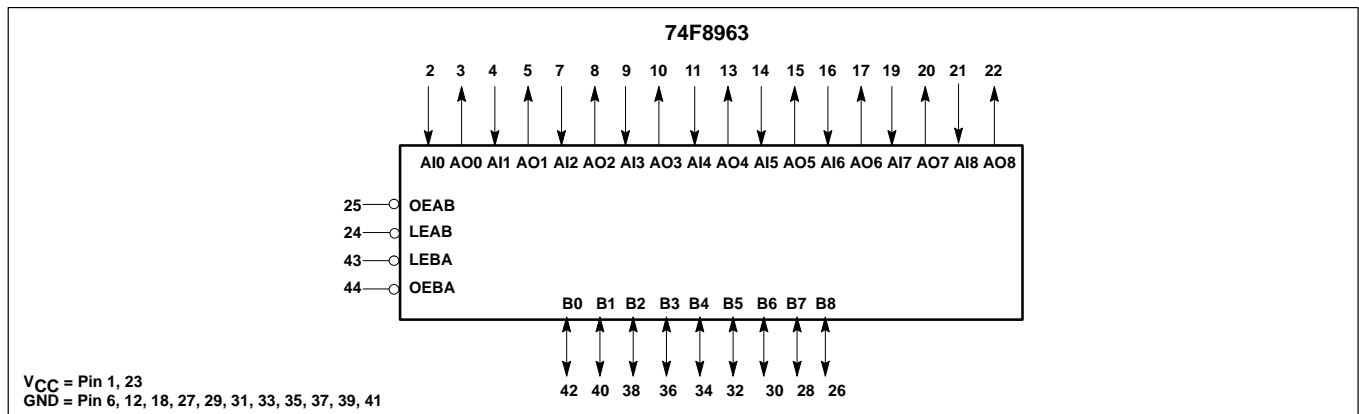
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## LOGIC SYMBOL FOR 74F8962



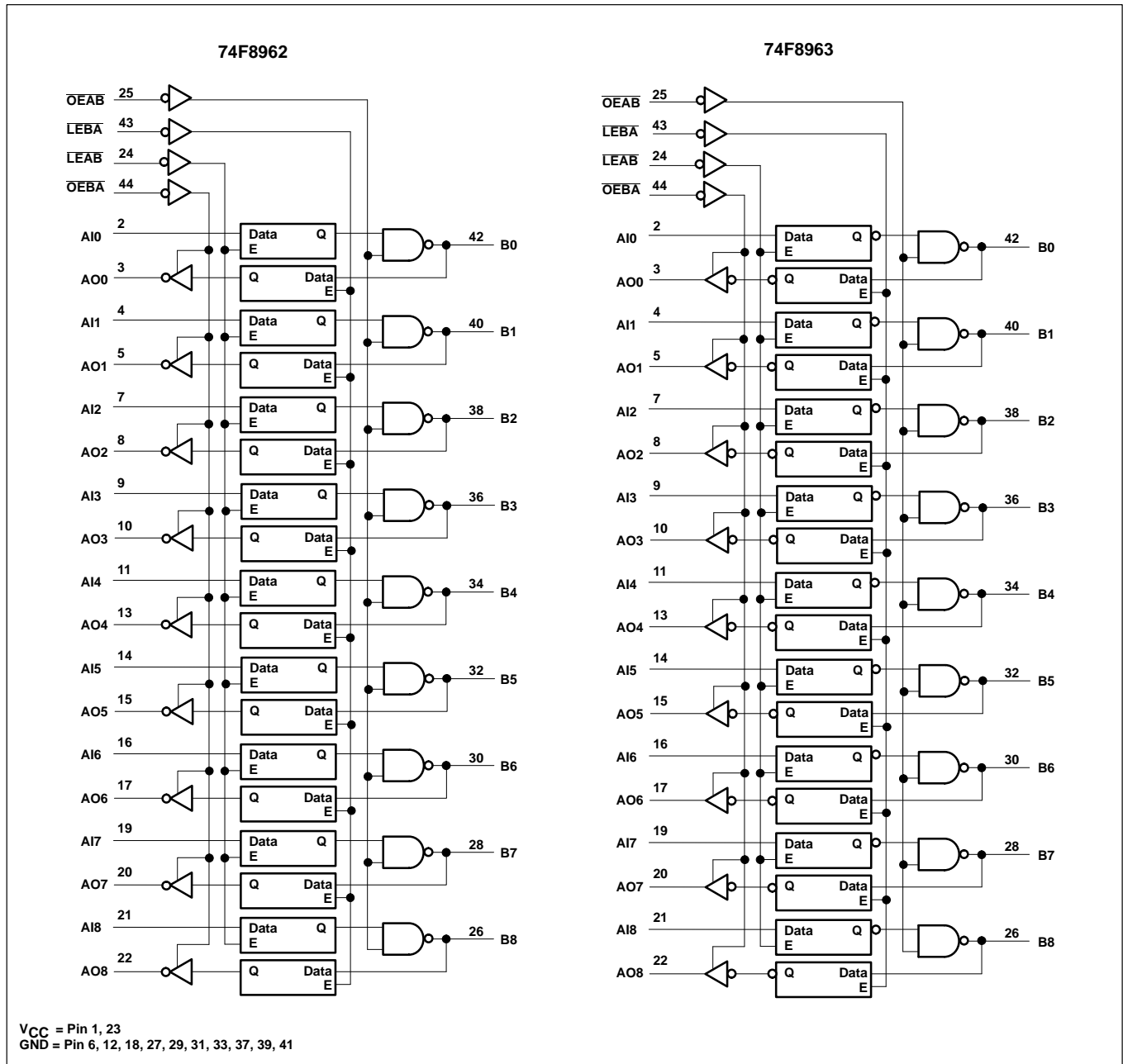
## LOGIC SYMBOL FOR 74F8963



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## LOGIC DIAGRAM



# 9-Bit latched bidirectional Futurebus transceivers (open-collector)

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**FUNCTION TABLE FOR 74F8962**

INPUTS						LATCH STATES		OUTPUTS		OPERATING MODE
AIn	Bn*	LEAB	LEBA	OEAB	OEBA	AB	BA	AOn	Bn	
H	H	L	L	H	H	H	H	Z	X	B and AO disabled
L	L	L	L	H	H	L	L	Z	X	
X	X	H	H	H	H	Qn	Qn	Z	X	
H	-	L	X	L	H	H	Qn	Z	L	AO 3-state, transparent data from AI to B
L	-	L	X	L	H	L	Qn	Z	H**	
X	H	X	L	H	L	Qn	H	L	X	B disabled, transparent data from B to AO
X	L	X	L	H	L	Qn	L	H	X	
X	X	H	X	L	H	Qn	Qn	Z	$\bar{Q}n$	AO 3-state, latched data to B
X	X	X	H	H	L	Qn	Qn	$\bar{Q}n$	X	B disabled, latched to AO
X	X	H	H	L	L	Qn	Qn	$\bar{Q}n$	$\bar{Q}n$	Latched state to AO and B
H	-	L	L	L	L	H	L	H	L	Read back from AI to B to AO (both latches transparent)
L	-	L	L	L	L	L	H	L	H**	

**Notes to function table for 74F8962**

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. - = Input not externally driven
5. Z = High impedance "off" state
6. Qn = High or low voltage level one setup time prior to the low-to-high  $\overline{LEXX}$  transition.
7. H\*\* = Goes to level of pullup voltage.
8. B\* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

**FUNCTION TABLE FOR 74F8963**

INPUTS						LATCH STATES		OUTPUTS		OPERATING MODE
AIn	Bn*	LEAB	LEBA	OEAB	OEBA	AB	BA	AOn	Bn	
H	H	L	L	H	H	L	L	Z	X	B and AO disabled
L	L	L	L	H	H	H	H	Z	X	
X	X	H	H	H	H	$\bar{Q}n$	$\bar{Q}n$	Z	X	
H	-	L	X	L	H	L	$\bar{Q}n$	Z	H	AO 3-state, transparent data from AI to B
L	-	L	X	L	H	H	$\bar{Q}n$	Z	L	
X	H	X	L	H	L	$\bar{Q}n$	L	H	X	B disabled, transparent data from B to AO
X	L	X	L	H	L	$\bar{Q}n$	H	L	X	
X	X	H	X	L	H	$\bar{Q}n$	$\bar{Q}n$	Z	$\bar{Q}n$	AO 3-state, latched data to B
X	X	X	H	H	L	$\bar{Q}n$	$\bar{Q}n$	Qn	X	B disabled, latched to AO
X	X	H	H	L	L	$\bar{Q}n$	$\bar{Q}n$	Qn	Qn	Latched state to AO and B
H	-	L	L	L	L	L	L	H	H**	Read back from AI to B to AO (both latches transparent)
L	-	L	L	L	L	H	L	L	L	

**Notes to function table for 74F8963**

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. - = Input not externally driven
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6. Qn = High or low voltage level one setup time prior to the low-to-high  $\overline{LEXX}$  transition.
7. H\*\* = Goes to level of pullup voltage.
8. B\* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

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## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	OEBA, OEAB, LEBA, LEAB	-0.5 to +7.0	V
		A10 – A18, B0 – B8	-0.5 to +5.5	V
I <sub>IN</sub>	Input current		-40 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state		-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in low output state	A00 – A08	48	mA
		B0 – B8	200	mA
T <sub>amb</sub>	Operating free air temperature range		0 to +70	°C
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	Except B0 – B8	2.0			V
		B0 – B8	1.62			V
V <sub>IL</sub>	Low-level input voltage	Except B0 – B8			0.8	V
		B0 – B8			1.47	V
I <sub>Ik</sub>	Input clamp current				-18	mA
I <sub>OH</sub>	High-level output current	A00 – A08			-3	mA
I <sub>OL</sub>	Low-level output current	A00 – A08			24	mA
		B0 – B8			100	mA
T <sub>amb</sub>	Operating free air temperature		0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
				MIN	TYP <sup>2</sup>	MAX		
$I_{OH}$	High-level output current	B0 – B8	$V_{CC} = \text{MAX}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$ , $V_{OH} = 2.1\text{V}$			100	$\mu\text{A}$	
$I_{OFF}$	Power-off output current	B0 – B8	$V_{CC} = 0.0\text{V}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$ , $V_{OH} = 2.1\text{V}$			100	$\mu\text{A}$	
$V_{OH}$	High-level output voltage	AO0 – AO8 <sup>4</sup>	$V_{CC} = \text{MAX}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$ , $I_{OH} = -3\text{mA}$	2.5		$V_{CC}$	V	
$V_{OL}$	Low-level output voltage	AO0 – AO8 <sup>4</sup>	$V_{CC} = \text{MIN}$ , $I_{OL} = 24\text{mA}$			0.50	V	
		B0 – B8	$V_{IL} = \text{MAX}$ $I_{OL} = 100\text{mA}$	0.75	1.0	1.10	V	
			$V_{IH} = \text{MIN}$ $I_{OL} = 4\text{mA}$	0.40			V	
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}$ , $I_I = I_{IK}$			-1.2	V	
$I_I$	Input current at maximum input voltage	OEAB, OEBA, LEAB, LEBA, A10 – A18	$V_{CC} = \text{MAX}$ , $V_I = 7.0\text{V}$			100	$\mu\text{A}$	
		B0 – B8	$V_{CC} = \text{MAX}$ , $V_I = 5.5\text{V}$			1	mA	
$I_{IH}$	High-level input current	OEAB, OEBA, LEAB, LEBA, A10 – A18	$V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$	
		B0 – B8	$V_{CC} = \text{MAX}$ , $V_I = 2.1\text{V}$			100	$\mu\text{A}$	
$I_{IL}$	Low-level input current	OEAB, OEBA, LEAB, LEBA, A10 – A18	$V_{CC} = \text{MAX}$ , $V_I = 0.5\text{V}$			-100	$\mu\text{A}$	
		B0 – B8	$V_{CC} = \text{MAX}$ , $V_I = 0.3\text{V}$			-100	$\mu\text{A}$	
$I_{OZH}$	Off state output current, high-level voltage applied	AO0 – AO8	$V_{CC} = \text{MAX}$ , $V_O = 2.7\text{V}$			50	$\mu\text{A}$	
$I_{OZL}$	Off state output current, low-level voltage applied		$V_{CC} = \text{MAX}$ , $V_I = 0.5\text{V}$			-50	$\mu\text{A}$	
$I_{OS}$	Short circuit output current <sup>3</sup>	AO0 – AO8	$V_{CC} = \text{MAX}$ , $B_n = 1.3\text{V}$ , $\overline{OEBA} = 0.8\text{V}$ , $\overline{OEAB} = 2.7\text{V}$	-60		-150	mA	
		only	$V_{CC} = \text{MAX}$ , $B_n = 1.8\text{V}$ , $\overline{OEBA} = 0.8\text{V}$ , $\overline{OEAB} = 2.7\text{V}$					
$I_{CC}$	Supply current (total)	$I_{CCH}$	$V_{CC} = \text{MAX}$			80	110	mA
		$I_{CCL}$	$V_{CC} = \text{MAX}$ , $V_{IL} = 0.5\text{V}$			105	145	mA
		$I_{CCZ}$				80	110	mA

### NOTES TO DC ELECTRICAL CHARACTERISTICS

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.
- Due to test equipment limitations, actual test conditions are for  $V_{IH} = 1.8\text{V}$  and  $V_{IL} = 1.3\text{V}$ .

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## AC ELECTRICAL CHARACTERISTICS FOR 74F8962

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
			$V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$V_{CC} = +5.0\text{V} \pm 5\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{PLH}$ $t_{PHL}$	Propagation delay Bn to AOn	Waveform 1, 2	5.0 3.5	7.0 5.5	10.0 8.5	4.5 3.5	11.0 8.5	4.5 3.5	10.5 8.5	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{LEBA}$ to AOn	Waveform 1, 2	5.5 4.5	7.0 6.5	10.0 9.5	5.0 4.5	10.0 9.5	5.0 4.5	10.0 9.5	ns	
$t_{PZH}$ $t_{PZL}$	Output enable time to high or low, OEBA to AOn	Waveform 5, 6	7.5 8.5	9.5 10.5	12.5 13.0	6.5 7.5	13.5 14.5	6.5 7.5	13.0 13.5	ns	
$t_{PHZ}$ $t_{PLZ}$	Output disable from high or low, $\overline{OEBA}$ to AOn	Waveform 5, 6	3.5 4.5	5.5 6.5	8.5 9.5	2.5 4.0	10.0 10.0	2.5 4.0	9.0 9.5	ns	
$t_{sk(o)}$	Skew between receivers in same package	Waveform 4		1.5	2.0		4.0		4.0	ns	
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
			$V_{CC} = +5.0\text{V}$ $C_D = 30\text{pF}$ $R_U = 9\Omega$			$V_{CC} = +5.0\text{V} \pm 10\%$ $C_D = 30\text{pF}$ $R_U = 9\Omega$		$V_{CC} = +5.0\text{V} \pm 5\%$ $C_D = 30\text{pF}$ $R_U = 9\Omega$			
MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{PLH}$ $t_{PHL}$	Propagation delay AIn to Bn	Waveform 1, 2	3.5 4.0	5.5 6.0	8.5 9.5	3.0 3.5	9.0 10.5	3.0 3.5	9.0 10.0	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{LEAB}$ to Bn	Waveform 1, 2	4.0 5.0	6.0 7.0	8.5 10.5	3.5 5.0	9.5 10.5	3.5 5.0	9.5 10.5	ns	
$t_{PLH}$ $t_{PHL}$	Output enable/disable time OEBA to Bn	Waveform 1	3.5 3.0	5.0 4.0	8.0 8.0	3.0 2.5	8.5 8.5	3.0 2.5	8.0 8.5	ns	
$t_{TLH}$ $t_{THL}$	Transition time, Bn port 10% to 90%, 90% to 10%	Test circuit and waveforms	1.0 1.0	1.2 2.0	1.6 2.5	1.0 1.0	2.5 3.5	1.0 1.0	2.5 3.5	ns	
$t_{sk(o)}$	Skew between drivers in same package	Waveform 4		0.5	2.5		3.0		3.0	ns	

## AC SETUP REQUIREMENTS FOR 74F8962

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
			$V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$V_{CC} = +5.0\text{V} \pm 5\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{su(H)}$ $t_{su(L)}$	Setup time, high or low AIn to $\overline{LEAB}$	Waveform 3	3.0 1.0			3.5 2.0		3.0 1.5		ns	
$t_h(H)$ $t_h(L)$	Hold time, high or low AIn to $\overline{LEAB}$	Waveform 3	3.0 0.0			3.5 0.0		3.0 0.0		ns	
$t_{su(H)}$ $t_{su(L)}$	Setup time, high or low Bn to $\overline{LEBA}$	Waveform 3	2.0 1.0			2.5 1.0		2.0 1.0		ns	
$t_h(H)$ $t_h(L)$	Hold time, high or low Bn to $\overline{LEBA}$	Waveform 3	3.0 1.5			3.5 2.0		3.0 2.0		ns	
$t_w(L)$	$\overline{LEAB}$ or $\overline{LEBA}$ pulse width, low	Waveform 3	4.5			4.5		4.5		ns	



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## AC ELECTRICAL CHARACTERISTICS FOR 74F8963

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
			$V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$V_{CC} = +5.0\text{V} \pm 5\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{PLH}$ $t_{PHL}$	Propagation delay Bn to AOn	Waveform 1, 2	3.5 2.5	5.5 4.0	8.0 7.0	3.0 2.0	9.0 7.5	3.0 2.0	8.0 7.5	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{\text{LEBA}}$ to AOn	Waveform 1, 2	6.0 4.0	7.5 5.5	10.0 8.5	5.0 3.5	11.5 9.0	5.0 3.5	10.0 8.5	ns	
$t_{PZH}$ $t_{PZL}$	Output enable time to high or low, OEBA to AOn	Waveform 5, 6	9.0 10.0	11.0 12.0	15.0 16.0	8.5 9.0	16.5 18.0	8.5 9.0	15.5 16.5	ns	
$t_{PHZ}$ $t_{PLZ}$	Output disable time from high or low, OEBA to AOn	Waveform 5, 6	4.0 5.5	6.0 7.0	9.0 11.0	3.0 5.0	10.5 12.0	3.0 5.0	9.5 11.0	ns	
$t_{sk(o)}$	Skew between receivers in same package	Waveform 4		1.5	2.0		4.0		4.0	ns	
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
			$V_{CC} = +5.0\text{V}$ $C_D = 30\text{pF}$ $R_U = 9\Omega$			$V_{CC} = +5.0\text{V} \pm 10\%$ $C_D = 30\text{pF}$ $R_U = 9\Omega$		$V_{CC} = +5.0\text{V} \pm 5\%$ $C_D = 30\text{pF}$ $R_U = 9\Omega$			
MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{PLH}$ $t_{PHL}$	Propagation delay AIn to Bn	Waveform 1, 2	2.0 2.0	4.0 3.5	6.5 6.5	1.5 1.5	7.0 6.5	2.0 2.0	7.0 6.5	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{\text{LEAB}}$ to Bn	Waveform 1, 2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 8.0	3.5 2.5	8.5 8.0	ns	
$t_{PLH}$ $t_{PHL}$	Output enable/disable time OEBA to Bn	Waveform 1	3.5 3.0	5.5 5.0	9.0 7.5	2.5 2.5	9.5 8.5	2.5 2.5	9.0 8.0	ns	
$t_{TLH}$ $t_{THL}$	Transition time, Bn port 10% to 90%, 90% to 10%	Test circuit and waveforms	1.0 1.0	1.2 2.0	1.6 2.5	1.0 1.0	2.5 3.5	1.0 1.0	2.5 3.5	ns	
$t_{sk(o)}$	Skew between drivers in same package	Waveform 4		0.5	2.0		3.0		3.0	ns	

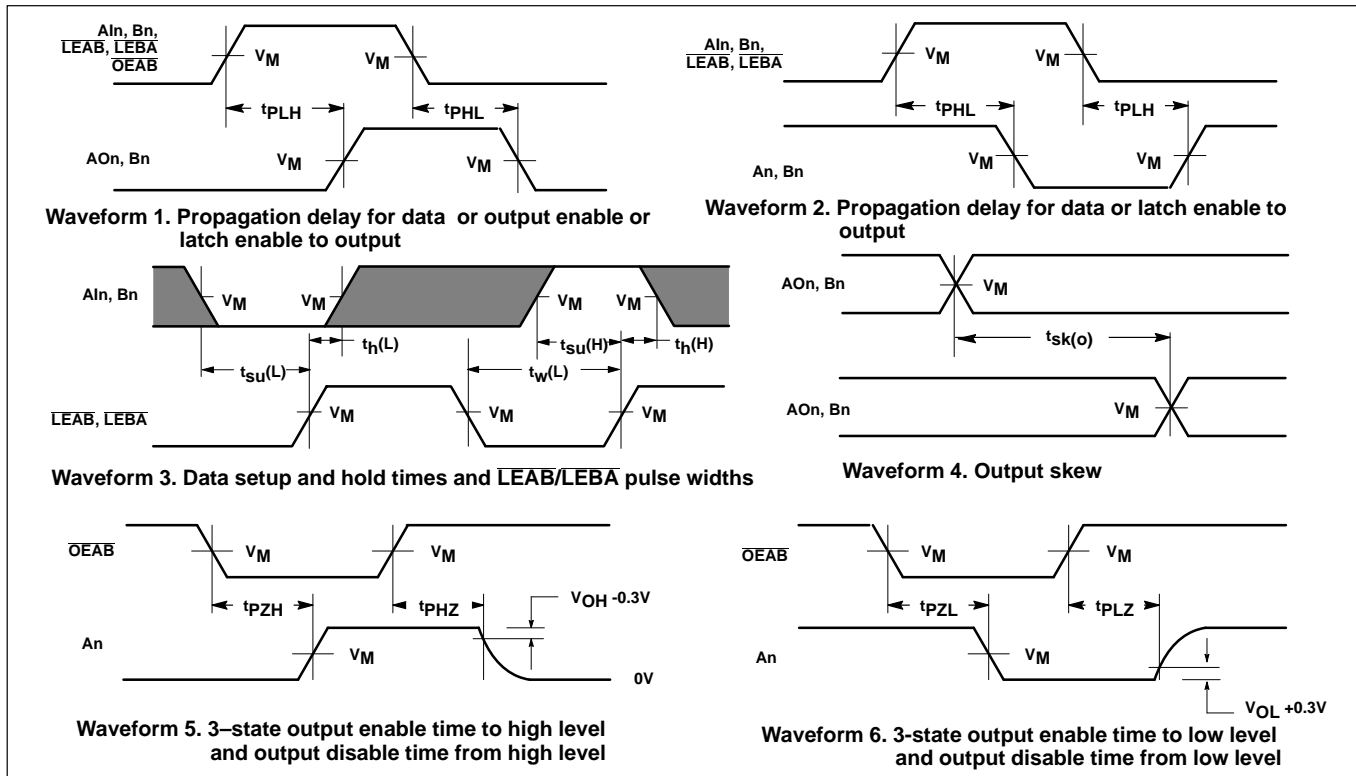
## AC SETUP REQUIREMENTS FOR 74F8963

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			
			$V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$V_{CC} = +5.0\text{V} \pm 5\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{su(H)}$ $t_{su(L)}$	Setup time, high or low AIn to $\overline{\text{LEAB}}$	Waveform 3	4.0 1.0			4.5 1.5		4.0 1.0		ns	
$t_h(H)$ $t_h(L)$	Hold time, high or low AIn to $\overline{\text{LEAB}}$	Waveform 3	2.5 0.0			3.0 0.0		2.5 0.0		ns	
$t_{su(H)}$ $t_{su(L)}$	Setup time, high or low Bn to $\overline{\text{LEBA}}$	Waveform 3	2.0 1.0			2.5 1.0		2.0 1.0		ns	
$t_h(H)$ $t_h(L)$	Hold time, high or low Bn to $\overline{\text{LEBA}}$	Waveform 3	2.5 1.0			3.0 1.5		3.0 1.0		ns	
$t_w(L)$	$\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ pulse width, low	Waveform 3	4.5			5.5		5.5		ns	

# 9-Bit latched bidirectional Futurebus transceivers (open-collector)

74F8962/8963

## AC WAVEFORMS



### NOTES TO AC WAVEFORMS

- For all waveforms,  $V_M = 1.5V$ .
- The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUITS AND WAVEFORMS

