

# NLAST4051

## Analog Multiplexer/ Demultiplexer

### TTL Compatible, Single-Pole, 8-Position Plus Common Off

The NLAST4051 is an improved version of the MC14051 and MC74HC4051 fabricated in sub-micron Silicon Gate CMOS technology for lower  $R_{DS(on)}$  resistance and improved linearity with low current. This device may be operated either with a single supply or dual supply up to  $\pm 3$  V to pass a 6 V<sub>PP</sub> signal without coupling capacitors.

When operating in single supply mode, it is only necessary to tie V<sub>EE</sub>, pin 7 to ground. For dual supply operation, V<sub>EE</sub> is tied to a negative voltage, not to exceed maximum ratings. Translation is provided in the device, the Address and Inhibit are standard TTL level compatible. For CMOS compatibility see NLAS4051. Pin for pin compatible with all industry standard versions of '4051.'

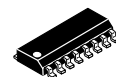
- Improved  $R_{DS(on)}$  Specifications
- Pin for Pin Replacement for MAX4051 and MAX4051A
  - One Half the Resistance Operating at 5.0 Volts
- Single or Dual Supply Operation
  - Single 3–5 Volt Operation, or Dual  $\pm 3$  Volt Operation
  - With V<sub>CC</sub> of 3.0 to 3.3 V, Device Can Interface with 1.8 V Logic, No Translators Needed
  - Address and Inhibit Logic are Over-Voltage Tolerant and May Be Driven Up +6 V Regardless of V<sub>CC</sub>
- Address and Inhibit Pins Standard TTL Compatible
  - Greatly Improved Noise Margin Over MAX4051 and MAX4051A
  - True TTL Compatibility V<sub>IL</sub> = 0.8 V, V<sub>IH</sub> = 2.0 V
- Improved Linearity Over Standard HC4051 Devices
- Popular SOIC, and Space Saving TSSOP, and QSOP 16 Pin Packages



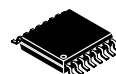
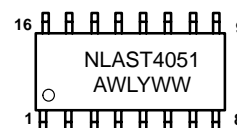
ON Semiconductor®

<http://onsemi.com>

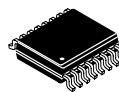
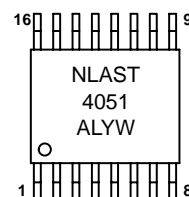
#### MARKING DIAGRAMS



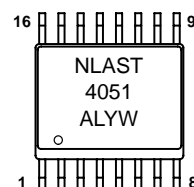
SO-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



QSOP-16  
QS SUFFIX  
CASE 492



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W = Work Week

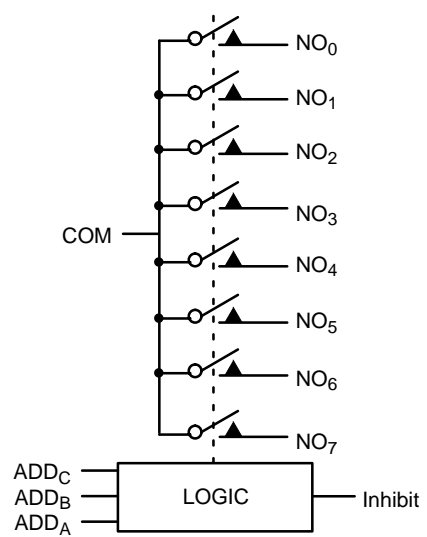
#### ORDERING INFORMATION

Device	Package	Shipping
NLAST4051D	SO-16	48 Units/Rail
NLAST4051DR2	SO-16	2500 Units/Reel
NLAST4051DT	TSSOP-16	96 Units/Rail
NLAST4051DTR2	TSSOP-16	2500 Units/Reel
NLAST4051QS	QSOP-16	98 Units/Rail
NLAST4051QSR	QSOP-16	2500 Units/Reel

# NLAST4051



**Figure 1. Pin Connection**  
(Top View)



**Figure 2. Logic Diagram**

## TRUTH TABLE

Inhibit	Address			ON SWITCHES*
	C	B	A	
1	X don't care	X don't care	X don't care	All switches open
0	0	0	0	COM-NO <sub>0</sub>
0	0	0	1	COM-NO <sub>1</sub>
0	0	1	0	COM-NO <sub>2</sub>
0	0	1	1	COM-NO <sub>3</sub>
0	1	0	0	COM-NO <sub>4</sub>
0	1	0	1	COM-NO <sub>5</sub>
0	1	1	0	COM-NO <sub>6</sub>
0	1	1	1	COM-NO <sub>7</sub>

\*NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

# NLAST4051

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$V_{EE}$	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +0.5	V
$V_{CC}$	Positive DC Supply Voltage (Note 2) (Referenced to GND) (Referenced to $V_{EE}$ )	-0.5 to +7.0 -0.5 to +7.0	V
$V_{IS}$	Analog Input Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
$V_{IN}$	Digital Input Voltage (Referenced to GND)	-0.5 to 7.0	V
I	DC Current, Into or Out of Any Pin	$\pm 50$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction Temperature under Bias	+150	°C
$\theta_{JA}$	Thermal Resistance SOIC TSSOP QSOP	143 164 164	°C/W
$P_D$	Power Dissipation in Still Air, SOIC TSSOP QSOP	500 450 450	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 > 1000	V
$I_{LATCH-UP}$	Latch-Up Performance Above $V_{CC}$ and Below GND at 125°C (Note 6)	$\pm 300$	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. The absolute value of  $V_{CC} \pm |V_{EE}| \leq 7.0$ .
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{EE}$	Negative DC Supply Voltage (Referenced to GND)	-5.5	GND	V
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	2.5 2.5	5.5 6.6	V
$V_{IS}$	Analog Input Voltage	$V_{EE}$	$V_{CC}$	V
$V_{IN}$	Digital Input Voltage (Note 7) (Referenced to GND)	0	5.5	V
$T_A$	Operating Temperature Range, All Package Types	-55	125	°C
$t_r, t_f$	Input Rise/Fall Time (Channel Select or Enable Inputs) $V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0	100 20	ns/V

7. Unused digital inputs may not be left open. All digital inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

# NLAST4051

## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage, Address or Inhibit Inputs		3.0	1.6	1.6	1.6	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, Address or Inhibit Inputs		3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
I <sub>IN</sub>	Maximum Input Leakage Current, Address or Inhibit Inputs	V <sub>IN</sub> = 6.0 or GND	0 V to 6.0 V	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	Address or Inhibit and V <sub>IS</sub> = V <sub>CC</sub> or GND	6.0	4.0	40	80	μA

## DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	V <sub>EE</sub> V	Guaranteed Limit			Unit
					-55 to 25°C	≤ 85°C	≤ 125°C	
R <sub>ON</sub>	Maximum "ON" Resistance	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = (V <sub>EE</sub> to V <sub>CC</sub> )  I <sub>S</sub>   = 10 mA (Figures 4 thru 9)	3.0	0	86	108	120	Ω
			4.5	0	37	46	55	
			3.0	-3.0	26	33	37	
ΔR <sub>ON</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ,  I <sub>S</sub>   = 10 mA, V <sub>IS</sub> = 2.0 V V <sub>IS</sub> = 3.0 V V <sub>IS</sub> = 2.0 V	3.0	0	15	20	20	Ω
			4.5	0	13	18	18	
			3.0	-3.0	10	15	15	
R <sub>flat(ON)</sub>	ON Resistance Flatness	V <sub>COM</sub> = 1, 2, 3.5 V V <sub>COM</sub> = 2, 0, 2 V	4.5	3.0	4	4	5	Ω
			3.0		2	2	3	
I <sub>NC(OFF)</sub> I <sub>NO(OFF)</sub>	Maximum Off-Channel Leakage Current	Switch Off V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> -1.0 V or V <sub>EE</sub> +1.0 V (Figure 17)	6.0	0	0.1	5.0	100	nA
			3.0	-3.0	0.1	5.0	100	
I <sub>COM(ON)</sub>	Maximum On-Channel Leakage Current, Channel- to-Channel	Switch On V <sub>IO</sub> = V <sub>CC</sub> -1.0 V or V <sub>EE</sub> +1.0 V (Figure 17)	6.0	0	0.1	5.0	100	nA
			3.0	-3.0	0.1	5.0	100	

# NLAST4051

## AC CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	V <sub>EE</sub> V	Guaranteed Limit				Unit
					-55 to 25°C		≤ 85°C	≤ 125°C	
					Min	Typ*			
t <sub>BBM</sub>	Minimum Break-Before-Make Time	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF (Figure 19)	3.0	0.0	1.0	6.5	–	–	ns
			4.5	0.0	1.0	5.0	–	–	
			3.0	-3.0	1.0	3.5	–	–	

\*Typical Characteristics are at 25°C.

## AC CHARACTERISTICS (C<sub>L</sub> = 35 pF, Input $t_r = t_f = 3$ ns)

Symbol	Parameter	V <sub>CC</sub> V	V <sub>EE</sub> V	Guaranteed Limit						Unit	
				-55 to 25°C			≤ 85°C		≤ 125°C		
				Min	Typ	Max	Min	Max	Min		Max
t <sub>TRANS</sub>	Transition Time (Address Selection Time) (Figure 18)	2.5	0			40		45		50	ns
		3.0	0			28		30		35	
		4.5	0			23		25		30	
		3.0	-3.0			23		25		28	
t <sub>ON</sub>	Turn-on Time (Figures 14, 15, 20, and 21) Enable to N <sub>O</sub> or N <sub>C</sub>	2.5	0			40		45		50	ns
		3.0	0			28		30		35	
		4.5	0			23		25		30	
		3.0	-3.0			23		25		28	
t <sub>OFF</sub>	Turn-off Time (Figures 14, 15, 20, and 21) Enable to N <sub>O</sub> or N <sub>C</sub>	2.5	0			40		45		50	ns
		3.0	0			28		30		35	
		4.5	0			23		25		30	
		3.0	-3.0			23		25		28	

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
C <sub>IN</sub>	Maximum Input Capacitance, Select Inputs	8	
C <sub>NO</sub> or C <sub>NC</sub>	Analog I/O	10	
C <sub>COM</sub>	Common I/O	10	
C <sub>(ON)</sub>	Feedthrough	1.0	

# NLAST4051

## ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Typ	Unit
					25°C	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response	V <sub>IS</sub> = ½ (V <sub>CC</sub> - V <sub>EE</sub> ) Source Amplitude = 0 dBm (Figures 10 and 22)	3.0	0.0	80	MHz
			4.5	0.0	90	
			6.0	0.0	95	
			3.0	-3.0	95	
V <sub>ISO</sub>	Off-Channel Feedthrough Isolation	f = 100 kHz; V <sub>IS</sub> = ½ (V <sub>CC</sub> - V <sub>EE</sub> ) Source = 0 dBm (Figures 12 and 22)	3.0	0.0	-93	dB
			4.5	0.0	-93	
			6.0	0.0	-93	
			3.0	-3.0	-93	
V <sub>ONL</sub>	Maximum Feedthrough On Loss	V <sub>IS</sub> = ½ (V <sub>CC</sub> - V <sub>EE</sub> ) Source = 0 dBm (Figures 10 and 22)	3.0	0.0	-2	dB
			4.5	0.0	-2	
			6.0	0.0	-2	
			3.0	-3.0	-2	
Q	Charge Injection	V <sub>IN</sub> = V <sub>CC</sub> to V <sub>EE</sub> , f <sub>IS</sub> = 1 kHz, t <sub>r</sub> = t <sub>f</sub> = 3 ns R <sub>IS</sub> = 0 Ω, C <sub>L</sub> = 1000 pF, Q = C <sub>L</sub> * ΔV <sub>OUT</sub> (Figures 16 and 23)	5.0	0.0	9.0	pC
			3.0	-3.0	12	
THD	Total Harmonic Distortion THD + Noise	f <sub>IS</sub> = 1 MHz, R <sub>L</sub> = 10 KΩ, C <sub>L</sub> = 50 pF, V <sub>IS</sub> = 5.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 6.0 V <sub>PP</sub> sine wave (Figure 13)	6.0	0.0	0.10	%
			3.0	-3.0	0.05	

# NLAST4051

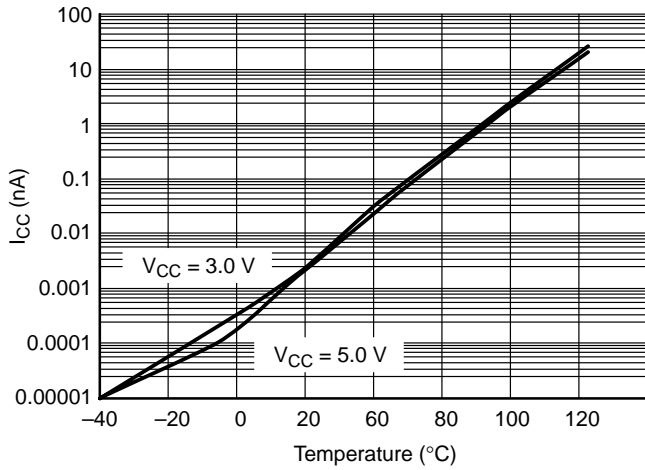


Figure 3.  $I_{CC}$  versus Temp,  $V_{CC} = 3\text{ V}$  and  $5\text{ V}$

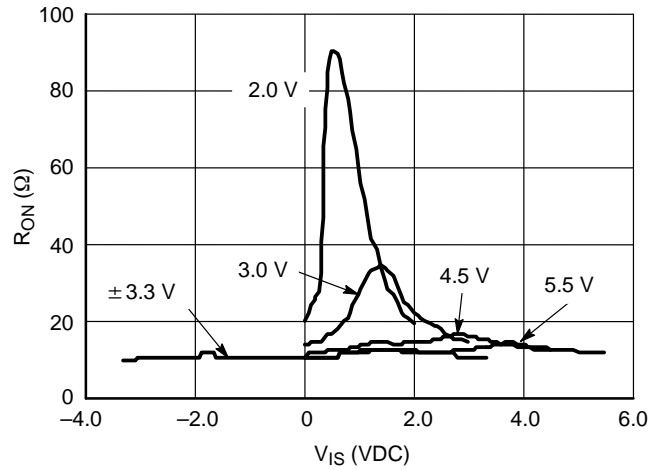


Figure 4.  $R_{ON}$  versus  $V_{CC}$ , Temp =  $25^{\circ}\text{C}$

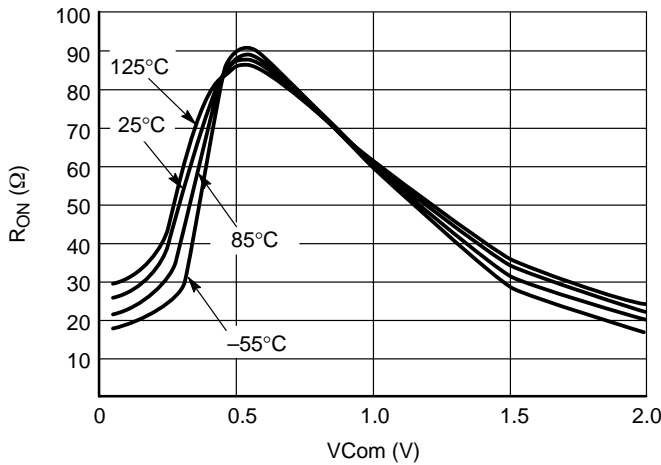


Figure 5. Typical On Resistance  
 $V_{CC} = 2.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$

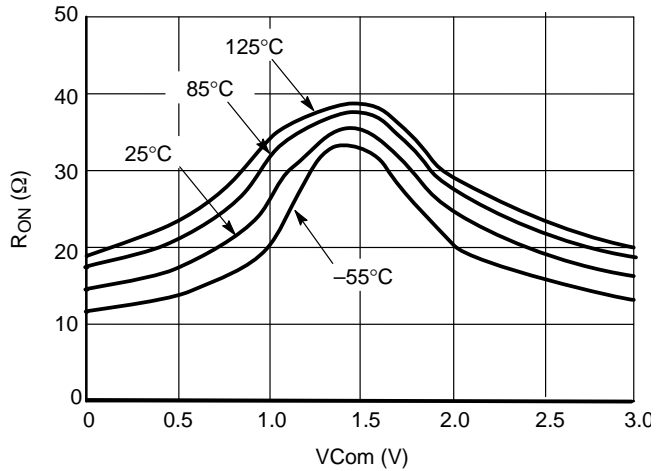


Figure 6. Typical On Resistance  
 $V_{CC} = 3.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$

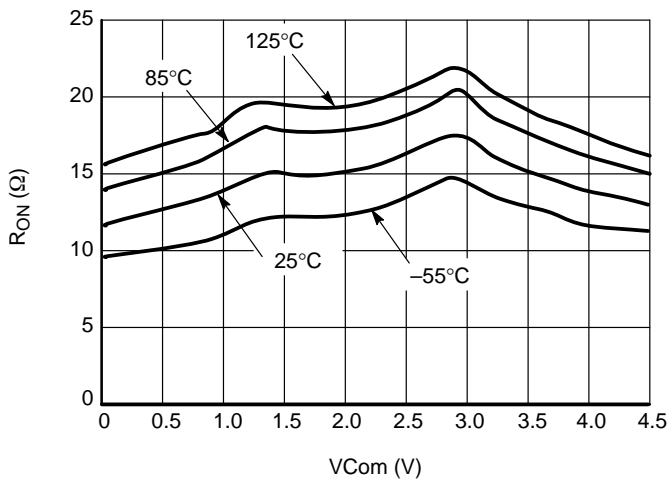


Figure 7. Typical On Resistance  
 $V_{CC} = 4.5\text{ V}$ ,  $V_{EE} = 0\text{ V}$

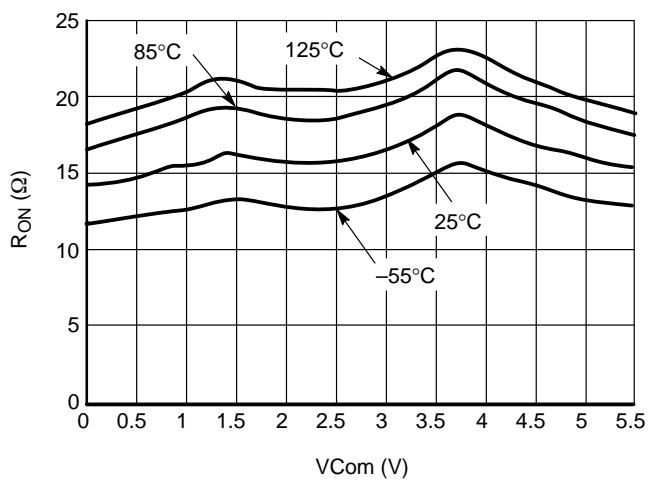
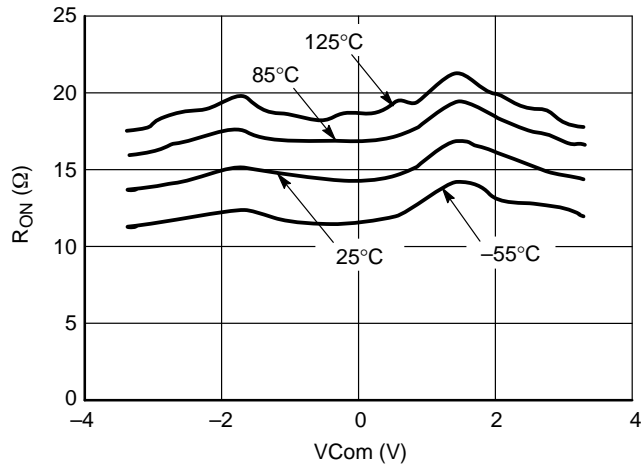
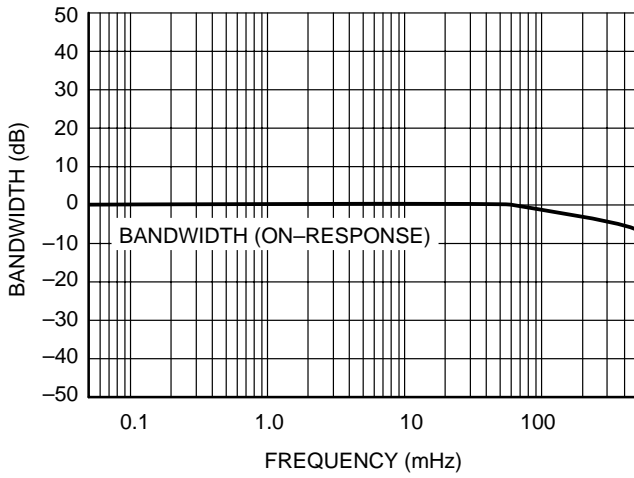


Figure 8. Typical On Resistance  
 $V_{CC} = 5.5\text{ V}$ ,  $V_{EE} = 0\text{ V}$

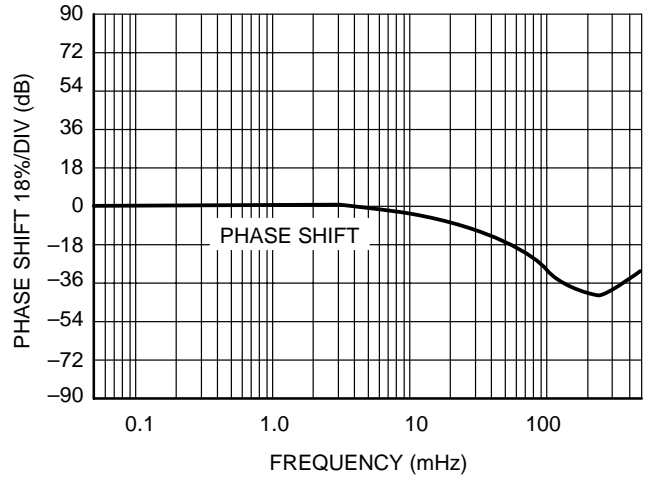
# NLAST4051



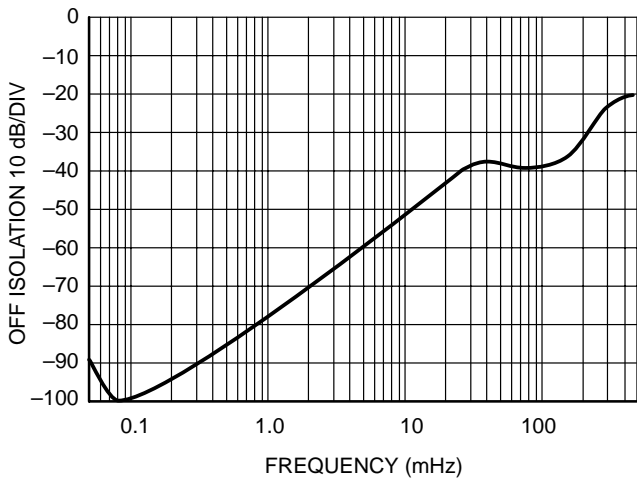
**Figure 9. Typical On Resistance**  
 $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = -3.3\text{ V}$



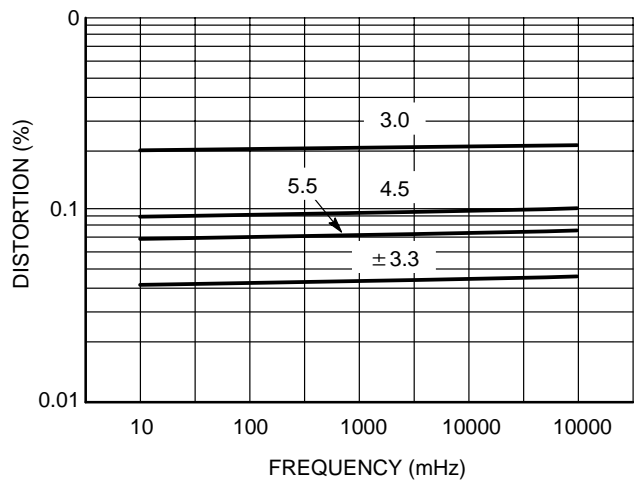
**Figure 10. Bandwidth**



**Figure 11. Phase Shift**



**Figure 12. Off Isolation**



**Figure 13. Total Harmonic Distortion**



# NLAST4051

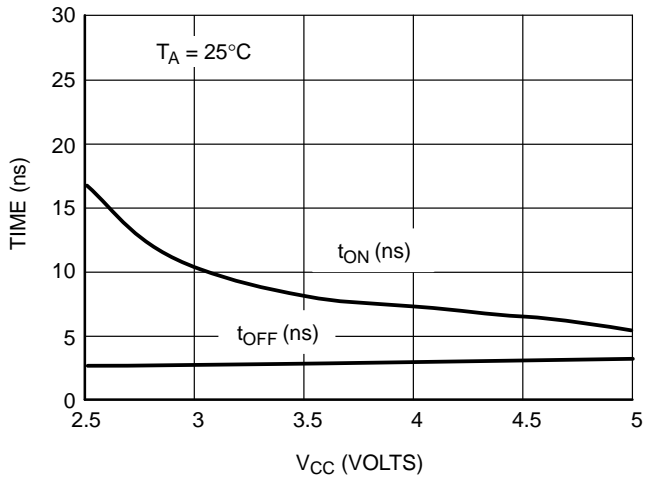


Figure 14.  $t_{ON}$  and  $t_{OFF}$  versus  $V_{CC}$

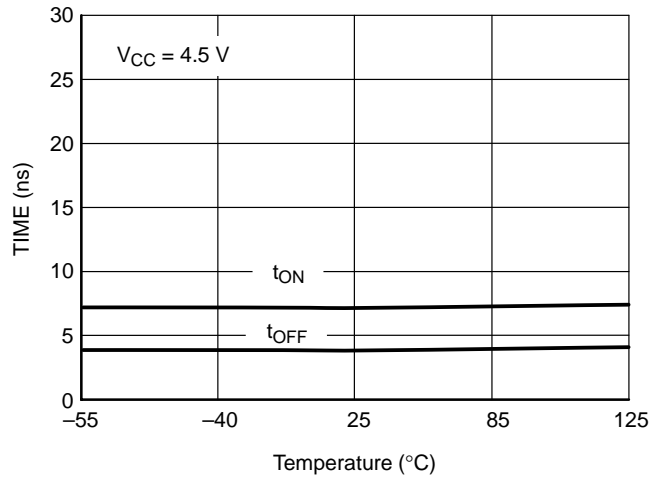


Figure 15.  $t_{ON}$  and  $t_{OFF}$  versus Temp

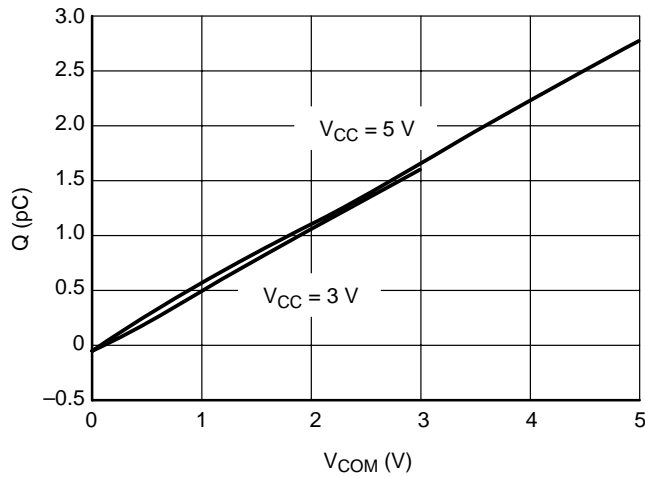


Figure 16. Charge Injection versus COM Voltage

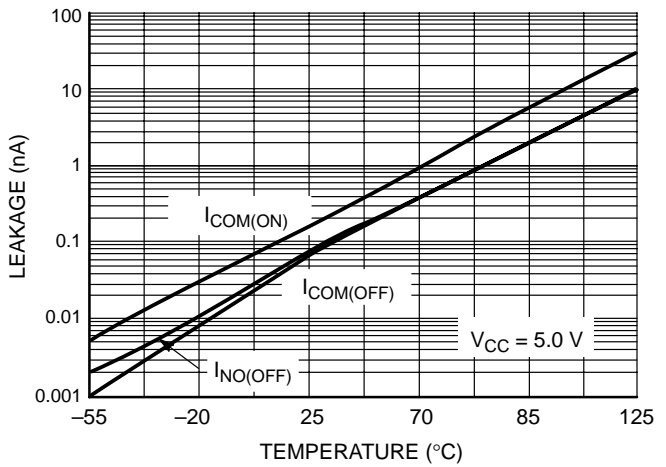


Figure 17. Switch Leakage versus Temperature

# NLAST4051

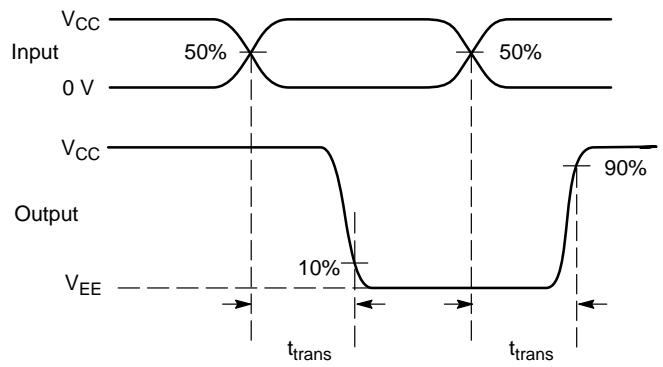
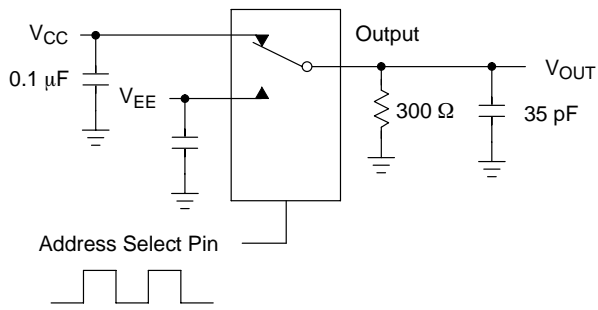


Figure 18. Channel Selection Propagation Delay

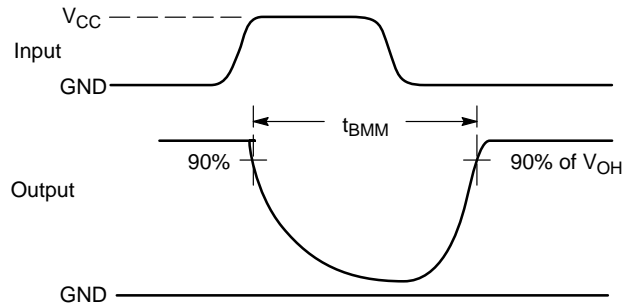
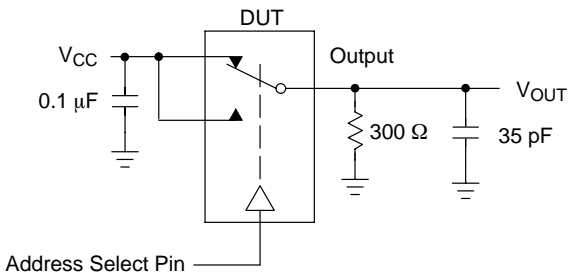


Figure 19.  $t_{BMM}$  (Time Break-Before-Make)

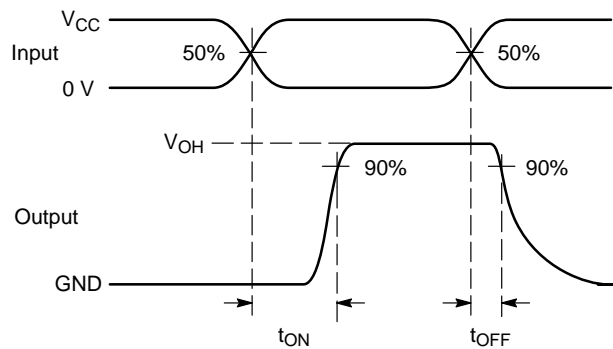
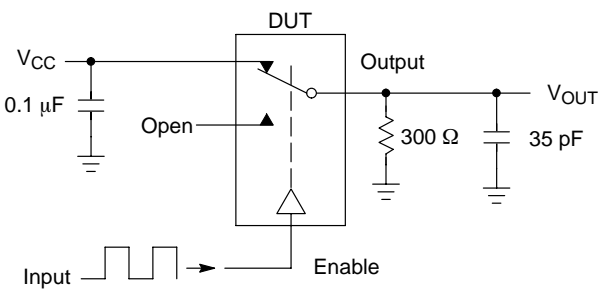


Figure 20.  $t_{ON}/t_{OFF}$

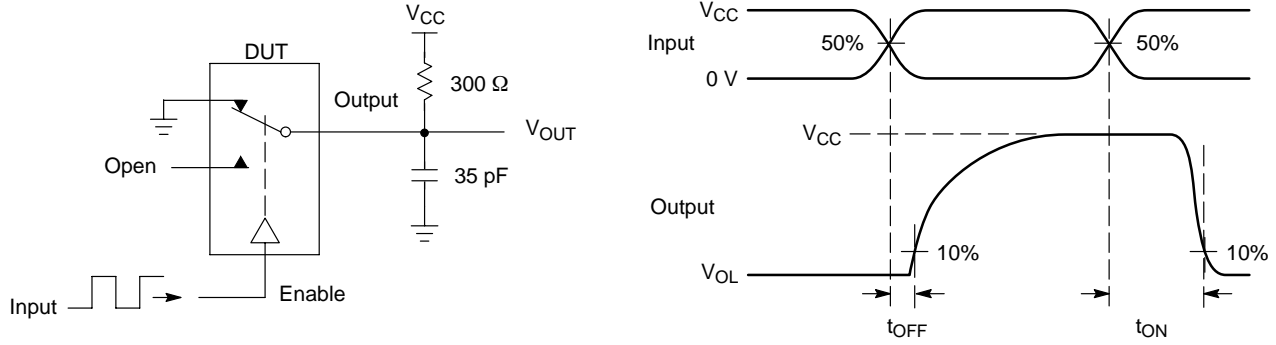
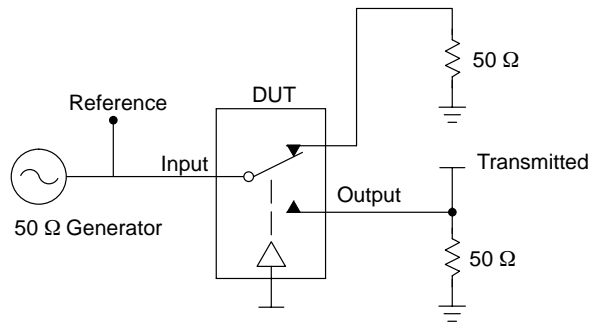


Figure 21.  $t_{ON}/t_{OFF}$



Channel switch Address and Inhibit/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

Figure 22. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$

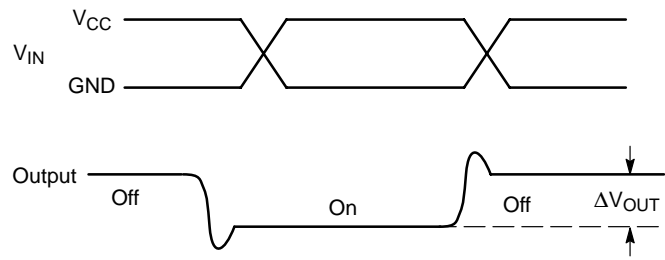
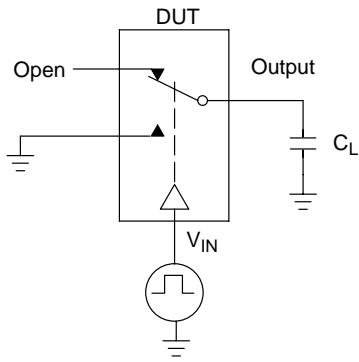


Figure 23. Charge Injection: (Q)

TYPICAL OPERATION

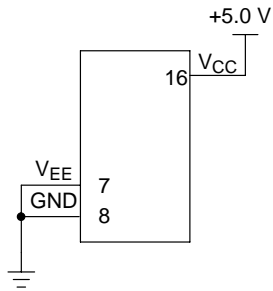


Figure 24. 5.0 Volts Single Supply  
 $V_{CC} = 5.0 \text{ V}$ ,  $V_{EE} = 0$

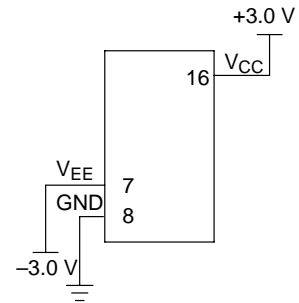
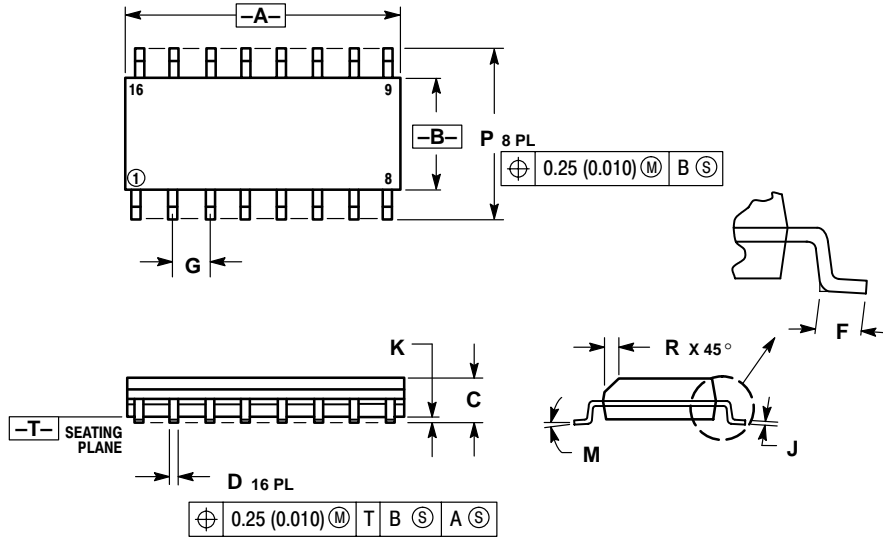


Figure 25. Dual Supply  
 $V_{CC} = 3.0 \text{ V}$ ,  $V_{EE} = -3.0 \text{ V}$

# NLAST4051

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



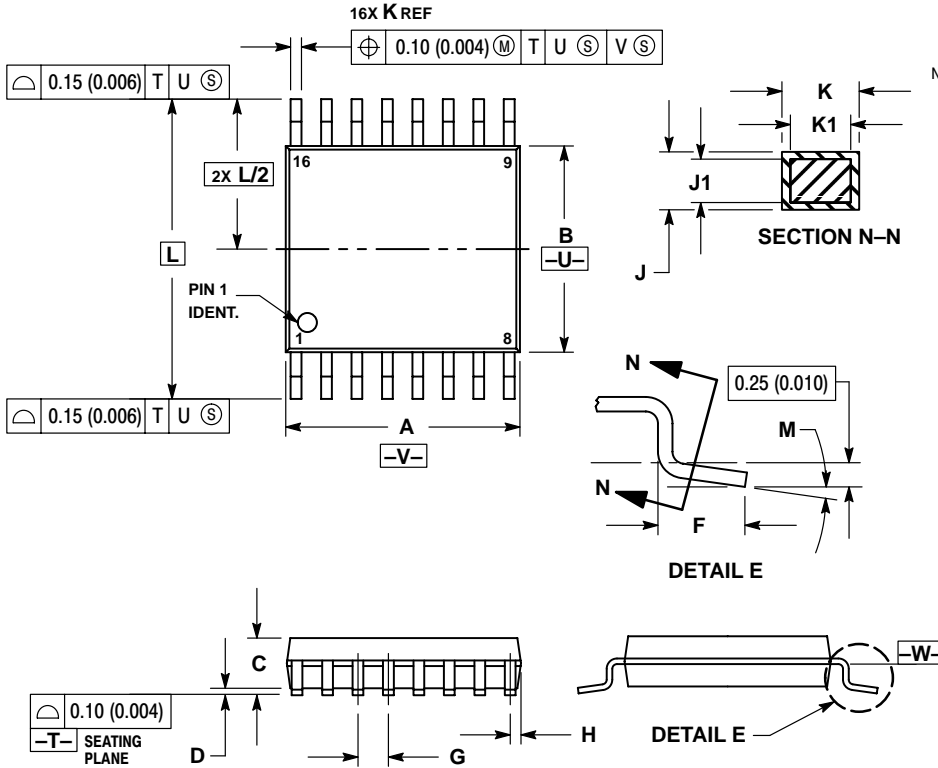
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# NLAST4051

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



**NOTES:**

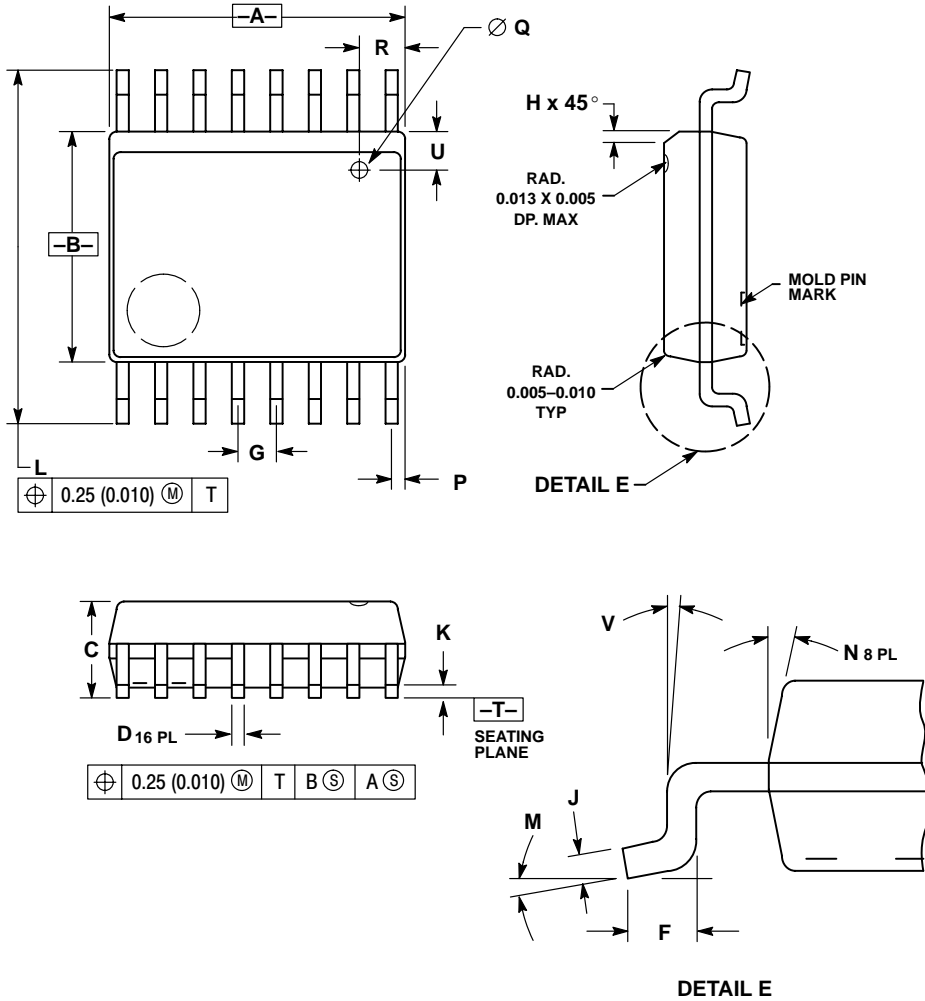
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# NLAST4051

## PACKAGE DIMENSIONS


QSOP-16  
 QS SUFFIX  
 CASE 492-01  
 ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
V	0°	8°	0°	8°

**ON Semiconductor** is a trademark and  is a registered trademark of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.