LOW SKEW CMOS PLL CLOCK DRIVER WITH INTEGRATED LOOP FILTER

QS5935

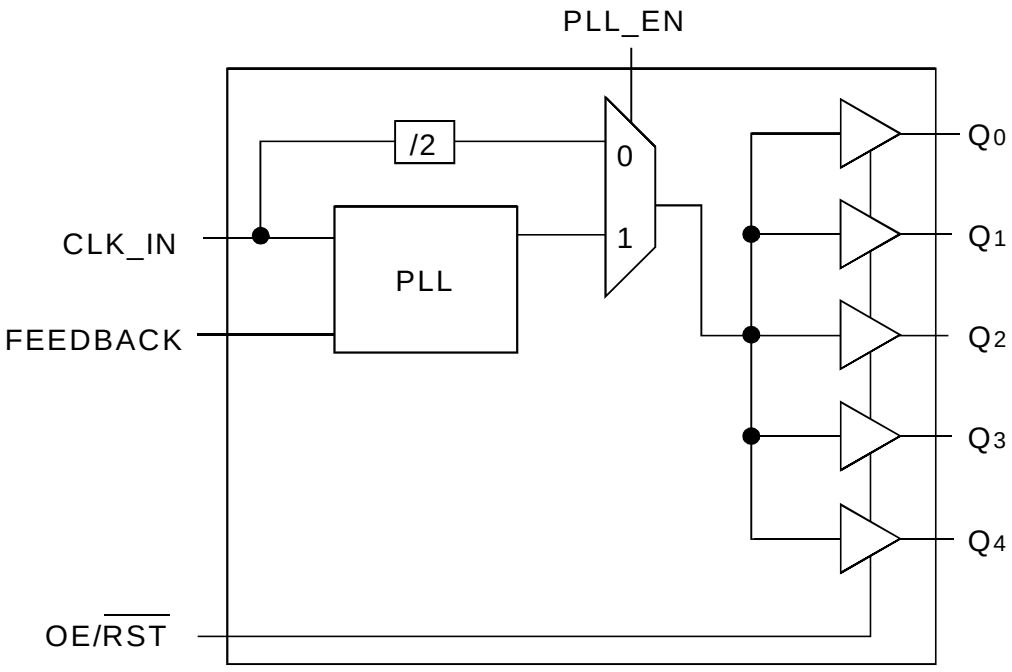
FEATURES:

- 5V operation
- Five low noise CMOS level outputs
- <500ps output skew, Q_0–Q_4
- Outputs 3-state and reset while OE/$\overline{RST}$ low
- PLL disable feature for low frequency testing
- Internal loop filter RC network
- Balanced drive outputs ±36mA
- 80MHz maximum frequency
- Available in QSOP package

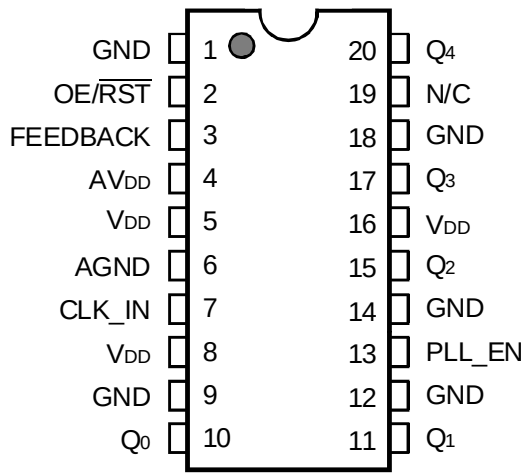
DESCRIPTION

The QS5935 Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to a reference clock input. Five outputs are available: Q_0–Q_4. Careful layout and design ensure <500ps skew between the Q_0–Q_4. The QS5935 includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. The PLL can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The QS5935 is designed for use in cost sensitive high-performance computing systems, workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. In the QSOP package, the QS5935 clock driver represents the best value in small form factor, high-performance clock management products.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Max.	Unit
AV_{DD}, V_{DD}	Supply Voltage to Ground	–0.5 to +7	V
	DC Input Voltage V_{IN}	–0.5 to V_{DD}+0.5	V
	Maximum Power Dissipation (T_A = 85°C)	0.5	W
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = 25° C, f = 1MHz, V_{IN} = 0V) (1)

Pins	Typ.	Max.	Unit
C_{IN}	3	4	pF
C_{OUT}	4	5	pF

NOTE:
1. Capacitance is characterized but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
CLK_IN	I	Reference clock input
FEEDBACK	I	External feedback provides flexibility for different output frequency relationships
Q_0 -Q_4	O	Clock outputs
OE/$\overline{RST}$	I	Output enable/asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled.
PLL_EN	I	When 1, PLL is enabled. When 0, PLL is disabled and the output for Q_0 -Q_4 will be CLK_IN/2 in frequency. This allows the CLK_IN input to be single-stepped for system debug.
V_{DD}	—	Power supply for output buffers
AV_{DD}	—	Power supply for phase lock loop and other internal circuitries
GND	—	Ground supply for output buffers
AGND	—	Ground supply for phase lock loop and other internal circuitries

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, AV_{DD}/V_{DD} = 5.0V ± 10%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	—	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –36mA	V_{DD} – 0.75	—	—	V
		I_{OH} = –100µA	V_{DD} – 0.2	—	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 36mA	—	—	0.45	V
		V_{DD} = Min., I_{OL} = 100µA	—	—	0.2	V
V_H	Input Hysteresis	—	—	100	—	mV
I_{OZ}	Output Leakage Current	V_{OUT} = V_{DD} or GND, V_{DD} = Max., Outputs Disabled	—	—	±5	µA
I_{IN}	Input Leakage Current	V_{IN} = AV_{DD} or GND, AV_{DD} = Max.	—	—	±5	µA

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max., OE/$\overline{RST}$ = LOW, CLK_IN = LOW, All outputs unloaded	—	1	mA
ΔI_{DD}	Power Supply Current per Input HIGH	V_{DD} = Max., V_{IN} = 3.4V	0.7	1.5	mA
I_{DDD}	Dynamic Power Supply Current (1)	V_{DD} = Max., C_L = 0pF	—	0.4	mA/MHz

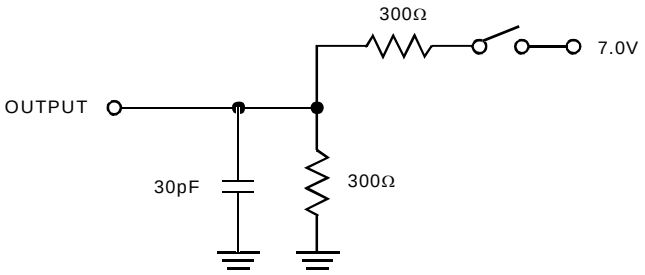
NOTE:
1. This value is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

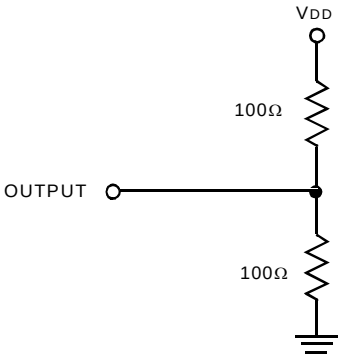
Symbol	Parameter (1)	Min.	Typ.	Max.	Unit
t_{SKR}	Output Skew Between Rising Edges, Q_0-Q_4 (2,3)	—	—	500	ps
t_{SKF}	Output Skew Between Falling Edges, Q_0-Q_4 (2,3)	—	—	500	ps
t_{PW}	Pulse Width, Q_0-Q_4	T_{CYC}/2 – 0.4	—	T_{CYC}/2 + 0.4	ns
t_J	Cycle-to-Cycle Jitter (2,5)	– 0.15	—	+0.15	ns
t_{PD}	CLK_IN to Feedback Delay (2,6)	– 500	—	+500	ps
t_{LOCK}	CLK_IN to Phase Lock	—	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, OE/$\overline{RST}$ LOW to HIGH (4)	0	—	14	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OE/$\overline{RST}$ HIGH to LOW (2,4)	0	—	14	ns
t_R, t_F	Output Rise/Fall Times, 0.2V_{DD} ~ 0.8V_{DD} (2)	—	—	2.5	ns
t_R, t_F	Maximum Rise/Fall Times, 0.8V to 2V	—	—	3	ns
F_I	Input Clock Frequency	10	—	80	MHz
t_{PWC}	Input Clock Pulse, HIGH or LOW (7)	2	—	—	ns
D_H	Duty Cycle, CLK_IN (7)	25	—	75	%

NOTES:
1. See Test Loads and Waveforms for test load and termination.
2. This parameter is guaranteed by characterization but not tested.
3. Skew specifications apply under identical environments (loading, temperature, V_{DD}, device speed grade).
4. Measured in open loop mode PLL_EN = 0.
5. Jitter is characterized using an oscilloscope, Q output at 20MHz. Measurement is taken one cycle after jitter.
6. t_{PD} measured at device inputs at 1.5V, Q output at 80MHz.
7. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

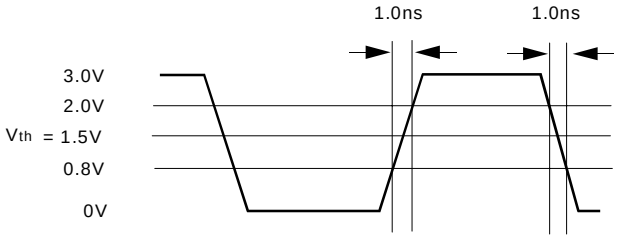
AC TEST LOADS AND WAVEFORMS



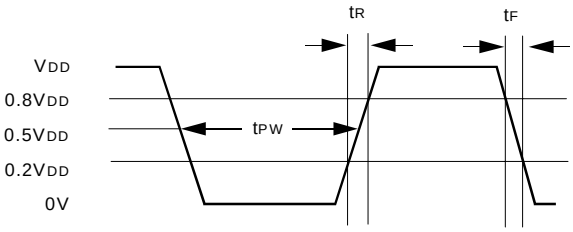
TEST CIRCUIT 1



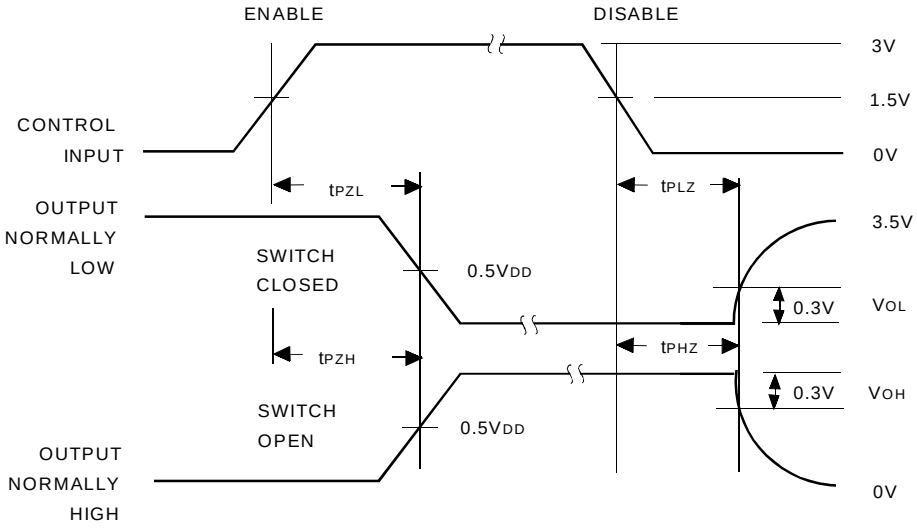
TEST CIRCUIT 2



TTL INPUT TEST WAVEFORM



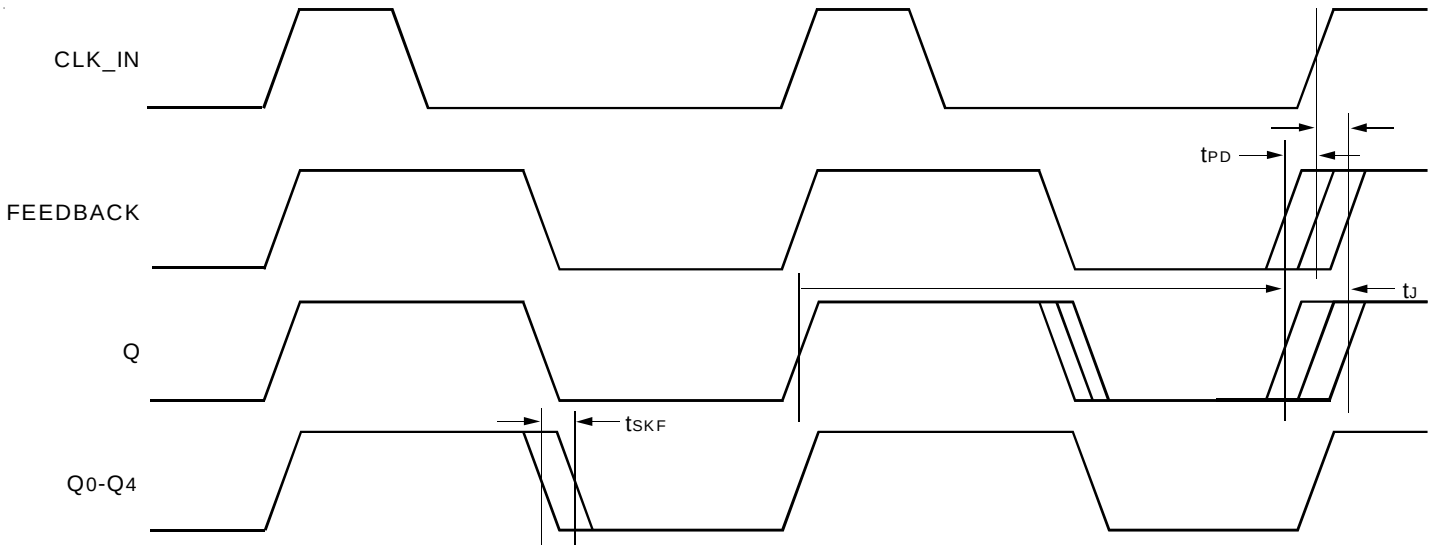
CMOS OUTPUT WAVEFORM



ENABLE AND DISABLE TIMES

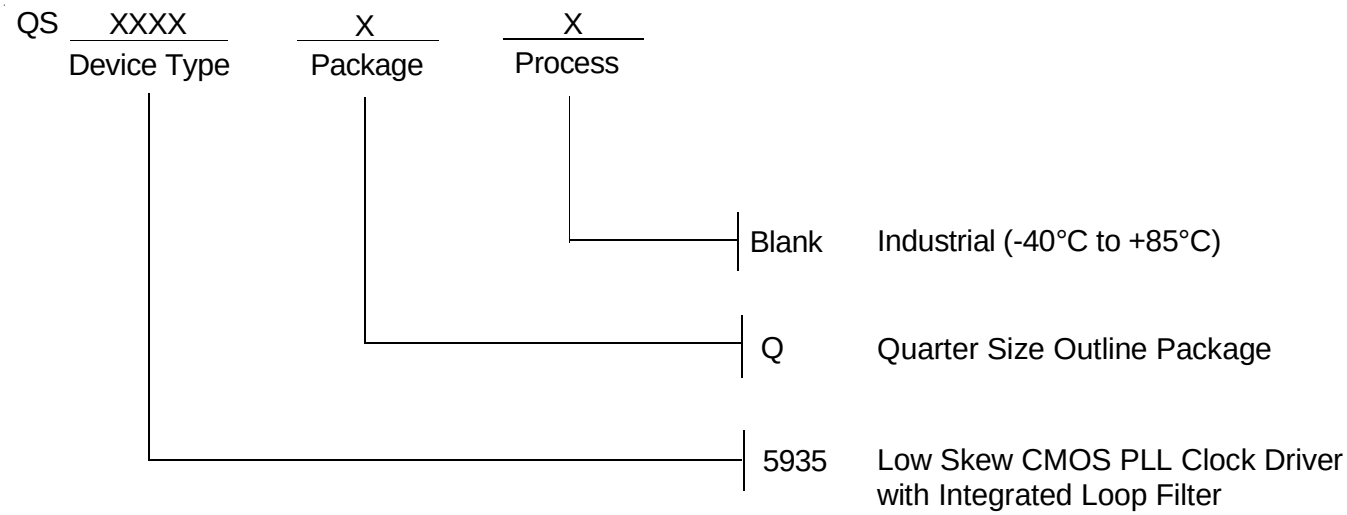
TEST CIRCUIT 1 is used for output enable/disable parameters.
TEST CIRCUIT 2 is used for all other timing parameters.

AC TIMING DIAGRAM



NOTES:
1. AC Timing Diagram applies to Q output connected to FEEDBACK .
2. All parameters are measured at 0.5V_{DD} except for t_{PD}, which is measured at 1.5V

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459