

SED1180F/SED1181F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

DESCRIPTION

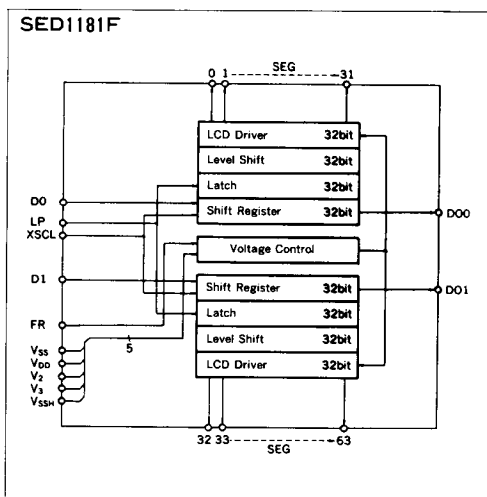
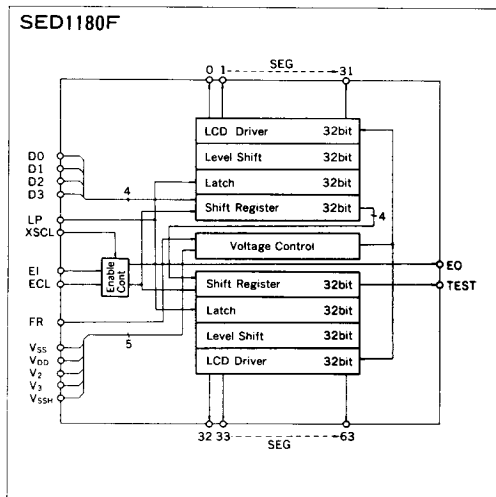
The SED1180F and SED1181F are LCD Segment drivers which are used in conjunction with the SED1190F and SED1191F (LCD common drivers).

They can drive a large dot-matrix LCD display with a duty ratio of 1/64 or higher.

FEATURES

- Display duty 1/64 to 1/128
- 64-bit high voltage resistant output, LCD driver (Segment driver)
- Rightward shift suitable for a 1/64-duty panel
- Allows cascade-connection. Dasy-chain connection of enable pins can be used to minimize power consumption. (SED1180F only)
- Power supply for the logic $-5V \pm 10\%$
- CMOS high-voltage-resistant process 25V (Max)
- SED1180F 4-bit bus data transfer
- SED1181F Independent serial data input for each 32 segment
- Package 80-pin QFP (plastic)

BLOCK DIAGRAM



PIN DESCRIPTION

SED1180F

Pin Name	Functions
SEG0 to 63	Outputs to Segment pins of LCD Output level changes at each latch pulse LP falling-edge.
XSCL	Shift clock for displayed data Falling-edge trigger
LP	Latch pulse for displayed data Falling-edge trigger
FR	LCD display frame signal
EI	Enable input ; enabled on "H", disabled on "L"
ECL	A clock pulse for propagation of enable signals Falling-edge trigger
EO	Enable output In cascade connection, EO of nth driver is connected to EI of (n+1)-th driver.
D0 to D3	4-bit display data input
TEST	Outputs shifted data input from D3
V _{DD} , V _{SS}	Power supply for the logic, V _{DD} : 0V (GND), V _{SS} : -5.0V
V ₂ , V ₃ , V _{SSH}	Power supply for driving LCD, V _{DD} >V ₂ >V ₃ >V _{SSH}

SED1181F

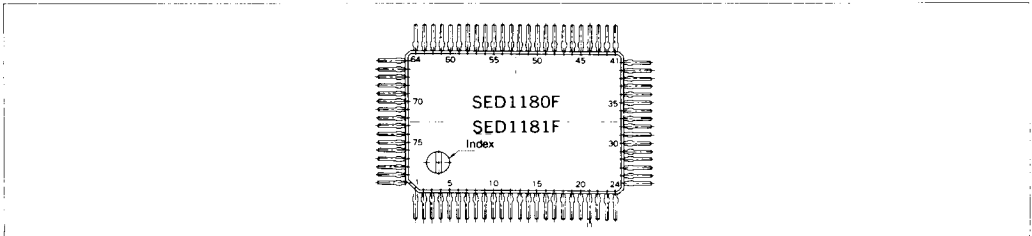
Pin Name	Functions
SEG0 to 63	Outputs to Segment pins of LCD Output level changes at each latch pulse LP falling-edge
XSCL	Shift clock for displayed data Falling-edge trigger
LP	Latch pulse for displayed data Falling-edge trigger
FR	LCD display frame signal
DO0	Outputs serial display data input from D0.
DO1	Outputs serial display data input from D1.
D0, D1	Input 2-bit serial display data (Data read at a XSCL falling-edge)
V _{DD} , V _{SS}	Power supply for the logic, V _{DD} : 0V (GND), V _{SS} : -5.0V
V ₂ , V ₃ , V _{SSH}	Power supply for driving LCD, V _{DD} >V ₂ >V ₃ >V _{SSH}

Note :

D0 : serial display data corresponds to SEG0 to SEG31.

D1 : serial display data corresponds to SEG32 to SEG63.

PIN CONFIGURATION



SED1180F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	V _{SSH}
10	SEG18	30	D3	50	SEG45	70	V ₂
11	SEG17	31	D2	51	SEG46	71	V ₃
12	SEG16	32	D1	52	SEG47	72	V _{SS}
13	SEG15	33	D0	53	SEG48	73	V _{DD}
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

SED1181F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V _{SSH}
10	SEG18	30	NC	50	SEG45	70	V ₂
11	SEG17	31	NC	51	SEG46	71	V ₃
12	SEG16	32	D1	52	SEG47	72	V _{SS}
13	SEG15	33	D0	53	SEG48	73	V _{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ABSOLUTE MAXIMUM RATINGS

(V_{DD} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{SS}	-7.0 to 0.3	V
Supply voltage (2)	V _{SSH} V ₂ , V ₃	-28.0 to 0.3	V
Input voltage	V _I	V _{SS} -0.3 to 0.3	V
Operating temperature	T _{opr}	-20 to 75	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature and time	T _{sol}	260°C · 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD} = 0V, V_{SS} = -5V ± 10%, Ta = -20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Supply voltage (1)	V _{SS}		-5.5	-5.0	-4.5	V	
Supply voltage (2)	V ₂		V _{SSH}		V _{DD}	V	
	V ₃		V _{SSH}		V _{DD}	V	
	V _{SSH}	Recommended V _{SSH}	-25.0		-14.0	V	
		Operable V _{SSH} *	-25.0		-5.0	V	
High level input voltage	V _{IH}		0.2V _{SS}		V _{DD} + 0.3	V	
Low level input voltage	V _{IL}		V _{SS} - 0.3		0.8V _{SS}	V	
High level output voltage	V _{OH}	I _{OH} = -0.6mA	-0.4		—	V	
Low level output voltage	V _{OL}	I _{OL} = 0.6mA	—		V _{SS} + 0.4	V	
Input leak current	I _{LI}	0V ≤ V _I ≤ V _{SS}	—	0.05	2.0	μA	
Output leak current	I _{LO}	0V ≤ V _O ≤ V _{SS}	—	0.05	5.0	μA	
Shift clock	XSCL		—		6.0	MHz	
Frame signal	FR		—	1/60	—	s	
Input capacitance	C _I	T _a = 25°C	—	5.0	8.0	pF	
Segment output on resistance	R _{SEG}	V _{OH} = V _{DD} - 0.5V	V _{SSH} = -20.0V	—	1.9	2.9	kΩ
		V _{OL} = V _{SSH} + 0.5V	V _{SSH} = -14.0V	—	2.4	3.9	
		SEG /bit	V _{SSH} = -9.0V	—	3.6	7.0	
			V _{SSH} = -5.0V	—	11.5	500.0	
Quiescent current	I _Q	V _{SSH} = -25V, V _{SS} = -5.5V V _I = V _{DD}	—	0.05	30	μA	
Operating current for the logic	I _{SSO}	SED 1180 FR cycle = 16.7ms ECL cycle = 13μs V _{SS} = -5.0V V _{IH} = V _{DD} , V _{IL} = V _{SS} LP cycle = 130μs XSCL = 1.5MHz (duty50%)	—	90	200	μA	
		SED 1181 FR cycle = 130μs (duty50%) All data input reversed bit by bit. All output pins are opened.	—	850	1200		
Operating current for LCD	I _{SSHO}	SED 1180 FR cycle = 16.7ms ECL cycle = 13μs V _{SS} = -4.5V, V _I = -4.0V V _I = -16.0V, V _{SW} = -20.0V V _{IH} = V _{DD} , V _{IL} = V _{SS} LP cycle = 130μs XSCL = 1.5MHz (duty50%)	—	40	80	μA	
		SED 1181 FR cycle = 130μs (duty50%) All data input reversed bit by bit. All output pins are opened.	—	70	100		

* Operable V_{SSH} indicates its functionally operable range although the driver output ON resistance becomes higher than with recommended V_{SSH}.

To determine the voltage, we recommend to test the driver with a liquid crystal panel.

●AC Electrical Characteristics

(V_{DD}=0V, V_{SS}= -5.0V ± 10%, T_a= -20 to 75°C)

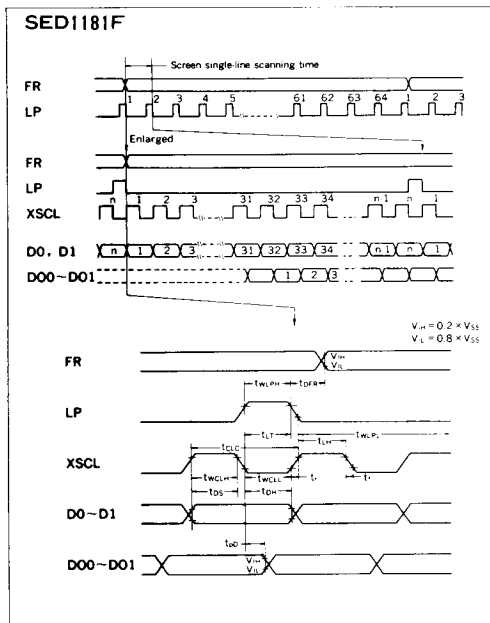
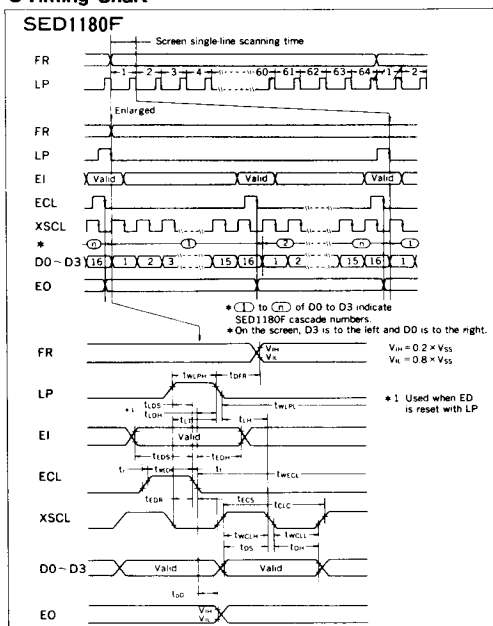
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shift clock cycle	t _{CLC}		166	—	—	ns
Shift clock "H" width	t _{WCLH}		63	—	—	ns
Shift clock "L" width	t _{WCLL}		63	—	—	ns
Data setup time	t _{DS}		50	—	—	ns
Data hold time	t _{DH}		30	—	—	ns
Enable clock "H" width	t _{WECH}	*3	100	—	—	ns
Enable clock "L" width	t _{WECL}	*3	100	—	—	ns
Enable data setup time	t _{EDS}	*3	50	—	—	ns
Enable data hold time	t _{EDH}	*3	20	—	—	ns
Enable clock delay time	t _{EDR}	*3	-10	—	—	ns
Enable clock setup time	t _{ECS}	*3	70	—	—	ns
Latch pulse "H" width	t _{WLPH}	*1	110	—	—	ns
Latch pulse "L" width	t _{WLPL}		220	—	—	ns
Latch timing	t _{LT}		100	—	—	ns
Latch hold time	t _{LH}		0	—	—	ns
Latch pulse data setup time	t _{LDS}	*2, *3	140	—	—	ns
Latch pulse data hold time	t _{L DH}	*2, *3	50	—	—	ns
Permissible frame signal delay	t _{DFR}		-500	—	500	ns
Input signal rise time	t _r		—	—	*4	
Input signal fall time	t _f		—	—	*4	
Enable output delay	t _{PD}	*3	20	—	150	ns
Serial data output delay	t _{PO}		20	—	150	ns

*1 t_{WLPH}=160ns (Min) when LP is used as EI data.*2 t_{WLPH}=250ns (Min) when EO output is reset with LP. (t_r=t_f=25ns)

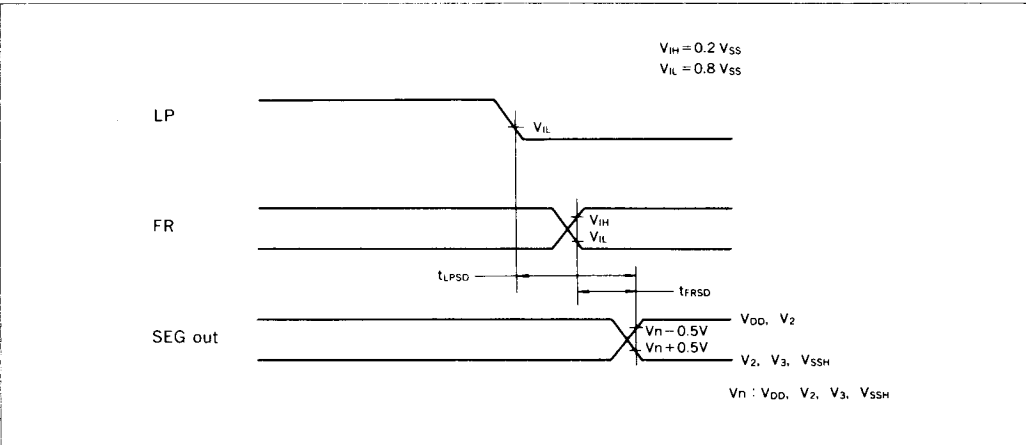
*3 Applicable to SED1180F only.

*4 t_r, t_f < (t_{acc} - t_{wah} - t_{wcll})/2, where t_r, t_f ≤ 50ns.

●Timing Chart



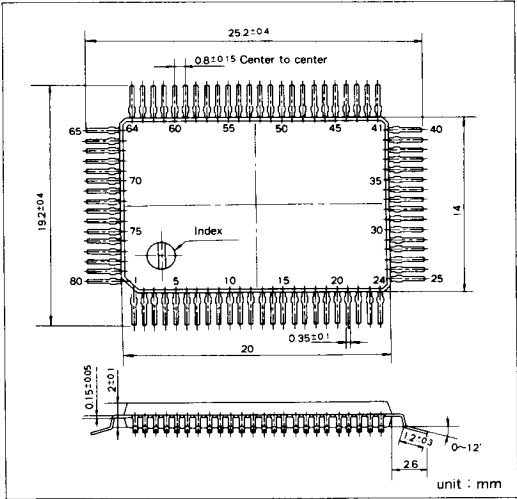
●SEG Output Signal Timing Characteristics



($V_{DD} = 0V$, $V_{SS} = -5V \pm 10\%$, $T_a = -20$ to $75^\circ C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LP-SEG output delay time	t_{LPSD}	$V_{SSH} = -14.0$ to $-25.0V$	—	—	4.5	μs
FR-SEG output delay time	t_{FRSD}	$C_L = 100pF$	—	—	4.5	μs

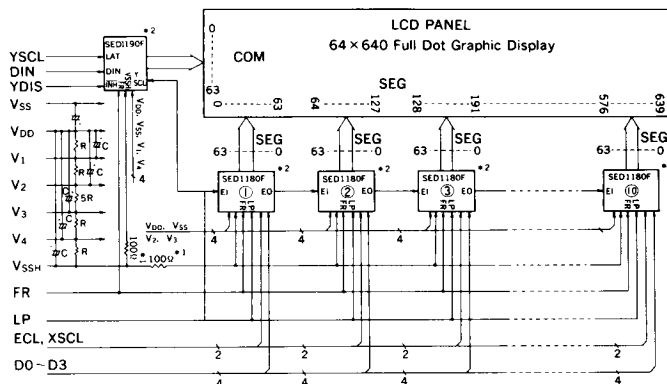
■PACKAGE DIMENSIONS



*Drawing is applicable to SED1180F_{0A}/SED1181F_{0B}.
*SED1180F_{5A}/SED1181F_{5A} are 2.7mm thick.

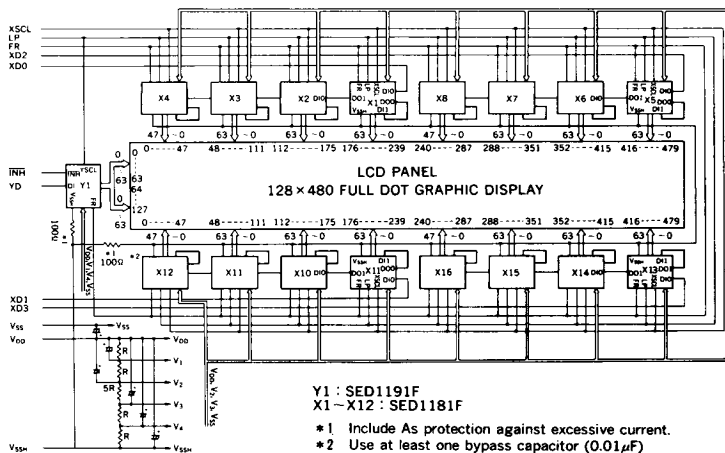
■EXAMPLE OF APPLICATION

SED1180F (64×640 dot, 1/64 duty, 1/9 bias)



- * 1 Use to protect against excessive current.
- * 2 Use at least one bypass capacitor (0.01μF)
Near V_{SS} and V_{SSH} of each driver LSI to improve noise immunity.

SED1181F (128×480 dot, 1/64 duty, 1/9 bias)



Y1: SED1191F
X1-X12: SED1181F

- * 1 Include As protection against excessive current.
- * 2 Use at least one bypass capacitor (0.01μF)
Near V_{SS} and V_{SSH} of each driver LSI to improve noise immunity.