Renesas Technology Releases SuperH Family SH7211F Single-Chip Microcontroller with On-Chip Flash Memory, Achieving World's Top-Level Operating Speed of 160 MHz

— Incorporating high-performance SH-2A CPU core with excellent real-time control capability, enabling implementation of high-quality real-time control devices for industrial equipment field, etc. —

Tokyo, November 15, 2005 — Renesas Technology Corp. today announced the SH7211F single-chip microcontroller with on-chip flash memory, featuring a high-performance SH-2A CPU core with excellent real-time control capability and the world's top-level operating speed of 160 MHz, as an addition to the 32-bit RISC (reduced instruction set computer) microcontroller SuperH™(*1) Family. Sample shipments will begin in January 2006 in Japan.

In addition to high-speed operation with large-capacity on-chip flash memory, the SH7211F features a comprehensive set of peripheral functions, such as 12-bit A/D converters and multifunction timer unit, suitable for device control integrated in a single chip, making it ideal for use in applications such as industrial devices requiring advanced real-time control, including AC servos and inverters and so forth.

Features of the SH7211F are as follows.

(1) Fast 160 MHz operation achieved through use of proprietary flash memory and circuit technologies

The SH7211F incorporates 512-Kbyte large-capacity flash memory. While logic circuitry such as the CPU core is capable of fast 160 MHz operation, in general the operating speed of flash memory is theoretically slower than that of the logic circuitry, and is difficult to increase. However, through the use of proprietary Renesas Technology flash memory technology based on accumulated know-how, and new circuit techniques for the flash memory cache circuitry and so forth, the SH7211F achieves virtually the same performance as when single-cycle access is performed at 160 MHz.

(2) Use of SH-2A CPU core offering greatly improved performance compared with Renesas Technology's previous SH-2

The SH-2A CPU core employs a superscalar architecture enabling simultaneous execution of two instructions, together with a Harvard architecture, improving performance by a factor of 1.5 or more compared with Renesas Technology's previous SH-2 CPU core at the same frequency.

Real-time control performance has also been greatly improved, providing high-quality real-time processing. In addition, ROM code efficiency has been improved by approximately 25% compared with the SH-2, enabling an approximately 25% reduction in program size.

(3) Comprehensive on-chip peripheral functions including a multifunction timer unit suited to industrial applications

The SH7211F incorporates a comprehensive set of peripheral functions suitable for industrial applications. Among these are two MTU2 (Multifunction Timer Unit 2)*2 units with AC servo and suchlike control capability, enabling two motors to be controlled simultaneously, a 12-bit A/D converter and 8-bit D/A converter useful for various kinds of industrial applications, and a variety of communication functions including a serial communication interface with 16-stage FIFO and an I^2C bus*3 interface. This rich selection of peripheral functions makes it possible to implement functionally advanced systems while reducing the number of external parts used and making end-products smaller and lower cost.

< Product Background >

With the increased precision and speed of device control in the field of industrial devices such as AC servos and general-purpose inverters requiring real-time control, features being demanded of control microcontrollers include higher processing performance, on-chip software leakage protection, and the large-capacity on-chip flash memory from the standpoints of, improved development efficiency. At the same time, there is a need to provide a wide variety of peripheral functions in a single chip in order to reduce board size and cost by cutting down on the number of system parts used.

Renesas Technology mass-produces products incorporating the 32-bit SH-2 CPU core for device control for use in industrial, OA, and consumer applications. Market demands for still higher performance were met with the development of the SH-2A CPU core maintaining upward instruction compatibility with the SH-2 while offering higher processing performance and ROM code efficiency, and the release of the well-received ROM-less SH7206. This has now been followed by the development of the SH7211F as the initial product featuring a high-performance SH-2A CPU core and on-chip flash memory.

< Additional Product Details >

The SH7211F incorporates a high-performance SH-2A CPU core offering excellent real-time control capability, and achieves high processing performance of approximately 320 MIPS (million instructions per second) at 160 MHz operation. Processing performance has been improved approximately 1.5-fold compared with the SH-2 CPU core at the same operating frequency, and approximately 3-fold compared with performance at the 80 MHz maximum operating frequency of SH-2 equipped products. Upward instruction set compatibility enables existing programs to be used, while an approximately 25% increase in ROM code efficiency allows program storage memory capacity to be reduced.

The SH-2A CPU core also offers improved real-time capability. Fifteen register banks specifically for interrupt use are provided in the CPU, and the response cycle until interrupt handling has been reduced from 37 cycles with the SH-2 to 6 cycles with the SH-2A. With a higher operating frequency and shorter response cycle, the program initiation response time with respect to an interrupt signal in SH-2A 160 MHz operation has been cut to approximately 1/12 of the response time in SH-2 80 MHz operation. This allows fast program switching when an interrupt event occurs, providing high-quality real-time control.

The SH7211F also includes a variety of peripheral functions suited to high-end industrial devices with an emphasis on real-time control capability, such as AC servos and inverters. Functions ideal for motor control use include an MTU2 and MTU2S with 3-phase PWM (pulse width modulation) output capability for inverter device use, eight 12-bit A/D converter channels, and two 8-bit D/A converter channels. Communication functions comprise an I^2C bus interface channel and a 4-channel serial communication interface with 16-stage FIFO, facilitating communication with peripheral devices. The external data bus can support flash ROM, SRAM, SDRAM, burst ROM, multiplex I/O, and so forth by means of bus state controller settings, enabling various kinds of memory to be connected directly without the use of external parts.

This comprehensive set of peripheral functions makes it possible to use fewer external parts and create functionally advanced products while cutting costs.

The package used is a 144-pin LQFP (20 mm × 20 mm).

On-chip debugging functions*[4] are included that enable real-time debugging at the maximum operating frequency. Supported development environments are the USB bus-powered E10A-USB requiring no external power supply, and the E200F providing faster emulation capability, allowing real-time tracing to be carried out at the maximum operating frequency.

Renesas Technology will continue to extend the product lineup in line with evolving market needs, with the development of faster and more powerful models featuring higher operating frequencies, increased on-chip flash memory and RAM capacities, and enhanced peripheral functions. The development of SoC (System on Chip) and SiP (System in Package) products using the SH-2A is also planned.

Renesas Technology plans to exhibit the SH7211F at "Embedded Technology 2005" being held at Pacifico Yokohama from November 16 to 18, 2005.

<Notes>

Notes: 1. SuperH is a trademark of Renesas Technology Corp.

2. MTU2 (Multi Function Timer Pulse Unit 2): A multifunction timer comprising six 16-bit timer counter channels, with maximum 16 pulse input/output and three pulse input capability

3. I^2C bus (Inter IC Bus) is an interface specification proposed by Royal Philips Electronics of the Netherlands.

4. On-chip debugging functions: Part of the debugging circuitry previously incorporated in an emulator. Providing these functions on-chip enables simple emulation to be carried out using an actual device during system evaluation.

* Other product names, company names, or brands mentioned are the property of their respective owners.

< Typical Applications >

- Industrial equipment: AC servos, inverters, vending machines, etc.

< Prices in Japan >* For Reference

Product Name	Package	Sample Price [Tax Included] (Yen)
SH7211F (R5F72115)	144-pin LQFP (20 mm × 20 mm)	2,300

< **Specifications** >

Item	**SH7211F Specifications**
Product name	R5F72115
Power supply voltage	1.5 V (internal)/3.3 V (external)
Maximum operating frequency	160 MHz
Maximum processing performance	320 MIPS (at 160 MHz operation)
CPU core	SH-2A (no FPU)
CPU instructions	91 (excluding FPU-related instructions)
On-chip RAM	32 Kbytes
External memory	Bus clock frequency: Maximum 40 MHz
	SRAM, SDRAM, burst ROM directly connectable by bus state controller
	Address space: 64 Mbytes × 8
	Provision for idle cycle insertion to prevent bus collisions
	Data bus width: External 8/16 bits
On-chip peripheral functions	Multifunction timer pulse unit 2 (MTU2)
	Multifunction timer pulse unit 2S (MTU2S)
	A/D converter (12-bit resolution) × 8 channels
	D/A converter (8-bit resolution) × 2 channels
	Serial communication interface with FIFO (SCIF) × 4 channels (asynchronous and clock synchronous serial communication capability)
	I^2C bus interface* × 1 channel
	Compare match timer (CMT) × 2 channels
	User break controller (UBC)
	On-chip debugging functions • Advanced user debugger (AUD) • User debug interface (H-UDI)
	Direct memory access controller (DMAC) × 8 channels
	Interrupt controller (INTC)
	Watchdog timer (WDT)
	Clock pulse generator (CPG): Built-in multiplication PLL
Power-down modes	Sleep mode
	Software standby mode
	Module standby mode
Package	144-pin LQFP (20 mm × 20 mm)

* I^2C bus (Inter IC Bus) is an interface specification proposed by Royal Philips Electronics of the Netherlands.

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.

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