Time-Code Receiver with A/D Converter

Description

The U4223B is a bipolar integrated straight-through receiver circuit in the frequency range of 40 kHz to 80 kHz. The device is designed for radio-controlled clock applications.

Features

- Very low power consumption
- Very high sensitivity
- High selectivity by using two crystal filters
- Power-down mode available
- Only a few external components necessary
- 4-bit digital output
- AGC hold mode

Block Diagram

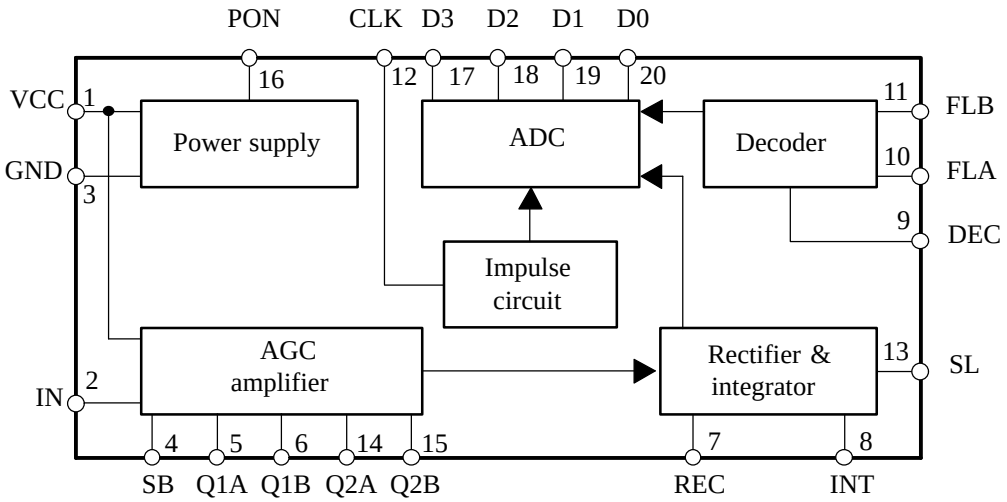


Figure 1. Block diagram

Ordering and Package Information

Extended Type Number	Package	Remarks
U4223B-MFS	SSO20 plastic	
U4223B-MFSG3	SSO20 plastic	Taping according to IEC-286-3
T4223B-MF	No	Die on foil
T4223B-MC	No	Die on carrier

Pin Description

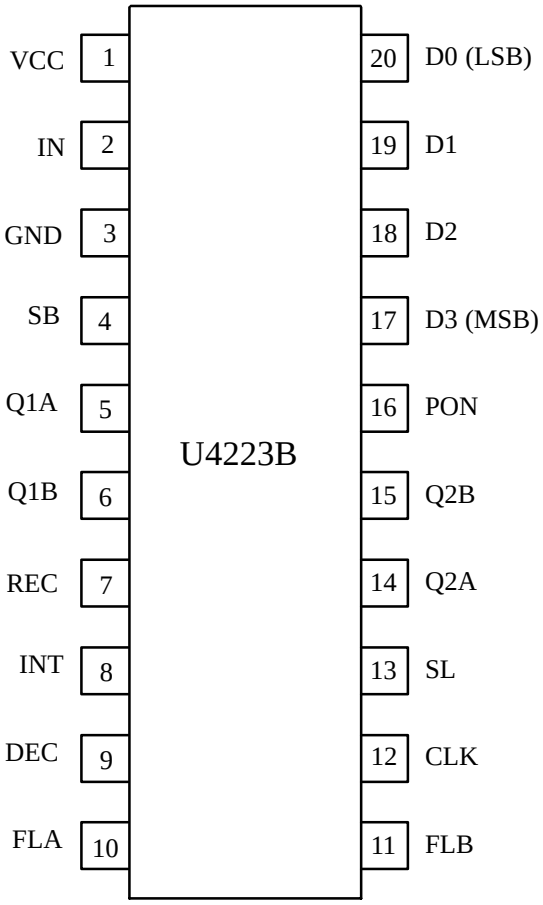


Figure 2. Pinning

Pin	Symbol	Function
1	VCC	Supply voltage
2	IN	Amplifier – Input
3	GND	Ground
4	SB	Bandwidth control
5	Q1A	Crystal filter 1
6	Q1B	Crystal filter 1
7	REC	Rectifier output
8	INT	Integrator output
9	DEC	Decoder input
10	FLA	Lowpass filter
11	FLB	Lowpass filter
12	CLK	Clock input for ADC
13	SL	AGC hold mode
14	Q2A	Crystal filter 2
15	Q2B	Crystal filter 2
16	PON	Power ON/OFF control
17	D3	Data out MSB
18	D2	Data out
19	D1	Data out
20	D0	Data out LSB

IN

A ferrite antenna is connected between IN and VCC. For high sensitivity, the Q factor of the antenna circuit should be as high as possible. Please note that a high Q factor requires temperature compensation of the resonant frequency in most cases. Specifications are valid for Q>30. An optimal signal-to-noise ratio will be achieved by a resonant resistance of 50 to 200 kΩ.

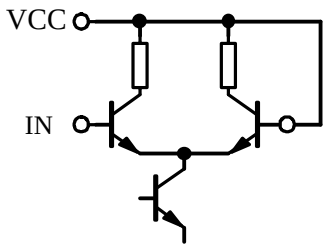


Figure 3.

SB

A resistor R_{SB} is connected between SB and GND. It controls the bandwidth of the crystal filters. It is recommended: R_{SB} = 0 Ω for DCF 77.5 kHz, R_{SB} = 10 kΩ for 60 kHz WWVB and R_{SB} = open for JG2AS 40 kHz.

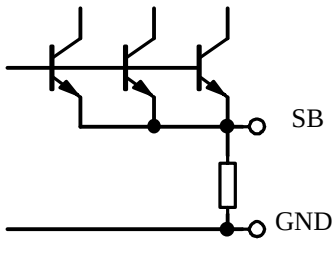


Figure 4.

Q1A, Q1B

In order to achieve a high selectivity, a crystal is connected between the Pins Q1A and Q1B. It is used with the serial resonant frequency of the time-code transmitter (e.g., 60 kHz WWVB, 77.5 kHz DCF or 40 kHz JG2AS).

The equivalent parallel capacitor of the filter crystal is internally compensated. The compensated value is about 0.7 pF. If full sensitivity and selectivity are not needed, the crystal filter can be substituted by a capacitor of 82 pF.

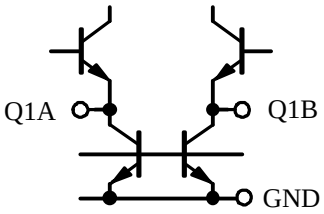


Figure 5.

REC

Rectifier output and integrator input: The capacitor C_1 between REC and INT is the lowpass filter of the rectifier and at the same time a damping element of the gain control.

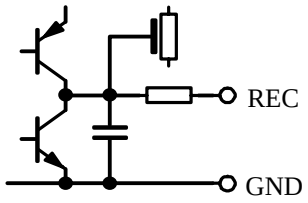


Figure 6.

DEC

Decoder input: Senses the current through the integration capacitor C_2. The dynamic input resistance has a value of about 420 kΩ and is low compared to the impedance of C_2.

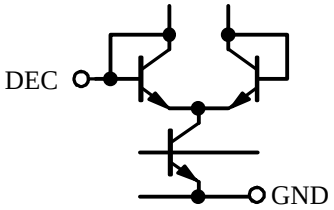


Figure 7.

SL

AGC hold mode: SL high ($V_{SL} = V_{CC}$) sets normal function, SL low ($V_{SL} = 0$) disconnects the rectifier and holds the voltage V_{INT} at the integrator output and also the AGC amplifier gain.

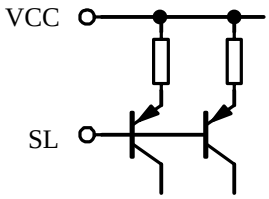


Figure 8.

INT

Integrator output: The voltage V_{INT} is the control voltage for the AGC. The capacitor C_2 between INT and DEC defines the time constant of the integrator. The current through the capacitor is the input signal of the decoder.

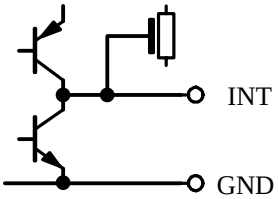


Figure 9.

FLA, FLB

Lowpass filter: A capacitor C_3 connected between FLA and FLB suppresses higher frequencies at the trigger circuit of the decoder.

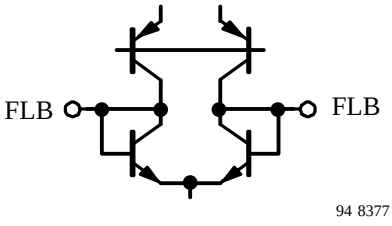


Figure 10.

Q2A, Q2B

According to Q1A/Q1B, a crystal is connected between the Pins Q2A and Q2B. It is used with the serial resonant frequency of the time-code transmitter (e.g., 60 kHz WWVB, 77.5 kHz DCF or 40 kHz JG2AS). The equivalent parallel capacitor of the filter crystal is internally compensated. The value of the compensation is about 0.7 pF.

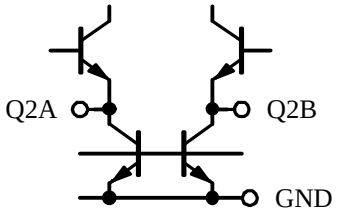


Figure 11.

PON

If PON is connected to GND, the receiver will be activated. The set-up time is typically 0.5 s after applying GND at this pin. If PON is connected to VCC, the receiver will switch to power-down mode.

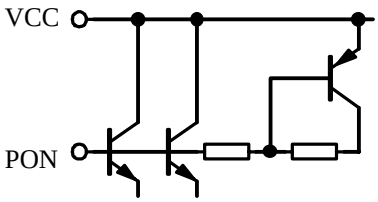


Figure 12.

D0, D1, D2, D3

The outputs of the ADC consist of PNP-NPN push-pull stages and can be directly connected to a microcomputer. In order to avoid any interference of the output into the antenna circuit, we recommend terminating each digital output with a capacitor of 10 nF. The digitalized signal of the ADC is Gray coded (see table). It should be taken into account that in power-down mode (PON = high), D0, D1, D2 and D3 will be high.

A sequence of the digitalized time-code signal can be analyzed by a special noise-suppressing algorithm in order to increase the sensitivity and the signal-to-noise ratio (more than 10 dB compared to conventional decoding). Details about the time-code format are described separately.

Decimal	Gray
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111
11	1110
12	1010
13	1011
14	1001
15	1000

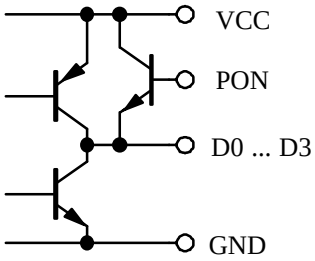


Figure 13.

CLK

The input of the ADC is switched to the AGC voltage by the rising slope of the clock. When conversion time has passed (about 1.8 ms at 25°C), the digitalized field-strength signal is stored in the output registers D0 to D3 as long as the clock is high and can be read by a microcomputer. The falling slope of the clock switches the input of the ADC to the time-code signal. In the meantime, the digitalized time-code signal is stored in the output registers D0 to D3 as long as the clock is low (see figure 14).

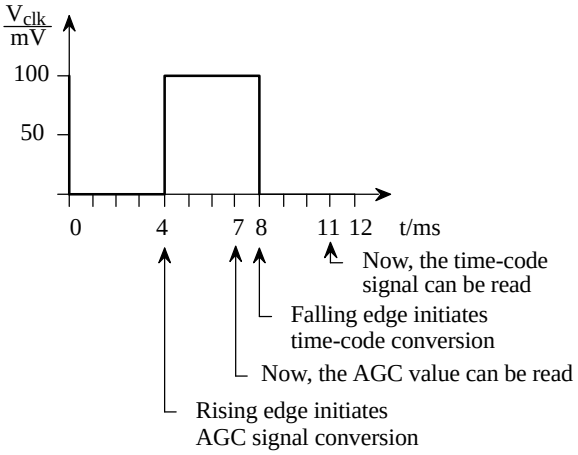


Figure 14.

In order to minimize interferences, we recommend a voltage swing of about 100 mV. A full supply-voltage swing is possible but reduces the sensitivity.

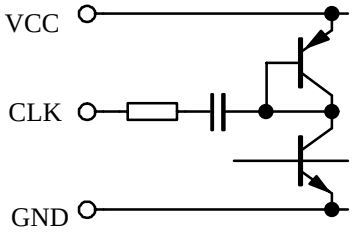


Figure 15.

Please note:
The signals and voltages at the Pins REC, INT, FLA, FLB, Q1A, Q1B, Q2A and Q2B cannot be measured by standard measurement equipment due to very high internal impedances. For the same reason, the PCB should be protected against surface humidity.

Design Hints for the Ferrite Antenna

The bar antenna is a very critical device of the complete clock receiver. Observing some basic RF design rules helps to avoid possible problems. The IC requires a resonant resistance of 50 kΩ to 200 kΩ. This can be achieved by a variation of the L/C-relation in the antenna circuit. It is not easy to measure such high resistances in the RF region. A more convenient way is to distinguish between the different bandwidths of the antenna circuit and to calculate the resonant resistance afterwards.

Thus, the first step in designing the antenna circuit is to measure the bandwidth. Figure 17 shows an example for the test circuit. The RF signal is coupled into the bar antenna by inductive means, e.g., a wire loop. It can be measured by a simple oscilloscope using the 10:1 probe. The input capacitance of the probe, typically about 10 pF, should be taken into consideration. By varying the frequency of the signal generator, the resonant frequency can be determined.

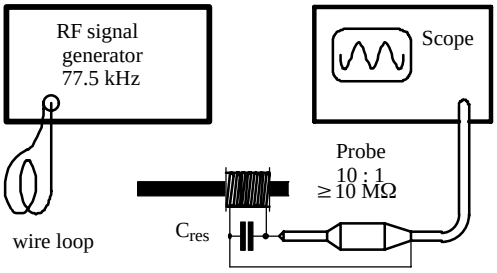


Figure 16.

At the point where the voltage of the RF signal at the probe drops by 3 dB, the two frequencies can then be measured. The difference between these two frequencies is called the bandwidth BW_A of the antenna circuit. As the value of the capacitor C_{res} in the antenna circuit is known, it is easy to compute the resonant resistance according to the following formula:

$$R_{res} = \frac{1}{2 \times \pi \times BW_A \times C_{res}}$$

where
R_{res} is the resonant resistance,
BW_A is the measured bandwidth (in Hz)
C_{res} is the value of the capacitor in the antenna circuit (in Farad).

If high inductance values and low capacitor values are used, the additional parasitic capacitances of the coil ($\leq$ 20 pF) must be considered. The Q value of the capacitor should be no problem if a high Q type is used. The Q value of the coil differs more or less from the DC resistance of the wire. Skin effects can be observed but do not dominate.

Therefore, it should not be a problem to achieve the recommended values of the resonant resistance. The use of thicker wire increases the Q value and accordingly reduces bandwidth. This is advantageous in order to improve reception in noisy areas. On the other hand, temperature compensation of the resonant frequency might become a problem if the bandwidth of the antenna circuit is low compared to the temperature variation of the resonant frequency. Of course, the Q value can also be reduced by a parallel resistor.

Temperature compensation of the resonant frequency is a must if the clock is used at different temperatures. Please ask your supplier of bar antenna material and of capacitors for specified values of the temperature coefficient.

Furthermore, some critical parasitics have to be considered. These are shortened loops (e.g., in the ground line of the PCB board) close to the antenna and undesired loops in the antenna circuit. Shortened loops decrease the Q value of the circuit. They have the same effect like conducting plates close to the antenna. To avoid undesired loops in the antenna circuit, it is recommended to mount the capacitor C_{res} as close as possible to the antenna coil or to use a twisted wire for the antenna-coil connection. This twisted line is also necessary to reduce feedback of noise from the microprocessor to the IC input. Long connection lines must be shielded.

A final adjustment of the time-code receiver can be carried out by pushing the coil along the bar antenna. The maximum of the integrator output voltage V_{INT} at Pin INT indicates the resonant point. But attention: The load current should not exceed 1 nA, that means an input resistance $\geq$ 1 GΩ of the measuring device is required. Therefore, a special DVM or an isolation amplifier is necessary.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{CC}	5.25	V
Ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	R_{stg}	–40 to +85	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883 D), except Pins 2, 5, 6, 14 and 15	$\pm V_{ESD}$	2000	V

Thermal Resistance

Parameters	Symbol	Maximum	Unit
Thermal resistance	R_{thJA}	70	K/W

Electrical Characteristics

V_{CC} = 3 V, reference point Pin 3, input signal frequency 80 kHz, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pin	Symbol	Min	Typ	Max	Unit
Supply voltage range	Pin 1	V_{CC}	1.2		5.25	V
Supply current	Pin 1 Without reception signal with reception signal = 200 µV OFF mode	I_{CC}		 15	 30 25 0.1	 µA µA µA
Set-up time after V_{CC} ON	V_{CC} = 1.5 V	t		2		s
AGC amplifier input; IN Pin 2						
Reception frequency range		f_{in}	40		80	kHz
Minimum input voltage	R_{res} = 100 kΩ, Q_{res} > 30	V_{in}		1	1.5	µV
Maximum input voltage		V_{in}	40	80		mV
Input capacitance to GND		C_{in}		1.5		pF

Parameters	Test Conditions / Pin	Symbol	Min	Typ	Max	Unit
ADC; D0, D1, D2, D3 Pins 17, 18, 19 and 20						
Output voltage HIGH LOW	R_{LOAD} = 870 kΩ to GND R_{LOAD} = 650 kΩ to VCC	V_{OH} V_{OL}	V_{CC}-0.4		 0.4	V V
Output current HIGH LOW	$V_{TCO} = V_{CC}/2$ $V_{TCO} = V_{CC}/2$	I_{SOURCE} I_{SINK}	3 4	10 12		µA µA
Input current into DEC (first bit)	Falling slope of CLK	I_{decs}	–24	–17	–11	nA
Input current into DEC (last bit)	Falling slope of CLK	I_{dece}	28	35	42	nA
Input current into DEC (step range)	Falling slope of CLK	I_{decst}	1.75	3.5	7	nA
Input voltage at IN (first bit)	RF generator at IN, without modulation rising slope of CLK	V_{min}		–10		dBµV
Input voltage at IN (last bit)	RF generator at IN, without modulation rising slope of CLK	V_{max}		75		dBµV
Input voltage at IN (step range)	RF generator at IN, without modulation rising slope of CLK	V_{step}		5.5		dBµV
Clock input; CLK Pin 12						
Input voltage swing		V_{swing}	50	100	V_{CC}	mV
Clock frequency		f_{clk}		100	125	Hz
Dynamical input resistance		$R_{dyn.}$		100		kΩ
Power-ON/OFF control; PON Pin 16						
Input voltage HIGH LOW	Required $I_{IN} \geqq 0.5$ µA		V_{CC}-0.2		 V_{CC}-1.2	V V
Input current	V_{CC} = 3 V V_{CC} = 1.5 V V_{CC} = 5 V	I_{IN}	1.4	1.7 0.7 3	2	µA µA µA
Set-up time after PON		t		0.5	2	s
AGC hold mode; SL Pin 13						
Input voltage HIGH LOW	Required $I_{IN} \geqq 0.5$ µA		V_{CC}-0.2		 V_{CC}-1.2	V V
Input current	$V_{in} = V_{CC}$ V_{in} = GND			 2.5	0.1	µA µA
Rejection of interference signals	$\lvert f_d - f_{ud} \rvert$ = 625 Hz V_d = 3 µV, f_d = 77.5 kHz using 2 crystal filters using 1 crystal filter	 a_f a_f		 43 22		 dB dB

Test Circuit (for Fundamental Function)

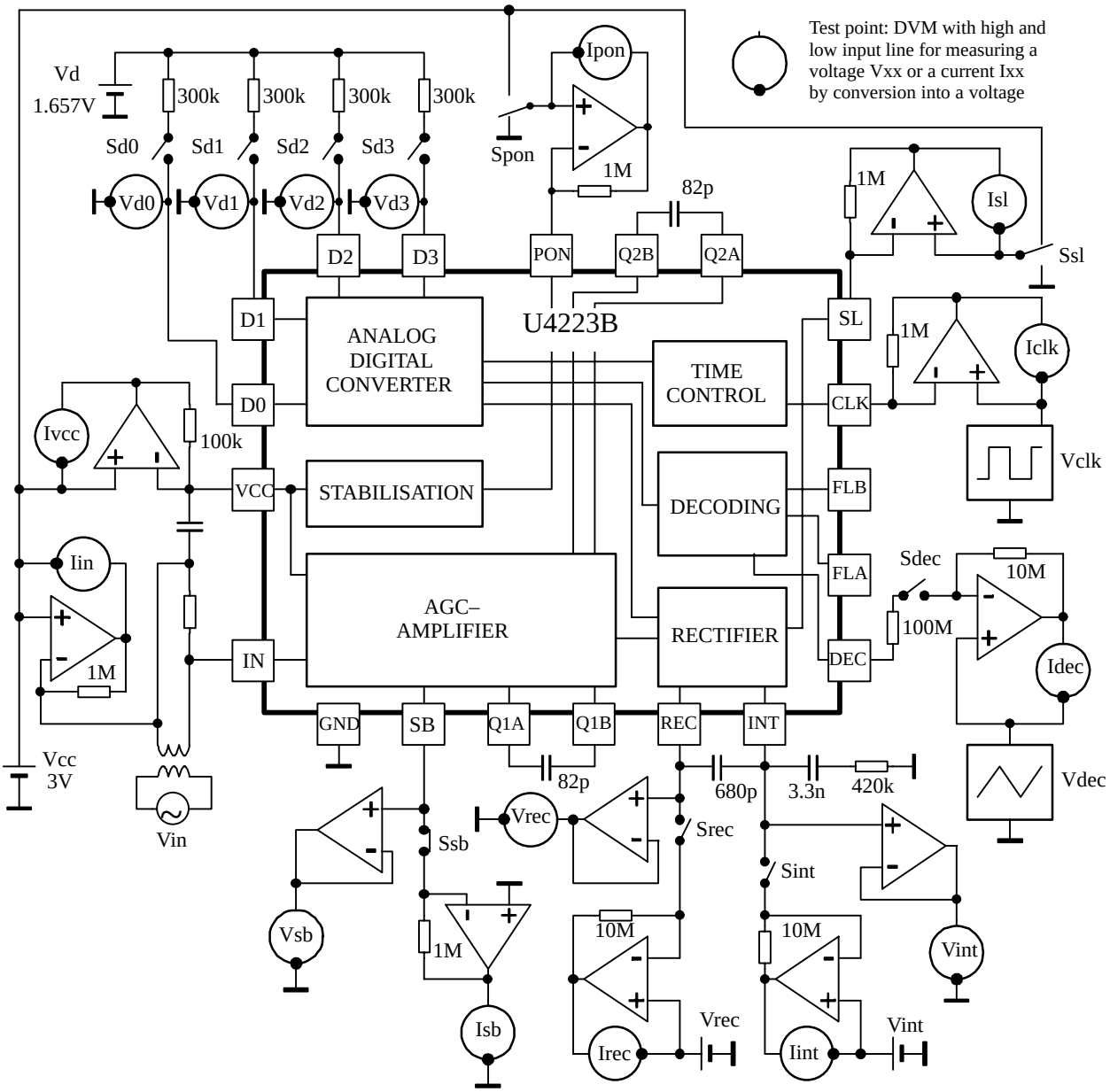


Figure 17. Test circuit

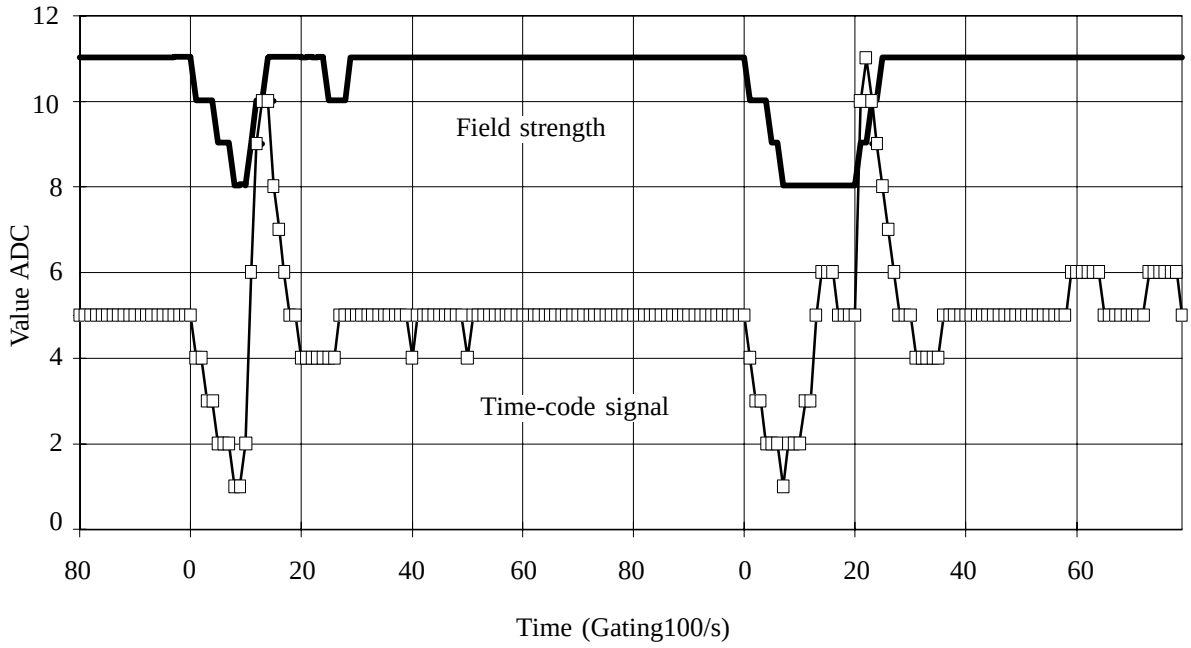


Figure 18. Example of a normal DCF signal

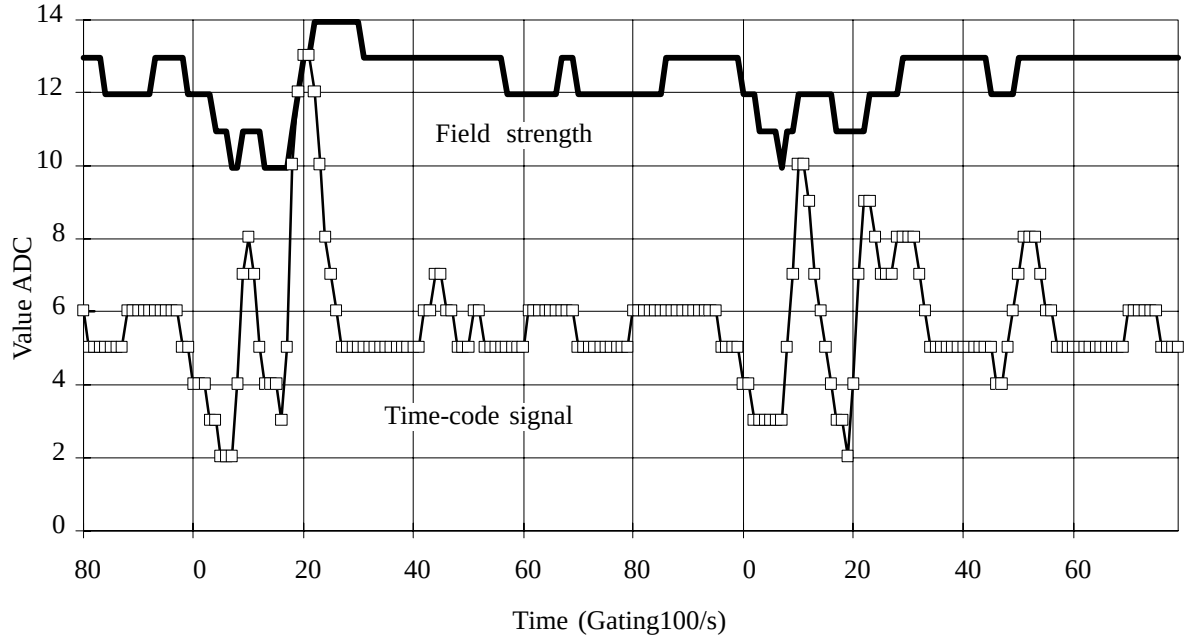


Figure 19. Example of a disturbed DCF signal

Application Circuit for DCF 77.5 kHz

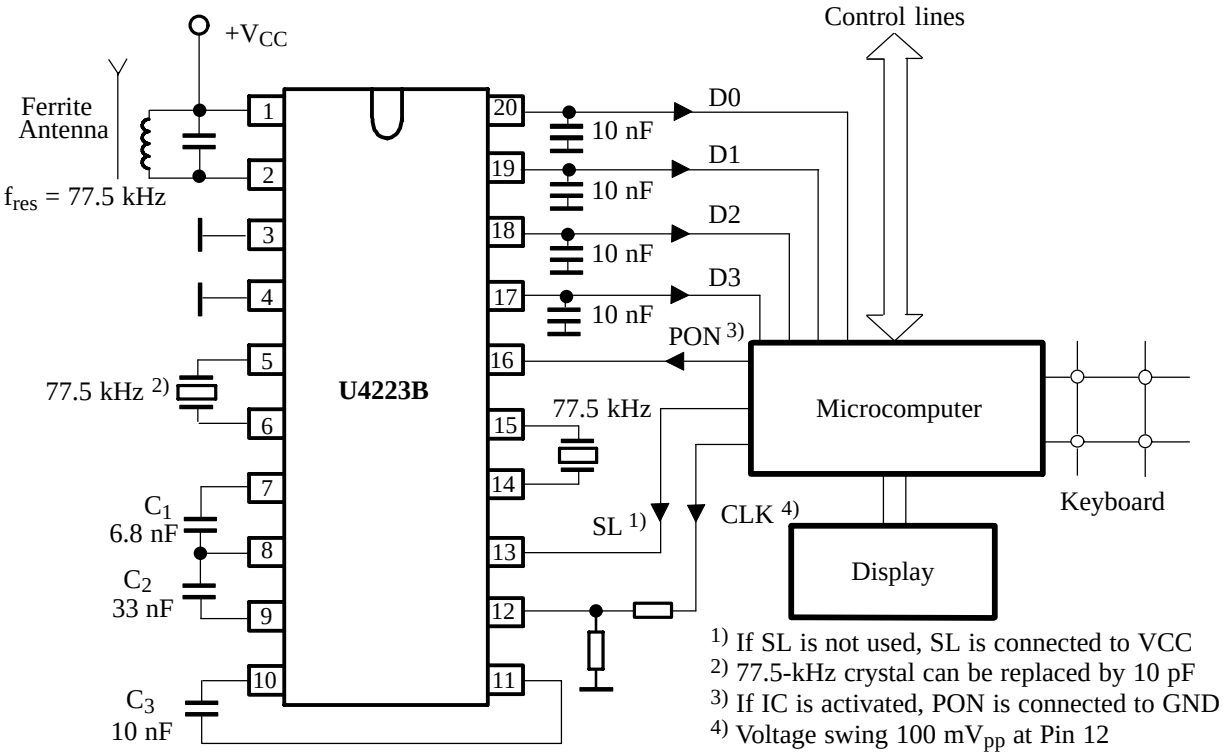


Figure 20.

Application Circuit for WWVB 60 kHz

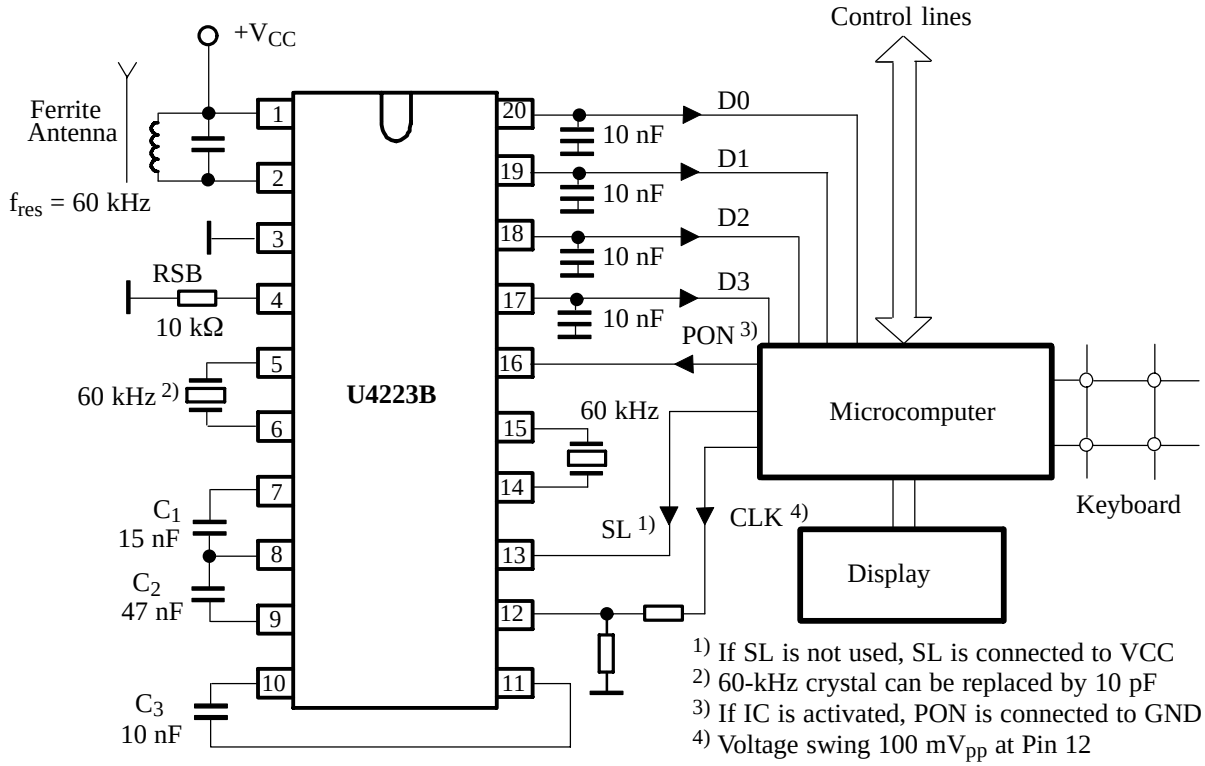


Figure 21.

Application Circuit for JG2AS 40 kHz

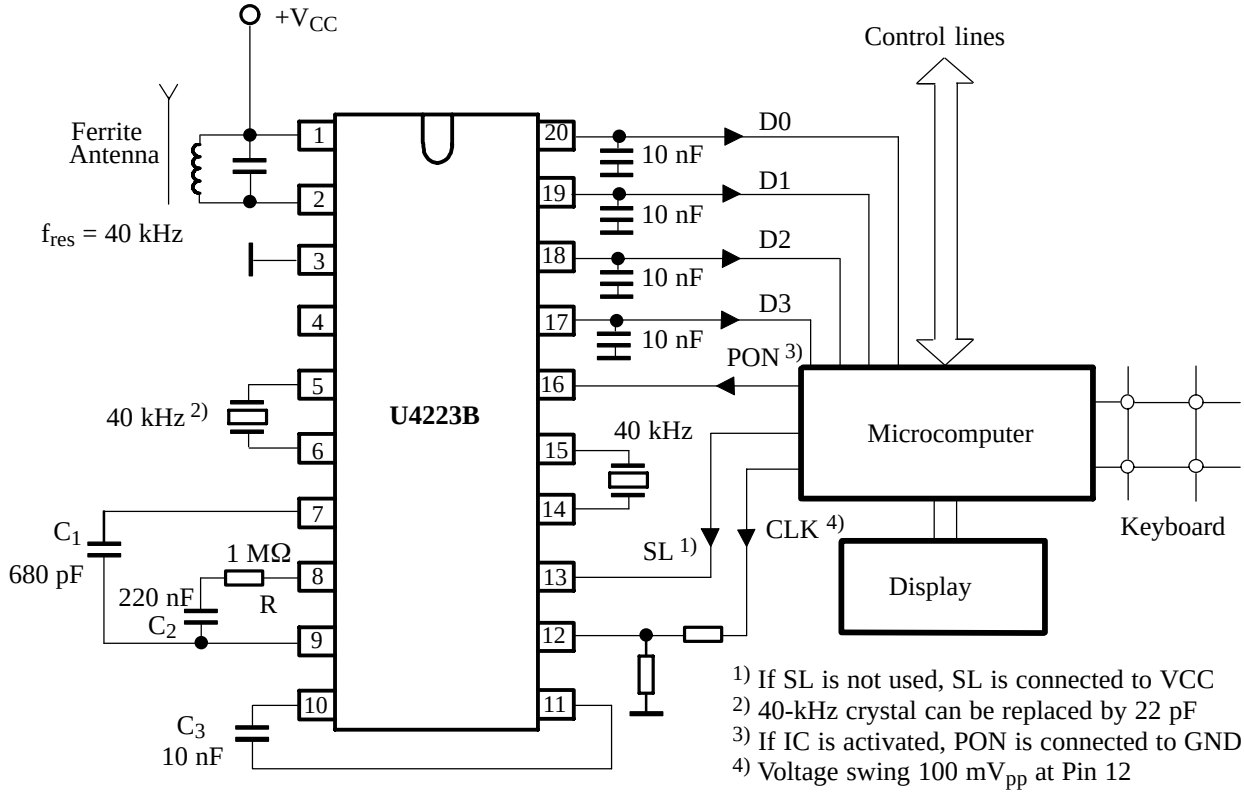


Figure 22.

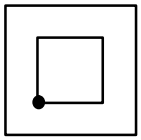
PAD Coordinates

The T4223B is also available as die for “chip-on-board” mounting.
DIE size: 2.26 x 2.09 mm
PAD size: 100 x 100 µm (contact window 88 x 88 µm)
Thickness: 300 µm ± 20 µm

SYMBOL	X-Axis/µm	Y-Axis/µm
IN1	128	832
IN	128	310
GND	354	124
SB	698	128
Q1A	1040	128
Q1B	1290	128
REC	1528	128
INT	1766	128
DEC	2044	268
FLA	2044	676
FLB	2044	1072

SYMBOL	X-Axis/µm	Y-Axis/µm
CLK	2044	1400
SL	2044	1638
Q2A	2000	1876
Q2B	1634	1876
PON	1322	1876
TCO	1008	1876
D3	696	1876
D2	384	1876
D1	128	1682
D0	128	1454
VCC	128	1138

The PAD coordinates are referred to the left bottom point of the contact window.



PAD Layout

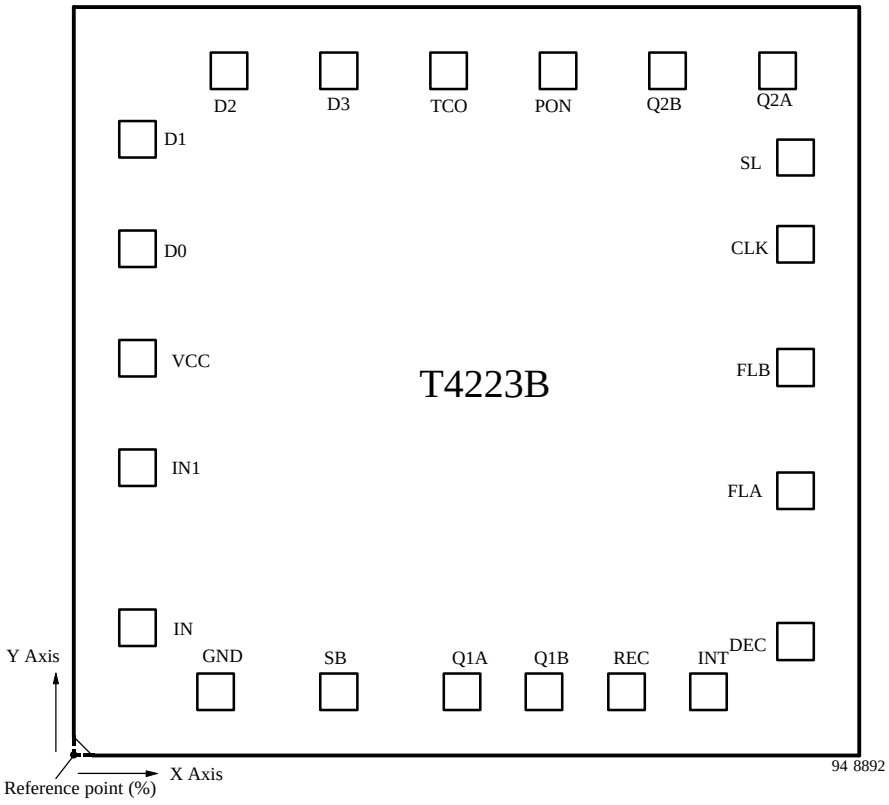


Figure 23.

Information on the German Transmitter

Station: DCF 77,
Frequency 77.5 kHz,
Transmitting power 50 kW

Location: Mainflingen/Germany,
Geographical coordinates: 50° 0.1'N, 09° 00'E
Time of transmission: permanent

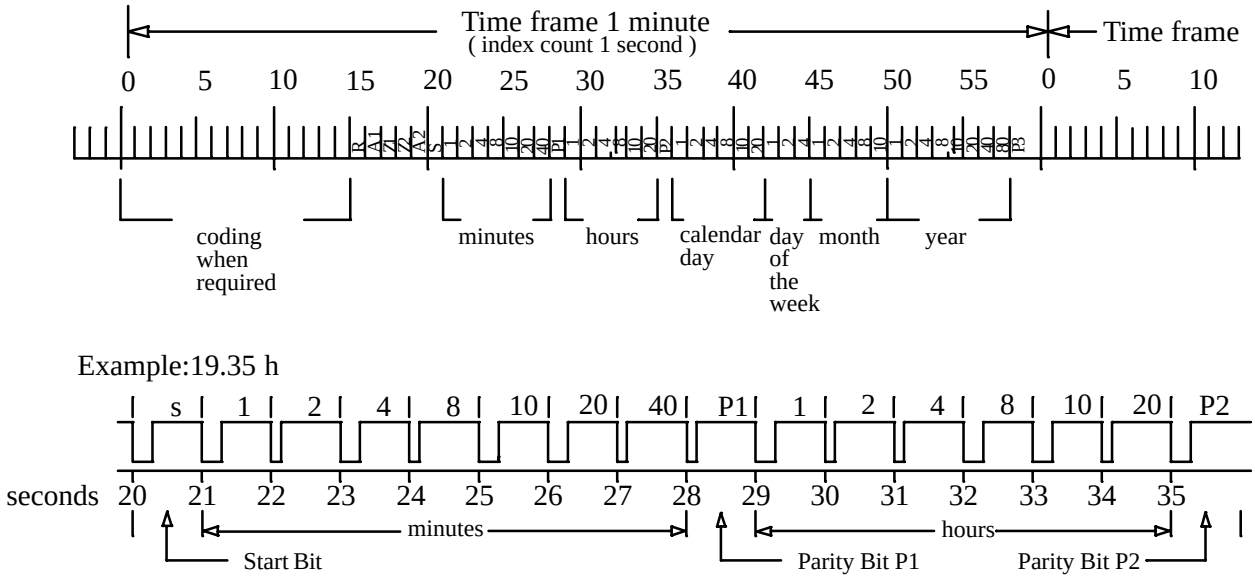


Figure 24.

Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

Time-Code Format (based on Information of Deutsche Bundespost)

The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A1 (announcement of change-over to summer time), Z1 (during summer time 200 ms, otherwise 100 ms), Z2 (during standard time 200 ms, otherwise 100 ms) and A2 (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

Information on the British Transmitter

Station: MSF
Frequency 60 kHz
Transmitting power 50 kW
Location: Teddington, Middlesex

Geographical coordinates: 52° 22'N, 01° 11'W
Time of transmission: permanent, except the first Tuesday of each month from 10.00 h to 14.00 h.

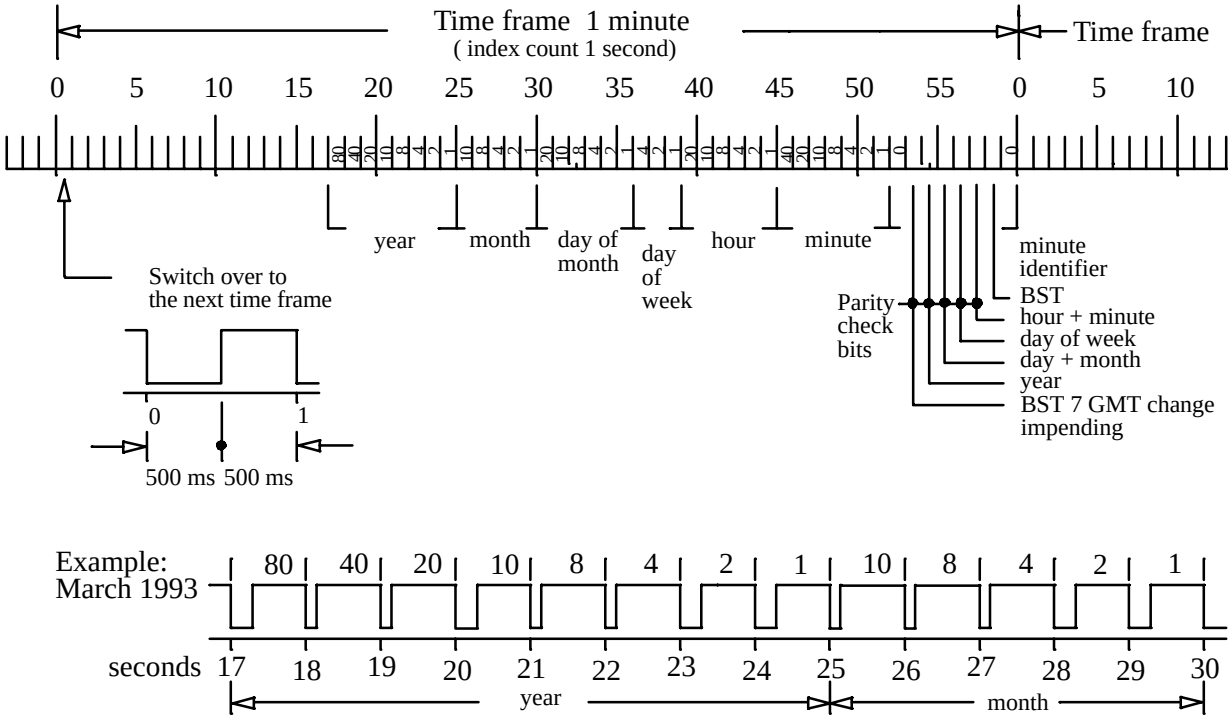


Figure 25.

Modulation

The carrier amplitude is switched off at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one).

Time-Code Format

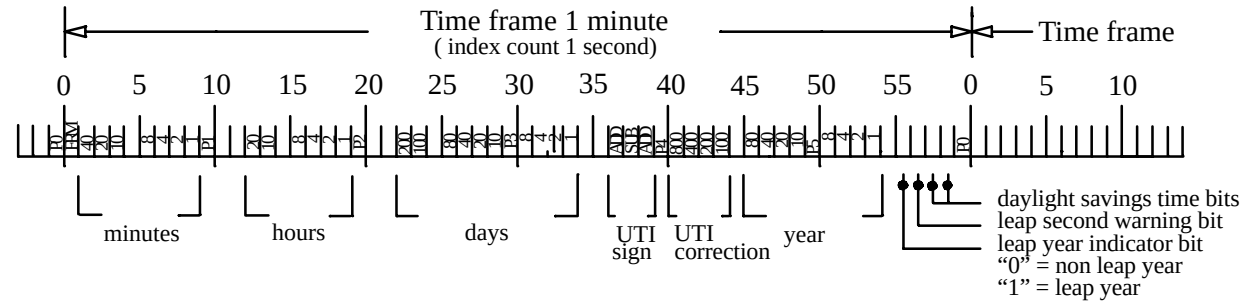
The time-code format consists of 1-minute time frames. A time frame contains BCD–coded information of year, month, calendar day, day of the week, hours and minutes. At the switch-over to the next time frame, the carrier amplitude is switched off for a period of 500 ms.

The prescence of the fast code during the first 500 ms at the beginning of the minute in not guaranteed. The transmission rate is 100 bits/s and the code contains information of hour, minute, day and month.

Information on the US Transmitter

Station: WWVB
Frequency 60 kHz
Transmitting power 40 kW

Location: Fort Collins
Geographical coordinates: 40° 40'N, 105° 03'W
Time of transmission: permanent



Example: UTC 18.42 h

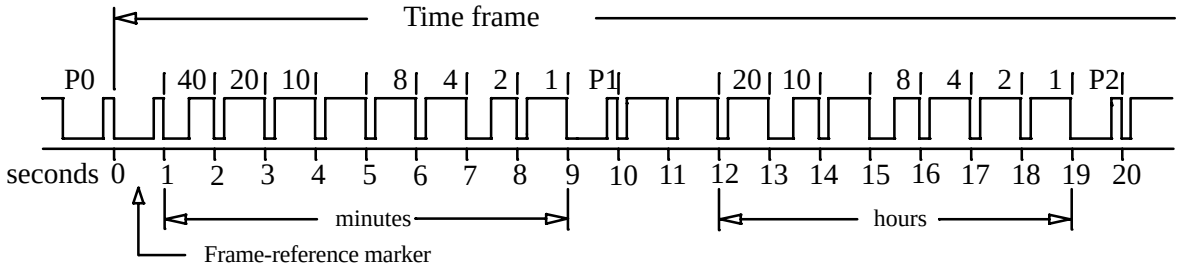


Figure 26.

Modulation

The carrier amplitude is reduced by 10 dB at the beginning of each second and is restored within 500 ms (binary one) or within 200 ms (binary zero).

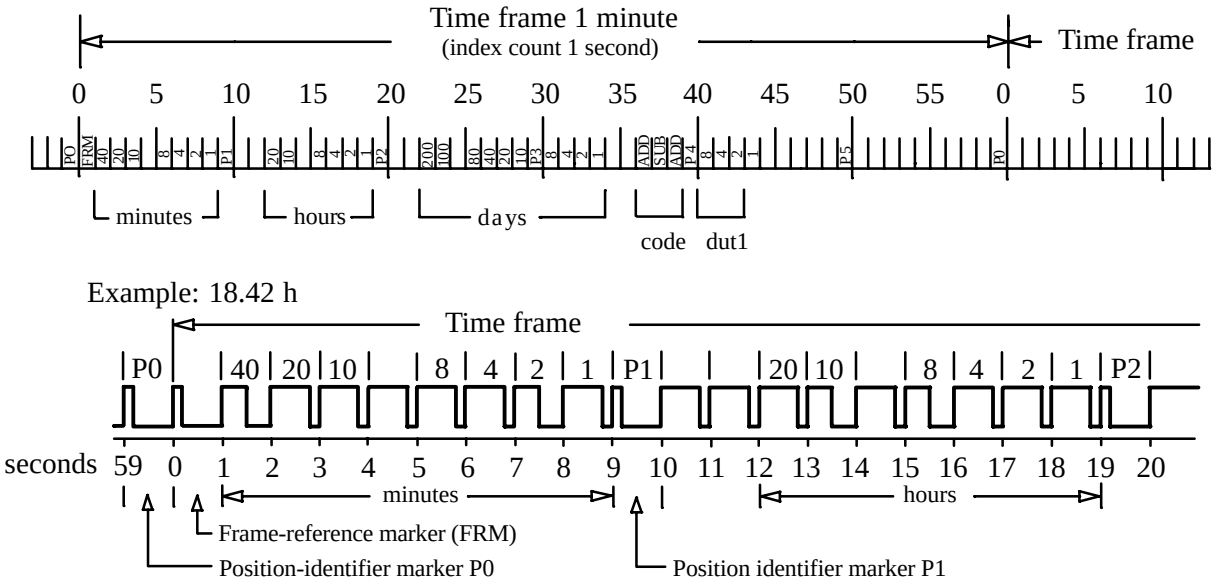
Time-Code Format

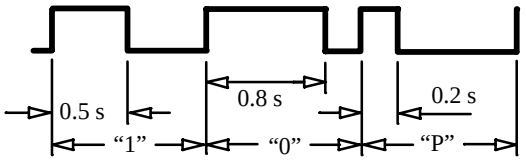
The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days and year. In addition, there are 6 position-identifier markers (P0 thru P5) and 1 frame-reference marker with reduced carrier amplitude of 800 ms duration.

Information on the Japanese Transmitter

Station: JG2AS
Frequency 40 kHz
Transmitting power 10 kW

Location: Sanwa, Ibaraki
Geographical coordinates: 36°11’ N, 139°51’ E
Time of transmission: permanent





0.5 second: Binary one
0.8 second: Binary zero
0.2 second: Identifier markers P0...P5

Figure 27.

Modulation

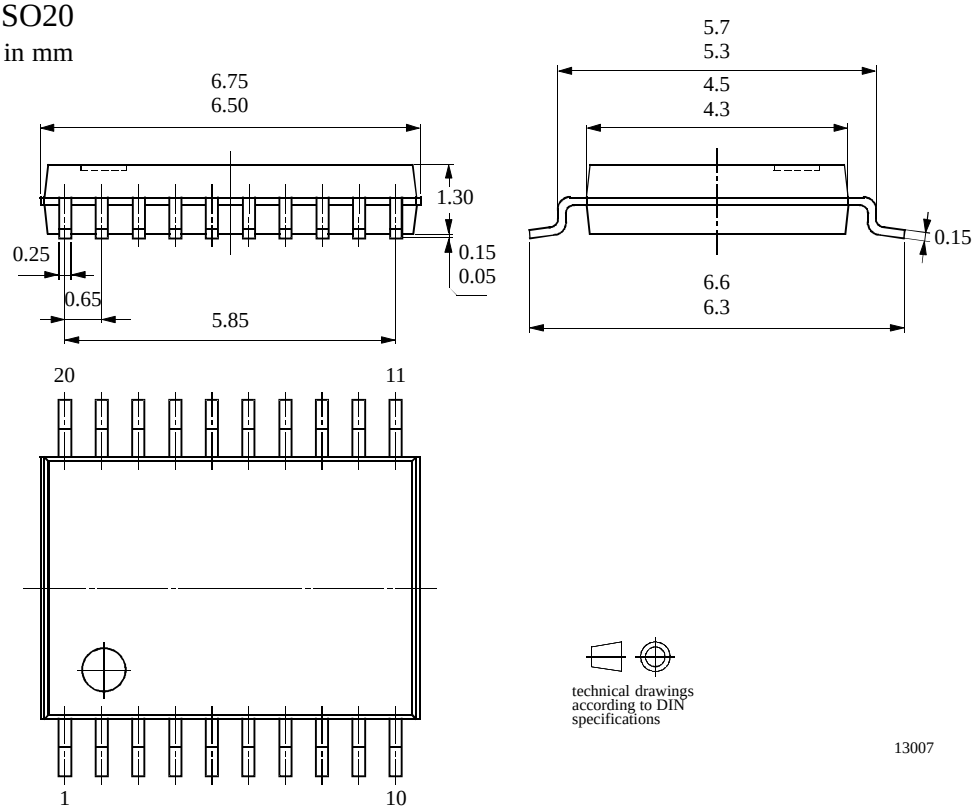
The carrier amplitude is 100% at the beginning of each second and is switched off after 500 ms (binary one) or after 800 ms (binary zero).

Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours and days. In addition, there are 6 position-identifier markers (P0 thru P5) and 1 frame-reference markers (FRM) with reduced carrier amplitude of 800 ms duration.

Package Information

Package SSO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423