μPD17P202A is a model of μPD17202A which is equipped with a one-time PROM in place of the μPD17202A internal mask ROM.

Since the user can write the program to μPD17P202A, the microcomputer is suitable for experimental or small-scale production of μPD17202A systems.

It is recommended that you also read the documents related to μPD17202A, in addition to this data sheet.

FEATURES

- Compatible with μPD17202A
- Internal one-time PROM: 2,048 x 16 bits
- Operating voltage range: 2.2 to 5.5 V

ORDERING INFORMATION

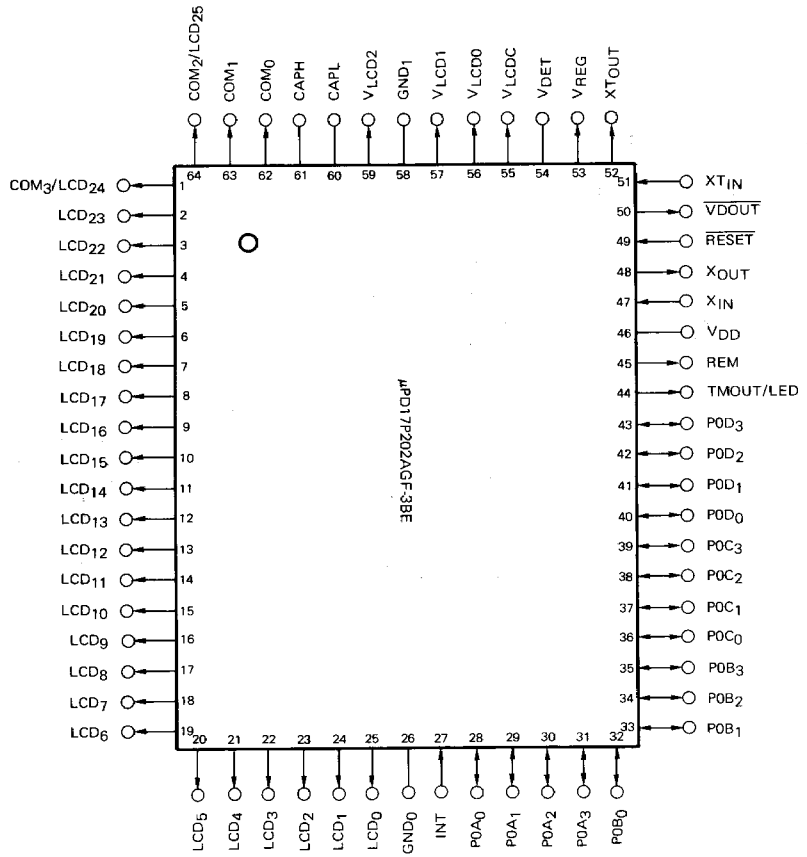
Order Code	Package	Quality Grade
μPD17P202AGF-001-3BE	64-pin plastic QFP (14 x 20 mm)	Standard
μPD17P202AGF-002-3BE	64-pin plastic QFP (14 x 20 mm)	Standard
μPD17P202AGF-003-3BE	64-pin plastic QFP (14 x 20 mm)	Standard

Note: Table below indicates differences in these products:

Item / Part number	Pull-up resistor for $\overline{\text{RESET}}$ pin	Pull-up resistors for P0A, P0B pins	Main clock generator used/unused	Subclock generator used/unused
μPD17P202AGF-001-3BE	Provided	Provided	Used	Used
μPD17P202AGF-002-3BE	Not provided	Provided	Used	Unused
μPD17P202AGF-003-3BE	Not provided	Not provided	Unused	Used

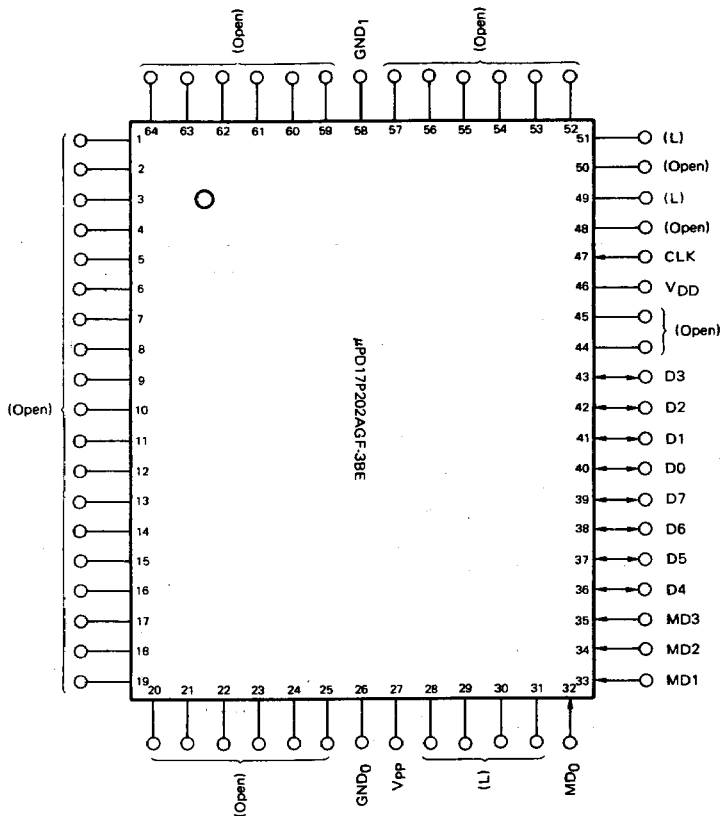
PIN CONFIGURATION (Top View)

(1) Ordinary operation



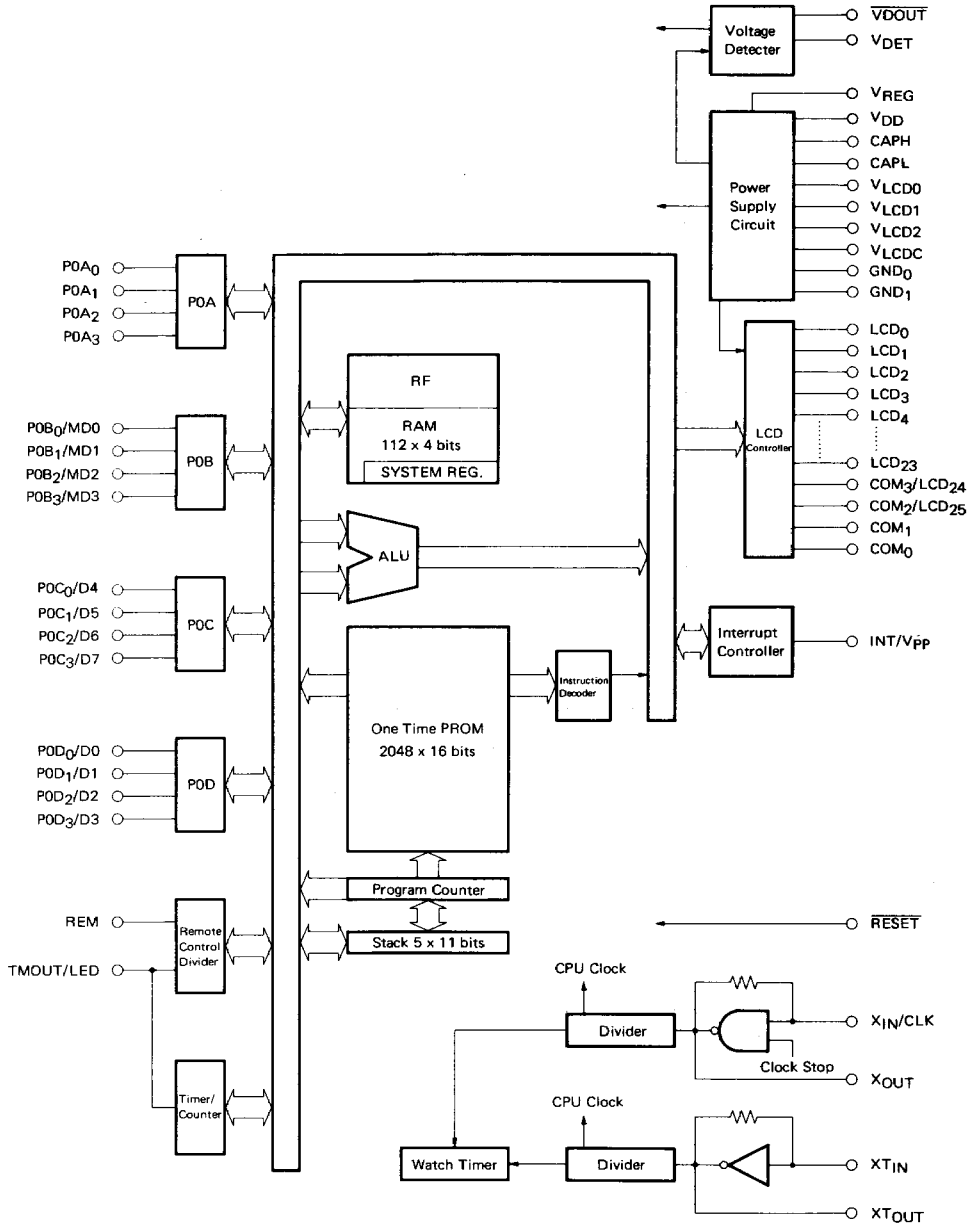
$P0A_0$-$P0A_3$	:	Input/output port
$P0B_0$-$P0B_3$	:	Input/output port
$P0C_0$-$P0C_3$	:	Input/output port
$P0D_0$-$P0D_3$	:	Input/output port
V_{REG}	:	Voltage regulator output
V_{DET}	:	Voltage detector detection voltage adjustment
V_{LCDC}	:	LCD drive reference voltage adjustment
V_{LCD0}-V_{LCD2}	:	LCD drive voltage outputs
LCD_0-LCE_{35}	:	LCD segment signal output
COM_0-COM_3	:	LCD common signal output
TMOUT	:	8-bit timer output
LED	:	Remote control transmission indication output
REM	:	Remote control transmission output
INT	:	External interrupt request signal input
$\overline{RESET}$	:	Reset input
$\overline{VDOUT}$	:	Low voltage detection circuit output
X_{IN}, X_{OUT}	:	Main clock oscillator circuit
XT_{IN}, XT_{OUT}	:	Subclock oscillator circuit
CAPH, CAPL	:	Booster capacitor connection pins
CLK	:	PROM clock input
MD0-MD3	:	PROM mode selection input
D0-D7	:	PROM data input/output
V_{PP}	:	PROM write voltage power supply pin
V_{DD}	:	Power supply pin
GND_0, GND_1	:	GND

(2) PROM programming mode



Note: ( ) indicates processing for pins not used in the PROM programming mode.
L : Ground each of these pins through a 470 Ω resistor.
Open : Do not connect these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 ORDINARY OPERATION MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
62 63 64 1 2 ↓ 25	COM_0 COM_1 LCD_{25}/COM_2 LCD_{24}/COM_3 LCD_{23} ↓ LCD_0	LCD controller/driver segment signal outputs and LCD controller/driver common signal outputs. ● LCD_{25} to LCD_0 ・ LCD controller/driver segment signal outputs ● COM_0 to COM_3 ・ LCD controller/driver common signal outputs	CMOS	–
26	GND_0	GND	–	–
27	INT	Inputs external interrupt request signal. Either the rising edge or the falling edge can be specified as the interrupt request effective edge.	–	Input
28 ↓ 31	$P0A_0$ ↓ $P0A_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs, and can be used as key return inputs for key matrix. See **Note**.	CMOS push-pull	Input
32 ↓ 35	$P0B_0$ ↓ $P0B_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs, and can be used as key return inputs for key matrix. See **Note**.	CMOS push-pull	Input
36 ↓ 39	$P0C_0$ ↓ $P0C_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain output, and can be used for key source output for key matrix.	N-ch open-drain	Input
40 ↓ 43	$P0D_0$ ↓ $P0D_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain output, and can be used for key source output for key matrix.	N-ch open-drain	Input
44	TMOUT/LED	This pin outputs NRZ signal (LED) synchronized with infrared remote control signal and 8-bit timer (TMOUT). ● TMOUT ・ 8-bit timer output ● LED ・ Remote control transmission indication output	CMOS push-pull	High level output

Note: Pull-up resistors are provided only in the μPD17P202A-001 and μPD17P202A-002.

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
45	REM	Infrared remote control signal output.	CMOS push-pull	High level output
46	V_{DD}	Positive voltage power supply pin. 2.2 to 5.5 V is applied in the normal operation mode.	–	–
47 48	X_{IN} X_{OUT}	Main clock oscillation circuit is connected across these pins. Connect a 4 MHz ceramic resonator or crystal resonator across these pins.	–	–
49	$\overline{RESET}$	Reset signal input.	–	Input
50	$\overline{VDOUT}$	Internal low voltage detection circuit output.	CMOS push-pull	–
51 52	XT_{IN} XT_{OUT}	Subclock oscillation circuit is connected across these pins. Connect a 32 kHz crystal resonator across these pins.	–	–
53	V_{REG}	Voltage regulator output for subclock generator.	–	–
54	V_{DET}	A resistor for adjusting the voltage detector detection level is connected to this pin.	–	–
55	V_{LCDC}	Adjusts LCD drive reference voltage.	–	–
56 57	V_{LCD0} V_{LCD1}	Outputs a voltage boosted from LCD drive reference voltage.	–	–
58	GND_1	GND	–	–
59	V_{LCD2}	Outputs a voltage boosted from LCD drive reference voltage.	–	–
60 61	CAPL CAPH	Voltage boosting capacitor is connected across these pins.	–	–

1.2 PROM PROGRAMMING MODE

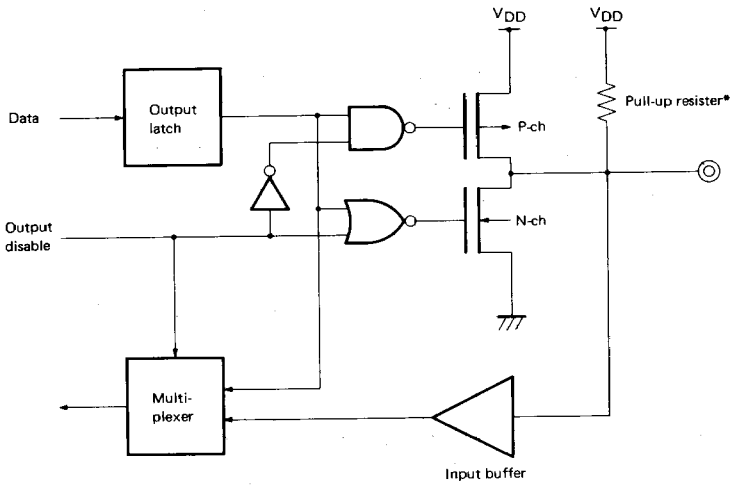
PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
26	GND_0	GND	–	–
27	V_{PP}	Positive power supply pin for PROM programming. 12.5 V is applied to this pin when programming, reading, or verifying the program memory.	–	–
32 I 35	MD3 I MD0	Operation mode selection inputs for PROM programming.	–	Input
36 I 39 40 I 43	D4 I D7 D0 I D3	8-bit data input/output for PROM programming.	CMOS push-pull	Input
46	V_{DD}	Positive power supply pin. 6 V is applied to this pin when programming, reading, or verifying the program memory.	–	–
47	CLK	Clock input for PROM programming.	–	–
48	GND_1	GND	–	–

Remarks: Pins other then listed above are not used in the PROM programming mode. Refer to **"Pin Connection Diagram (2) PROM Programming Mode"** for recommended conditions for unused pins.

1.3 PIN EQUIVALENT CIRCUITS

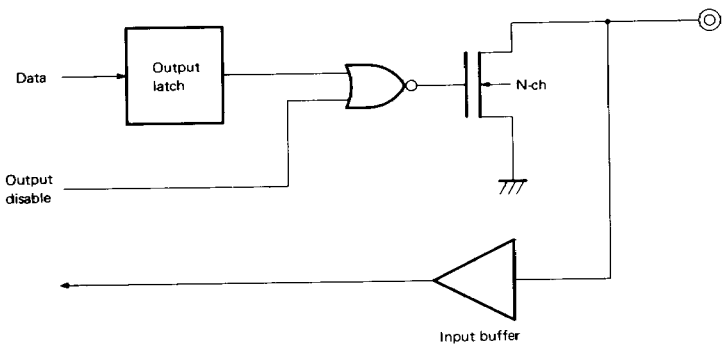
The simplified pin equivalent circuits schematic views for μPD17P202A's pins are presented below.

(1) POA_0 through POA_3, POB_0/MD0 through POB_3/MD3

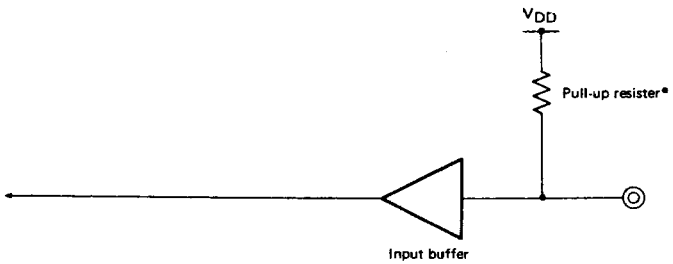


*: Only μPD17P202A-001 and μPD17P202A-002

(2) POC_0/D4 through POC_3/D7, POD_0/D0 through POD_3/D3



(3) $\overline{\text{RESET}}$



*: Only μPD17P202A-001

2. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

When the PROM is to be written, read, or verified, μPD17P201A is set in the PROM mode, and the pins shown in Table 2-1 are used. No address has to be input. Instead, the address is incremented by the clock input from the CLK pin.

Table 2-1 Pins Used to Write/Read/Verify Program Memory

Pin name	Function
V_{PP}	Apply program voltage (12.5 V) to this pin.
CLK	Address incrementing clock input
MD0 to MD3	Operation mode selector
D0 to D7	8-bit data input/output
V_{DD}	Apply operating voltage (6 V) to this pin.

2.1 OPERATION MODES FOR PROGRAM MEMORY WRITE, READ, AND VERIFY

μPD17P202A is set in the program memory write, read, or verify mode, when +6 V is applied to pin V_{DD}, and +12.5 V is applied to pin V_{PP}, after being placed in the reset status (V_{DD} = 5 V, $\overline{RESET}$ = low level) for a certain period of time.

The operation modes, selected by pens MD0 through MD3, are listed in Table 2-2.

Pins not used to write, read, or verify the program memory must be open, or grounded through pull-down resistors (470 Ω).

Table 2-2 Operation Modes for Program Memory Write, Read, and Verify

Operation mode selection						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read, verify mode
		H	x	H	H	Program inhibit mode

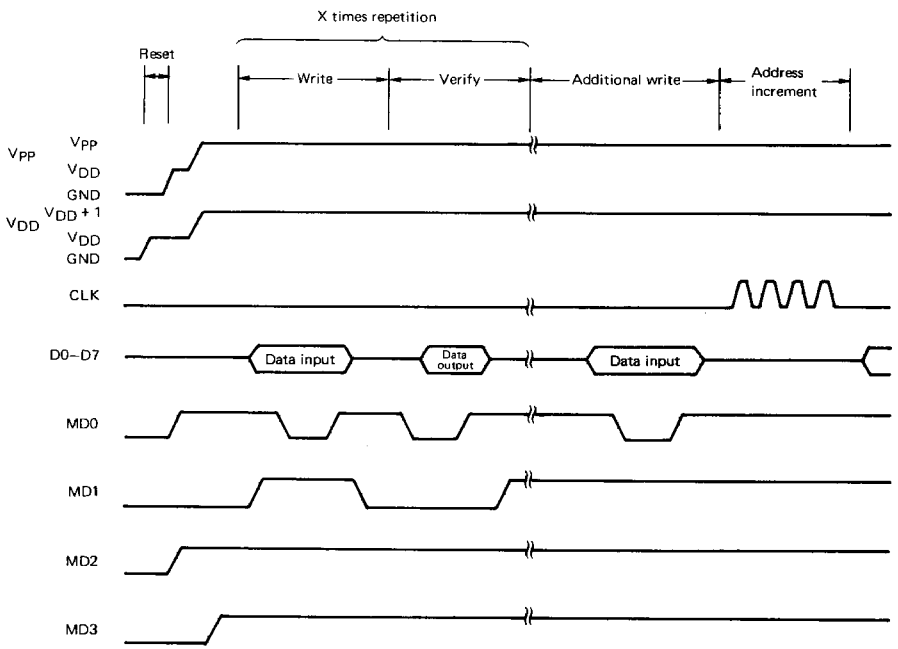
Remarks: x: L or H

2.2 PROGRAM MEMORY WRITING PROCEDURE

Write the program memory by following these steps. The program memory can be written at high speeds.

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Write data in the 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (10), if the memory has been written. If it has not been written, repeat (7) through (9).
(10) Additional writing for (the number of times (7) through (9) are repeated: X) x 1 ms
(11) Program inhibit mode
(12) Input a pulse four times to pin CLK, in order to increment the program memory address (by one).
(13) Repeat (7) through (12), until the last address is programmed.
(14) Program memory address 0 clear mode
(15) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(16) Turn power off.

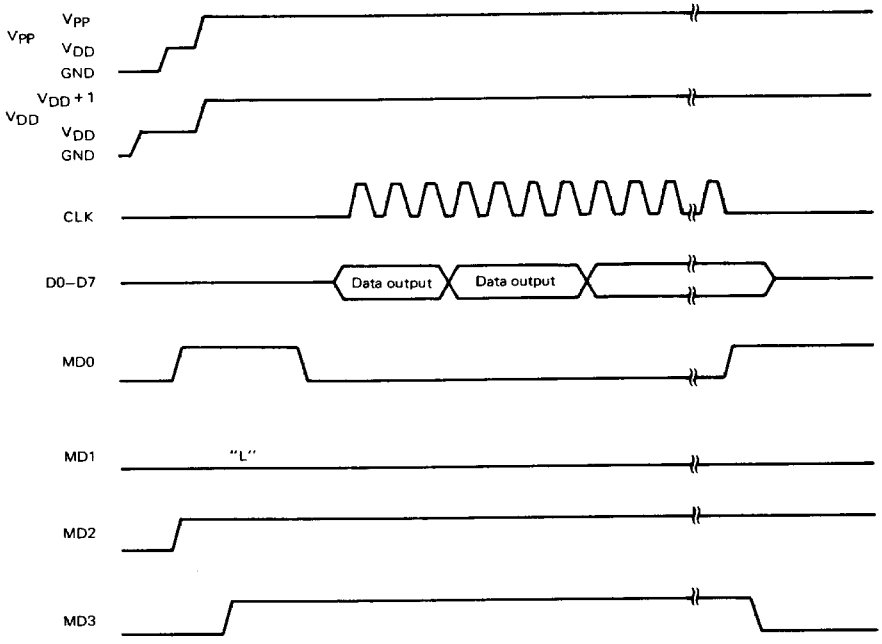
The following figure illustrates steps (2) through (12) above.



2.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Verify mode. The data for each address is output on a one-by-one basis in a cycle during which the clock pulse is input to pin CLK four times.
(8) Program inhibit mode
(9) Program memory address 0 clear mode
(10) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(11) Turn power off.

The following figure illustrates steps (2) through (9) above.



3. DIFFERENCES BETWEEN μPD17P202A AND μPD17202A

In the μPD17P202A, the internal mask ROM (program memory) for the μPD17202A is replaced by the PROM which can be programmed by the user. Therefore, the program memory and some mask options are the only differences between the μPD17P202A and μPD17202A, so the CPU functions and internal hardware are identical.

The table below summarizes the differences between the μPD17P202A and μPD17202A.

Refer to the μPD17202A data sheet for details on CPU functions and internal hardware.

<table>
<tr><th>Device / Item</th><th>μPD17P202A-001</th><th>μPD17P202A-002</th><th>μPD17P202A-003</th><th>μPD17202A</th></tr>
<tr><td>Program memory</td><td colspan="3">• PROM
• 0000H-07FFH
• 2048 x 16 bits</td><td>• Mask ROM
• 0000H-07FFH
• 2048 x 16 bits</td></tr>
<tr><td>$\overline{\text{RESET}}$ pin pull-up resistor</td><td rowspan="3">Provided</td><td>None</td><td rowspan="2">None</td><td rowspan="3">(Mask option)</td></tr>
<tr><td>P0A, P0B pins pull-up resistors</td><td rowspan="2">Provided</td></tr>
<tr><td>Main clock generator provided/not provided</td></tr>
<tr><td>Subclock generator provided/not provided</td><td>None</td><td>Provided</td></tr>
<tr><td>Pin connections</td><td colspan="3">V_{PP} pin, PROM programming pin are provided.</td><td>V_{PP} pin, PROM programming pin not provided</td></tr>
<tr><td>Operating voltage range</td><td colspan="4">2.2 to 5.5 V</td></tr>
<tr><td>Package</td><td colspan="4">64-pin plastic QFP (14 x 20 mm)</td></tr>
</table>

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	Pins INT, $\overline{\text{RESET}}$
	C_{PIN}			10	pF	Other than pins INT, $\overline{\text{RESET}}$

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
LCD Output Voltage Variable Range	V_{LCD0}	0.8		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9 V_{LCD0}	2 V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85 V_{LCD0}	3 V_{LCD0}		V		
Low-voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V	VDET pin external resistance = 2 MΩ	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	RESET	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	P0A-P0D	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	$\overline{\text{RESET}}$	V_{IL} = 0 V, w/o pull-up resistor
	I_{IL3}	20	50	100	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			0.2	μA	P0A, P0B	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	6	12	20	μA		V_{IL} = 0 V w/pull-up resistor
Low-Level Input Current	I_{IL6}			0.2	μA	P0C, P0D	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	V_{OH} = V_{DD}-0.3 V
	I_{OH2}	−7.0	−15.0	−25.0	mA	REM	V_{OH} = V_{DD}-2 V
	I_{OH3}	−0.3	−1.0	−2.0	mA	LED	V_{OH} = V_{DD}-0.3 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	$\overline{\text{VDOUT}}$	V_{OH} = V_{DD}-0.3 V

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VDOUT}$	V_{OL} = 0.3 V
Common Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V	
Supply Current	I_{DD1}		0.5	1.5	mA	Oepration mode	Both XT and X oscillate
	I_{DD2}		15	30	μA		Only XT oscillates
	I_{DD3}		0.5	1.5	mA	HALT mode	Both XT and X oscillate
	I_{DD4}		10	15	μA	STOP mode	Only XT oscillates

DC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Keep V_{PP} to below +13.5 V, including the overshoot.
2: Apply V_{DD} before V_{PP}, and remove V_{DD} after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address setup time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address hold time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 setup time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → data output delay time	t_{DV}	t_{DV}			1	μs	MD0=MD1=V_{IL}
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H}+t_{M1R}$ ≧ 50 μs
MD1 recovery time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program counter reset time	t_{PCR}	–	10			μs	
CLK input high-, low-level width	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			4.19	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	μs	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

*1: Symbols for corresponding μPD27C256

*2: The internal address is incremented (+1) at the falling edge of third clock periods for the four CLK clock periods, which constitute one cycle. The internal address has no external pin connection.