WM2152

12-bit, 30MSPS ADC

DESCRIPTION

The WM2152 is a high speed 12-bit analog-to-digital converter operating on a 3.3V supply. This device includes a high bandwidth sample and hold and internal voltage references. Conversion is controlled by a single clock input.

The device has a differential sample and hold input which gives excellent common-mode noise immunity and low distortion. The maximum differential input voltage can be set by the user, via two mode selection pins, to be 1V or 2V. A third PGA mode is designed particularly for single-ended input signals such as composite video sources. Single-ended input signals require one side of the differential input to be tied to an external voltage source.

The device provides internal reference voltages for setting the ADC full-scale range without the requirement for external circuitry. The WM2152 can also accept external reference levels for applications where common or high precision references are required.

The WM2152 provides an out of range indicator flag to indicate when the input signal exceeds the converter's full scale range. An output enable pin allows several devices to share a common bus. Power down mode for the device is under the control of the two mode control pins and takes power consumption down to less than 36µW.

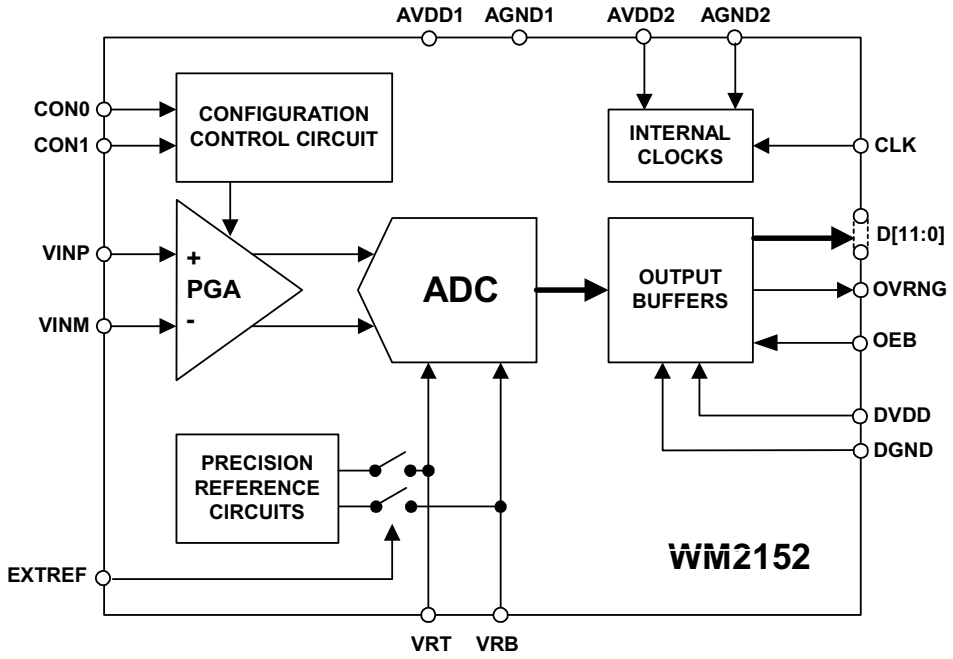
FEATURES

- 12-bit resolution ADC
- 30MSPS conversion rate
- Programmable Gain Amplifier (PGA)
- Out of range indicator
- Low power - 168mW typical at 3.3V supplies
- Powerdown mode to < 36µW
- 66dB SNR for 3.58MHz input signal
- -78db THD for 3.58MHz input signal
- 28-pin TSSOP package

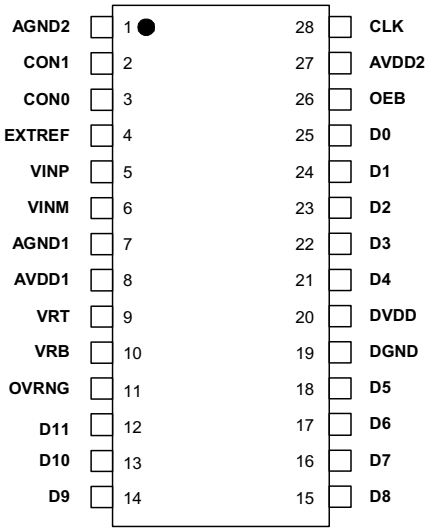
APPLICATIONS

- Direct IF sampling
- Baseband digitisation
- Video Digitisation
- Portable instrumentation
- Digital imaging
- High speed data acquisition

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM2152CDT/V	0 to +70°C	28-pin TSSOP
XWM2152IDT/V	-40 to +85°C	28-pin TSSOP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AGND2	Supply	Analog Ground (for Internal Clocks)
2	CON1	Analog Input	Mode control pin 1
3	CON0	Analog Input	Mode control pin 0
4	EXTREF	Analog Input	Reference select pin (low = internal, high = external)
5	VINP	Analog Input	Positive analog input
6	VINM	Analog Input	Negative analog input
7	AGND1	Supply	Analog ground
8	AVDD1	Supply	Analog power supply
9	VRT	Analog I/O	Upper ADC reference voltage (decoupling or external input)
10	VRB	Analog I/O	Lower ADC reference voltage (decoupling or external input)
11	OVRNG	Digital Output	Out of range indicator (high = out-of-range)
12	D11	Digital Output	Data output bit 11 (MSB)
13	D10	Digital Output	Data output bit 10
14	D9	Digital Output	Data output bit 9
15	D8	Digital Output	Data output bit 8
16	D7	Digital Output	Data output bit 7
17	D6	Digital Output	Data output bit 6
18	D5	Digital Output	Data output bit 5
19	DGND	Supply	Digital ground (digital input/output buffers only)
20	DVDD	Supply	Digital power supply (digital input/output buffers only)
21	D4	Digital Output	Data output bit 4
22	D3	Digital Output	Data output bit 3
23	D2	Digital Output	Data output bit 2
24	D1	Digital Output	Data output bit 1
25	D0	Digital Output	Data output bit 0 (LSB)
26	OEB	Digital Input	Output enable (low = enable, high = disable)
27	AVDD2	Supply	Analog Power Supply (for Internal Clocks)
28	CLK	Analog Input	ADC conversion clock

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per specifications IPC/JEDEC J-STD-020A and JEDEC A113-B, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION	MIN	MAX
Digital supply voltage, DVDD to DGND	-0.3V	+4.0V
Internal clock supply voltage, AVDD2 to AGND2	-0.3V	+4.0V
Analog supply voltage, AVDD1 to AGND1	-0.3V	+4.0V
Maximum ground difference between AGND1, AGND2, and DGND	-0.3V	+0.3V
Voltage range digital input (OEB)	DGND - 0.3V	DVDD + 0.3V
Voltage range analog inputs	AGND1 - 0.3V	AVDD1 + 0.3V
Voltage range CLK input	AGND1 - 0.3V	AVDD1 + 0.3V
Operating junction temperature range, T_J	-40°C	+150°C
Storage temperature	-65°C	+150°C
Lead temperature (1.6mm from package body for 10 seconds)		+300°C
Package Body Temperature (soldering 10 seconds)		+240°C
Package Body Temperature (soldering 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Digital supply range	DVDD		3.0	3.3	3.6	V
Analog supply range	AVDD1, AVDD2		3.0	3.3	3.6	V
Ground	DGND, AGND1, AGND2			0		V
Clock frequency	f_{CLK}				30	MHz
Clock duty cycle			45	50	55	%
Operating Free Air Temperature	T_A	WM2152C	0		70	°C
		WM2152I	-40		85	°C

ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD1 = AVDD2 = DVDD = 3.3V, f_{CLK} = 30MHz, EXTREF = AGND, Mode=1, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
Resolution			12			bits
Integral Nonlinearity	INL	All modes	-2.5	±1.2	+2	LSB
Differential Nonlinearity	DNL	All modes		±0.4	±1	LSB
Missing Codes		All modes	No missing codes guaranteed			
Offset Error		All modes		0.5	1.2	%FSR
Gain Error		All modes		0.5	3.5	%FSR
Power supply rejection ratio	PSRR			54		dB
Dynamic Performance (Note 1)						
Effective number of bits	ENOB	f_{IN} =3.58MHz		10.9		bits
		f_{IN} =10MHz	10.6	10.9		bits
		f_{IN} =15MHz		10.8		bits
Total harmonic distortion	THD	f_{IN} =3.58MHz		-76		dB
		f_{IN} =10MHz		-74	-65	dB
		f_{IN} =15MHz		-72.5		dB
	SNR	f_{IN} =3.58MHz		68		dB
		f_{IN} =10MHz	66	68		dB
		f_{IN} =15MHz		67.7		dB
Signal to noise and distortion ratio	SINAD	f_{IN} =3.58MHz		67.4		dB
		f_{IN} =10MHz	65.6	67.4		dB
		f_{IN} =15MHz		66.6		dB
Spurious free dynamic range	SFDR	f_{IN} =3.58MHz		78.1		dB
		f_{IN} =10MHz	67	76.4		dB
		f_{IN} =15MHz		74.6		dB
Differential phase	DP			0.12		deg
Differential gain	DG			0.01		%
Analog Input Signal to (VINP, VINM)						
Input Span, (VINP – VINM)		Mode=1, VREF = 1V	-1		1	V
		Mode=2, VREF = 1V	-2		2	V
		Mode=3, VREF = 1V	0		1	V
Input (VINP or VINM) range		All modes	0		AVDD	V
Input capacitance	C_{IN}	All modes		6		pF
Analog input bandwidth				180		MHz
Conversion Characteristics						
Conversion frequency	f_{CLK}		5		30	MHz
Pipeline delay				5		cycles of CLK
Aperture delay	t_{AD}			2.0		ns
Aperture jitter				2.0		ps rms
Internal Voltage References (Note 3)						
Upper reference voltage	VRT			2.15		V
Lower reference voltage	VRB			1.15		V
Differential reference voltage (VRT-VRB)	VREF		0.95	1	1.05	V
Power up time of references from standby	t_{PU}			100		µs
External Voltage References (EXTREF = AVDD1)						
Externally applied VRT reference range			2		2.5	V

Test Conditions:
AVDD1 = AVDD2 = DVDD = 3.3V, f_{CLK} = 30MHz, EXTREF = AGND, Mode=1, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Externally applied VRB reference range			1.05		1.3	V
Externally applied differential reference range (VRT-VRB)			0.75		1.05	V
Reference Input Resistance (VRT to VRB)				9		kΩ
Digital Inputs / Outputs						
Input LOW level	V_{IL}				0.2 x DVDD	V
Input HIGH level	V_{IH}		0.8 x DVDD			V
Input current					+/- 1	uA
High level output voltage	V_{OL}	I_{OH}=50µA	DVDD-0.4			V
Low level output voltage	V_{OH}	I_{OL}=-50µA			0.4	V
High Impedance Output Current					±1	µA
Rise/Fall time		C_{LOAD}=10pF		5.5		ns
Analog Control Inputs (EXTREF, CON1, CON2), Clock Input (CLK)						
Input LOW level	V_{IL}				0.2 x AVDD1	V
Input HIGH level	V_{IH}		0.8 x AVDD1			V
Input current					+/- 1	uA
Power Supplies						
AVDD2 supply current	I_{AA2}		3.0	3.3	3.6	mA
AVDD1 supply current	I_{AA1}			35		mA
DVDD supply current	I_{DD}			13		mA
Total supply current	I_{TOT}			48	66	mA
Total supply current in standby mode	I_{SB}	f_{CLK} = 0MHz			10	µA
Power consumption				168	220	mW

Notes

1. Input amplitudes for all single tone dynamic tests are all -0.5dBFS.
2. Inputs for two-tone IMD are 4.4MHz and 4.5MHz, each at -7dBFS.
3. The internal reference voltage is not intended for use driving off-chip.

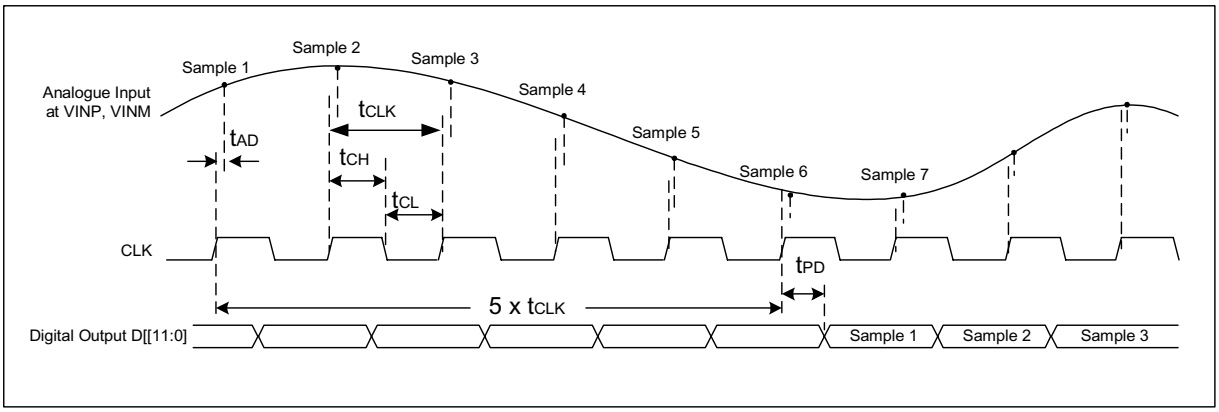


Figure 1. Input and output timing

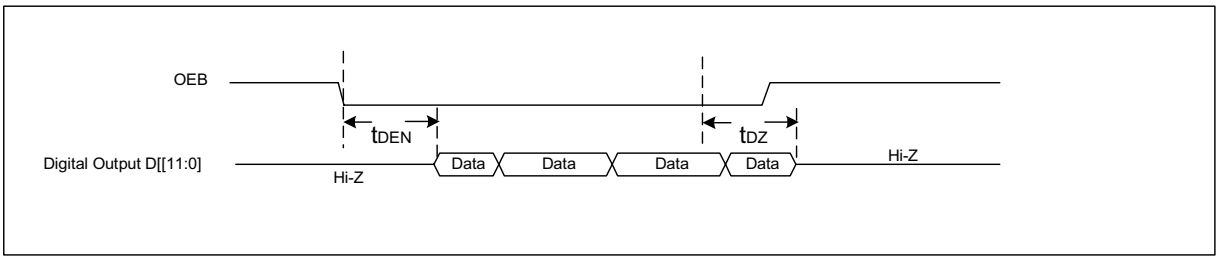


Figure 2. Output enable timing

Test Conditions:
AVDD1 = AVDD2 = DVDD = 3.3V, f_{CLK} = 30MHz, EXTREF = AGND, Mode=1, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing						
Clock period	t_{CLK}		33.3			ns
Clock low or high	t_{CH}, t_{CL}		15	16.6		ns
Pipeline delay				5		CLK cycles
Clock to data valid	t_{PD}				19	ns
Output disable to hi-Z output	t_{DZ}			3.2		ns
Output enable to data valid	t_{DEN}			16	19	ns

TYPICAL SYSTEM PERFORMANCE

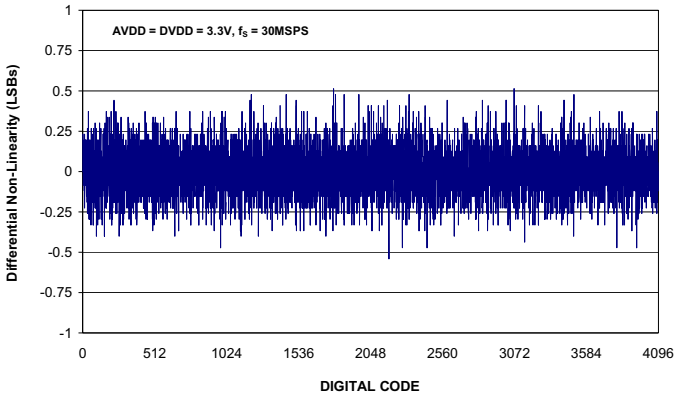


Figure 3 Differential Non-Linearity

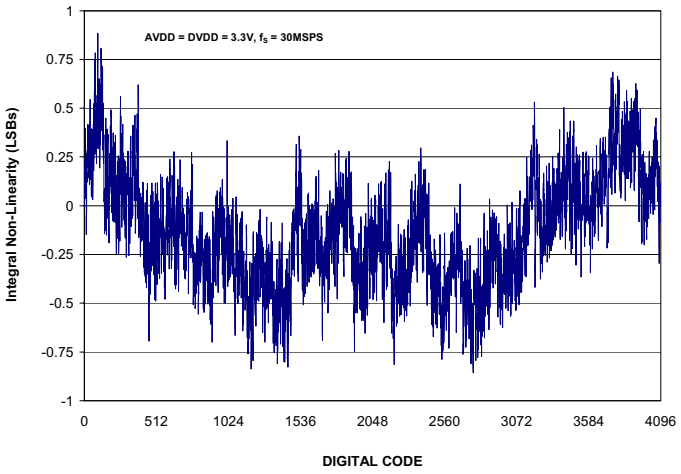


Figure 4 Integral Non-Linearity

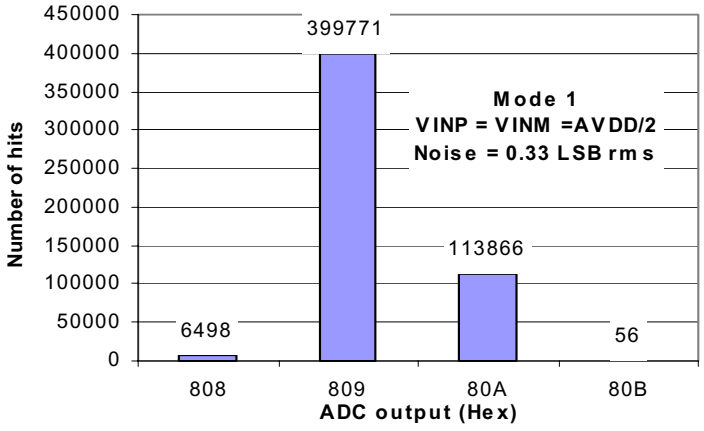


Figure 5 Shorted-Input Noise

DEVICE DESCRIPTION

INTRODUCTION

The WM2152 (see Block Digram on Page 1) consists of:

- Programmable gain amplifier (PGA) including high bandwidth sample-and-hold. This is configured using control pins CON0, CON1.
- 12-bit, 30MSPS pipeline analog-to-digital converter (ADC) core
- On-chip generation of the ADC references VRT and VRB (or external references can be applied to these pins if EXTREF is set high)
- 12-bit parallel digital output, with separate supplies DVDD, DGND.
- Out-of-range output pin OVRNG goes high when the input signal exceeds the converter's range (positive or negative)
- The digital outputs, including OVRNG, are all set high-impedance if OEB is driven low.

CONFIGURATION DETAILS

The device is typically configured by tying pins CON0, CON1, and EXTREF high or low.

- There are no pull-offs on these inputs, so they must not be left floating.
- These inputs have protection diodes and input buffers connected to AVDD and AGND, so they should be tied to AVDD or AGND, not DVDD or DGND.

INTERNAL/EXTERNAL REFERENCES

Pin EXTREF controls whether the ADC voltage references are generated internally, or whether these are supplied externally (for applications where common or high precision references are required)

EXTREF	Mode of Operation
0	Internal References used
1	External References applied.

INPUT SIGNAL RANGE/POWER-DOWN

Pins CON0, CON1 power down the chip, or configure the PGA as follows:

MODE	CON1	CON0	Mode of Operation
0	0	0	Device Powered Down
1	0	1	Single Ended Mode / Differential Mode x1
2	1	0	Differential Mode x0.5
3	1	1	Single Ended Mode with Offset

Figure 6 illustrates the input signal ranges obtainable.

(a) Mode1 - single-ended input: VINM is held constant, VINP acts as a single-ended input with zero-scale VINM-1V and full-scale VINM+1V. (Note VINP could be held constant and VINM used as the input with zero-scale VINP+1V, full-scale VINP-1V).

(b) Mode 1 - differential: complementary inputs are applied to VINM and VINP. Zero scale when VINP-VINM=-1V, full-scale when VINP+VINM=+1V.

(c) Mode 2 - differential mode x 0.5: as (b), but the PGA gain is reduced, so zero scale is now wVINP-VINM=-2V, full-scale when VINP+VINM=+2V.

(d) Mode 3 - single-ended with offset: In mode 3 an offset is applied within the PGA, so now zero scale is VINP=VINM, full-scale is when VINP=VIMN+1V. In this example, VINM is held constant and VINP swings 1V. This mode is useful for positive-going video signals, for example.

(e) Mode 3 - single-ended with offset: as (d), but now VINP is held constant, and VINM is a negative going signal with respect to VINP.

Note:

(i) In all cases, the effective input signal is VINP - VINM.

(ii) The input has excellent common-mode rejection, so VINM and VINP may be placed anywhere between AVDD1 and AGND1.

(iii) The above full-scale ranges assume the nominal internally generated ADC reference voltages, i.e. VRT-VRB = 1V. If externally applied references are used, and VRT-VRB is not 1V, the full-scale ranges will scale accordingly. E.g. in case (a) above, if VRT-VRB is 0.8V, zero scale will occur at VINP=VINM-0.8V, full scale at VINP=VINM+0.8V.

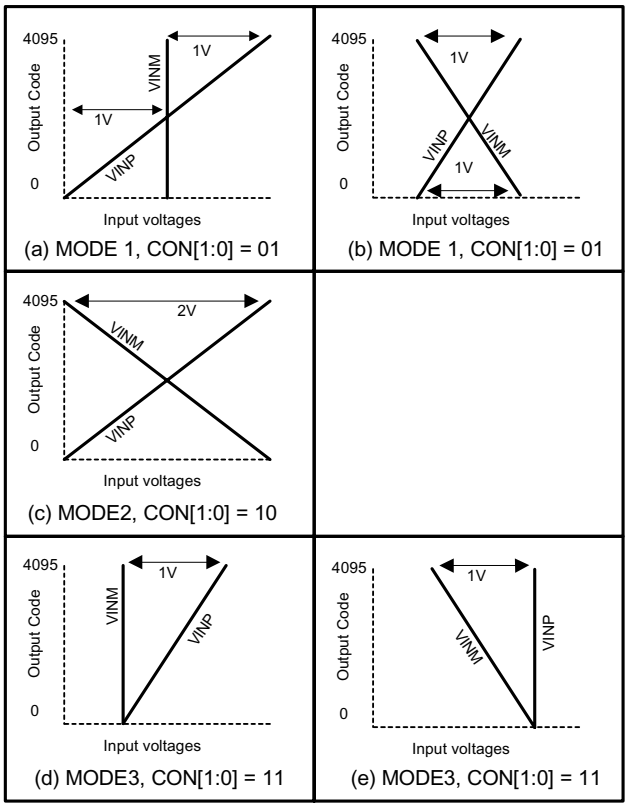


Figure 6 Input voltage ranges

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

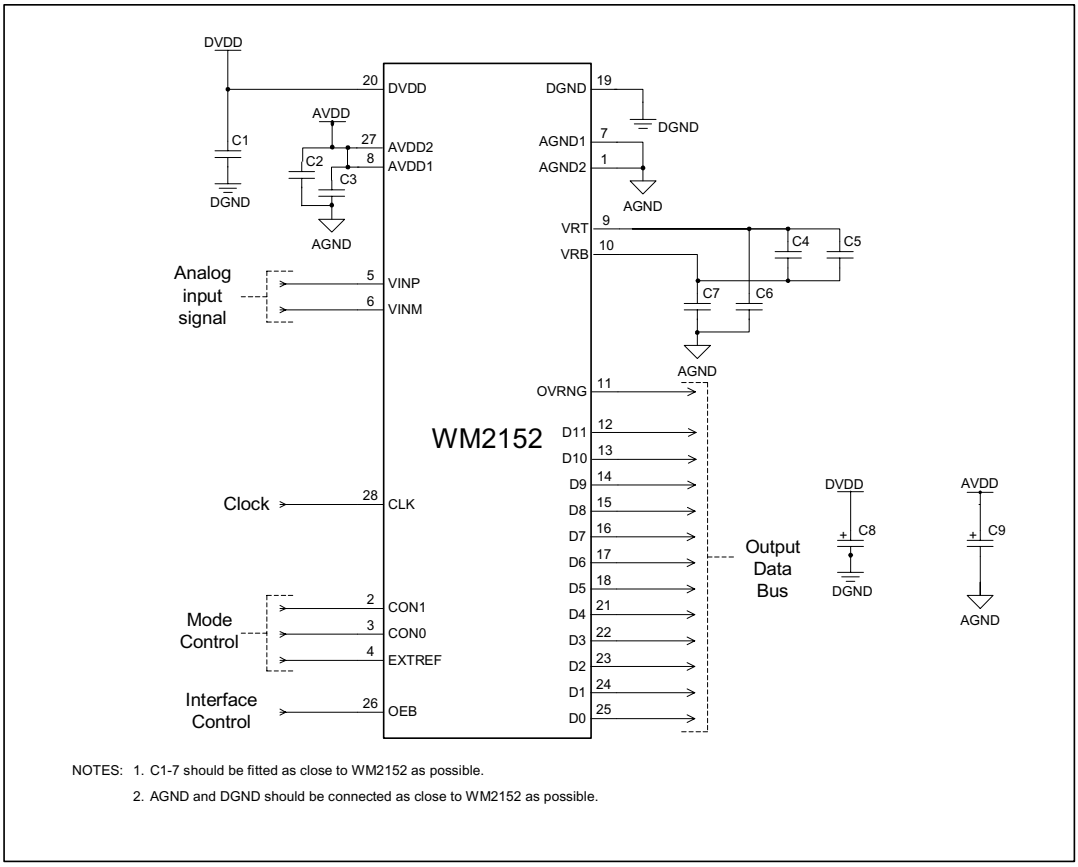


Figure 7 External Components Diagram

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	100nF	De-coupling for DVDD.
C2	100nF	De-coupling for AVDD2.
C3	100nF	De-coupling for AVDD1.
C4	100nF	High frequency de-coupling between VRT and VRB.
C5	10µF	Low frequency de-coupling between VRT and VRB (non-polarised).
C6	100nF	De-coupling for VRT.
C7	100nF	De-coupling for VRB.
C8	10µF	Reservoir capacitor for DVDD.
C9	10µF	Reservoir capacitor for AVDD.

Table 1 External Components Descriptions

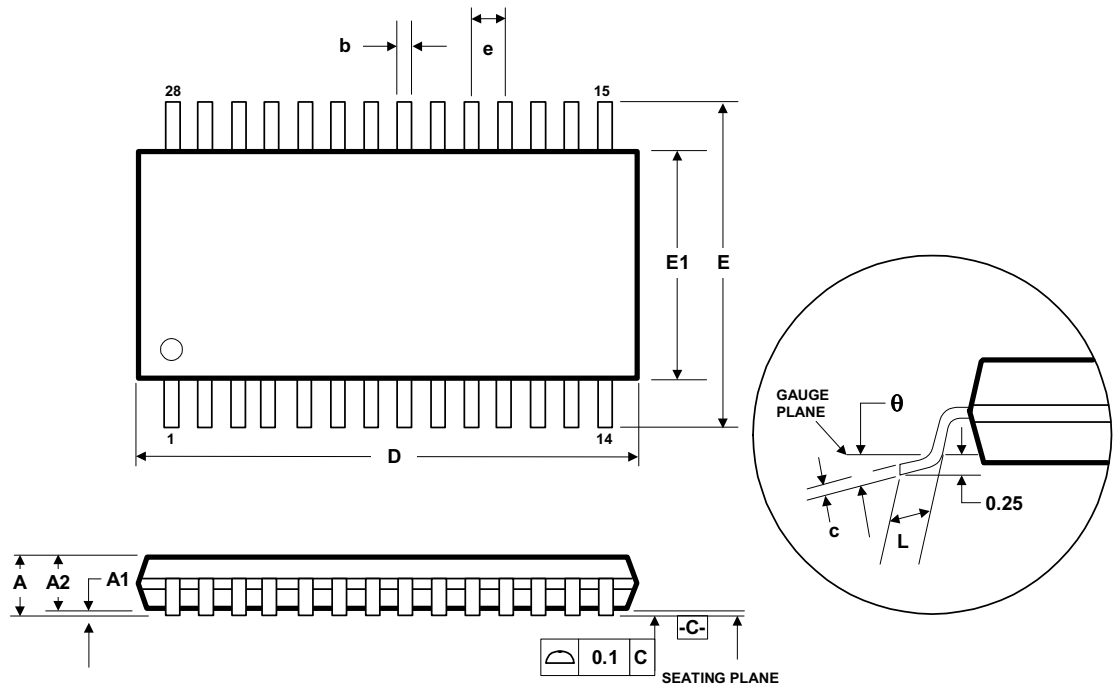
USER TIPS FOR OBTAINING BEST PERFORMANCE FROM THE WM2152

- Drive the clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.
- Minimise capacitive loads on the digital outputs, to minimise on-chip current spikes.
- Use separately decoupled ground planes for digital and analog supplies and for AVDD1,AVDD2. and route any digital return currents away from sensitive analog nodes.
- Keep all decoupling capacitors as close as possible to the respective supply or reference pins.
- Solder the device directly to the PCB: socketing the device will introduce extra parasitic inductance and degrade decoupling
- Small series resistors and shunt capacitors on the analog inputs will help pre-filter high-frequency noise and prevent it being aliased down by the sample-hold. These may also help the preceding amplifier to drive into the switched-capacitior inputs of the WM2152.

An Evaluation Kit WM2152-EV1B is available for this part, consisting of an evaluation board and manual.

PACKAGE DIMENSIONS

DT: 28 PIN TSSOP (9.7 x 4.4 x 1.0 mm) **DM022.A**



Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	9.60	9.70	9.80
e	0.65 BSC		
E	6.4 BSC		
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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