JLC1562B

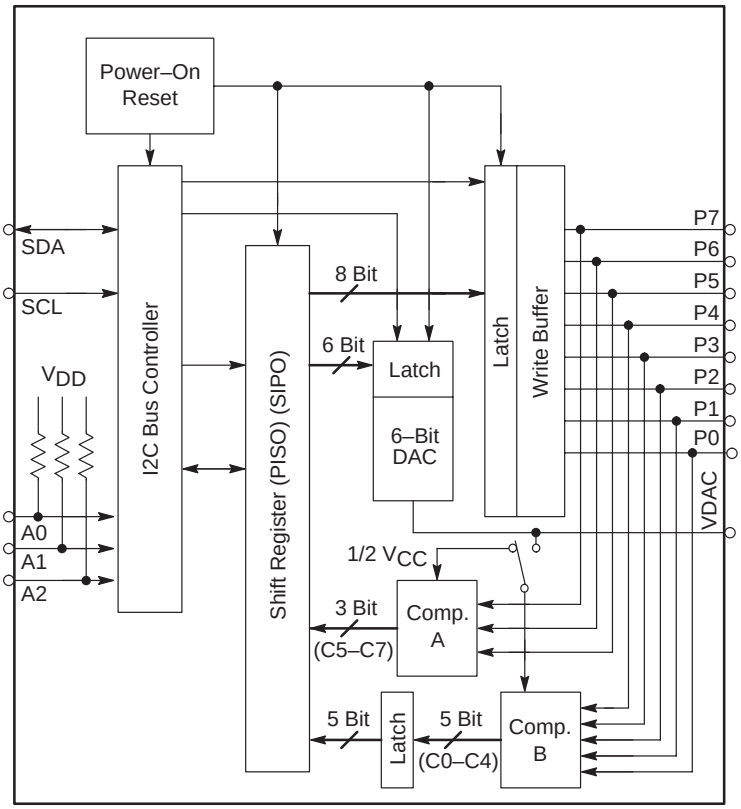
I2C Bus I/O Expander

The JLC1562B facilitates easy I2C Bus expandibility. Multiple devices (up to 8 on the same I2C Bus) are easily added as each device has its own selectable 3–bit address. The JLC1562B provides an 8–bit bidirectional input/output port and 6–bit resolution Digital to Analog Converter. The device can also be used as an Analog to Digital Converter with 5 input signal lines each with 6–bit A/D resolution. The voltage on pins P0–P4 is compared with a controllable threshold voltage and the results are readable through the I2C Bus.

I2C Bus interface pins SDA, SCL and A0–A2 are; Serial Data, Serial Clock and Device Address respectively. External interface pins are P0–P7 and VDAC; I/O Port and D/A output.

Features

- Low Power Dissipation
- I2C–Bus Format (2–wire type; SDA, SCL) Data Transfer
- 6–bit A/D Converter
- Bus Address Selectable (3–bit)
- Address Input pins are pulled up to Vdd with internal resistor
- I/O pins are Open Drain Outputs
- Analog Input through Comparator
- Inputs Protected from External Bus Currents in Power Down mode



NOTE: Internal Power On Reset sets P0 ~ P7 low, sets VDAC to 1/80 V_{DD} and selects 1/2 V_{DD} for Comparator “B” threshold.

Figure 1. Block Diagram

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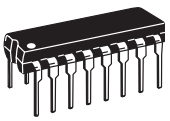
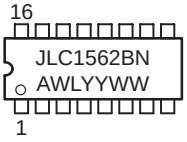
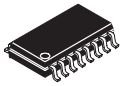
MARKING DIAGRAMS

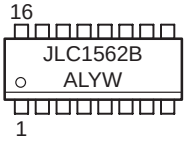


PDIP–16
N SUFFIX
CASE 648



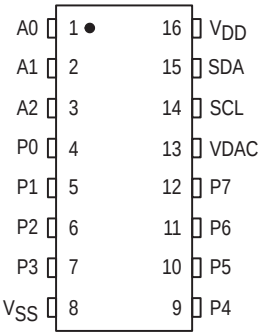


EIAJ–16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

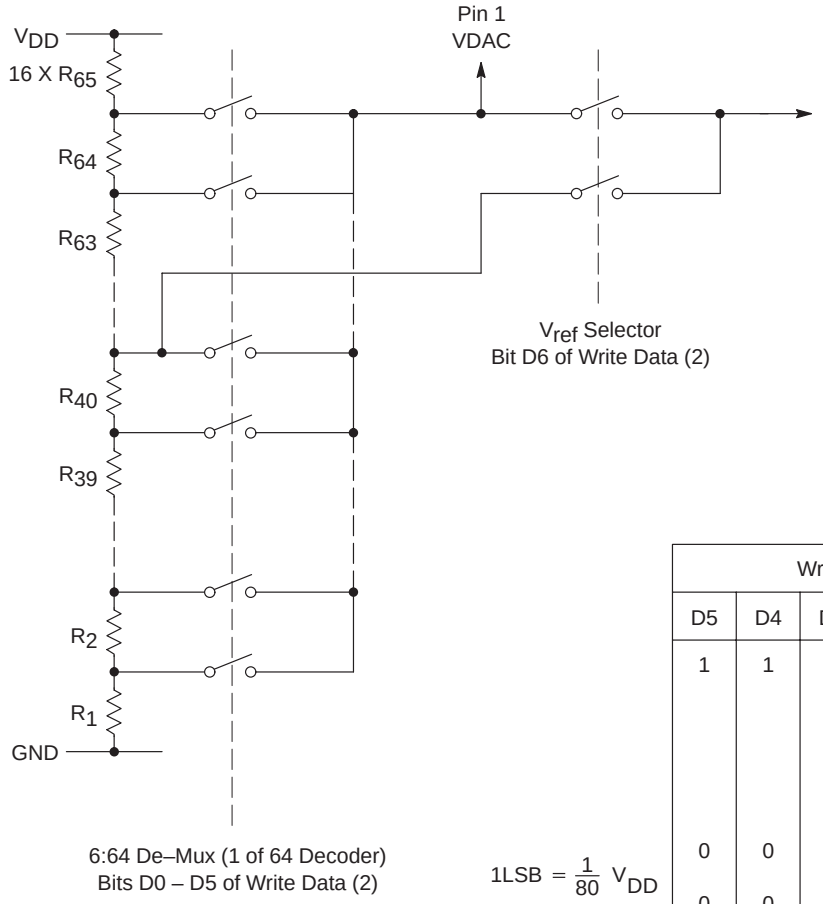
PIN ASSIGNMENT



PIN LIST	
A0–A2	Chip Address Input
P0–P4	Comparator Input / Open Drain Output
P5–P7	Comparator Input / Open Drain Output
SCL	Serial Clock Input
SDA	I2C Data Output
VDAC	DAC Output

ORDERING INFORMATION

Device	Package	Shipping
JLC1562BN	PDIP–16	500 / Unit Pak
JLC1562BF	EIAJ–16	50 Units / Rail
JLC1562BFEL	EIAJ–16	2000 Units / Reel



Write Data (2)	
D6	V_{ref} Value
1	V_{ref} = VDAC
0	$V_{ref} = \frac{40}{80} V_{DD}$

Write Data (2)						
D5	D4	D3	D2	D1	D0	V_{ref}
1	1	1	1	1	1	$\frac{64}{80} V_{DD}$
			•			•
			•			•
			•			•
			•			•
0	0	0	0	0	1	$\frac{2}{80} V_{DD}$
0	0	0	0	0	0	$\frac{1}{80} V_{DD}$

MAXIMUM RATINGS (Referenced to GND)

Symbol	Parameter	Value	Unit
V_{dd}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{dd} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{dd} + 0.5	V
I	DC Input/Output Current (per Pin)	25	mA
IDD	DC Supply Current (VDD and GND Pins)	75	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	300	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{dd}	DC Supply Voltage	4.2	6.0	V
V_{in}, V_{out}	DC Input Voltage	0.0	V_{dd}	V
T_A	Operating Temperature	– 40	+ 85	°C

DC CHARACTERISTICS (Referenced to V_{SS})

Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
V_{IH}	Maximum Input Voltage, “H”	0.7 V_{dd}	–	V
V_{IL}	Maximum Input Voltage, “L”	–	0.3 V_{dd}	V
V_{OL}	Maximum Output Voltage, “L” (I_{out} = 4mA)	–	0.3	V
I_{in}	Maximum Input Leakage Current (V_{in} = V_{dd} or V_{ss}, SCL pin only)	–	± 1.0	μA
I_{oz}	Maximum Output Hi–Z Leakage Current (Output = High Impedance; V_{out} = V_{dd})	–	± 5.0	μA
C_{in}	Maximum Input Capacitance (Input Pin)	–	10	pF
C_{out}	Maximum Output Capacitance (Output Pin)	–	15	pF
$C_{i/o}$	Maximum I/O Capacitance (I/O Pin)	–	15	pF
V_{ICR}	Comparator Common Mode Input Voltage Range	0	V_{dd} – 1.5	V
I_{CC}	Maximum Quiescent Supply Current (per Package)	–	5.0	mA

COMPARATOR AC CHARACTERISTICS

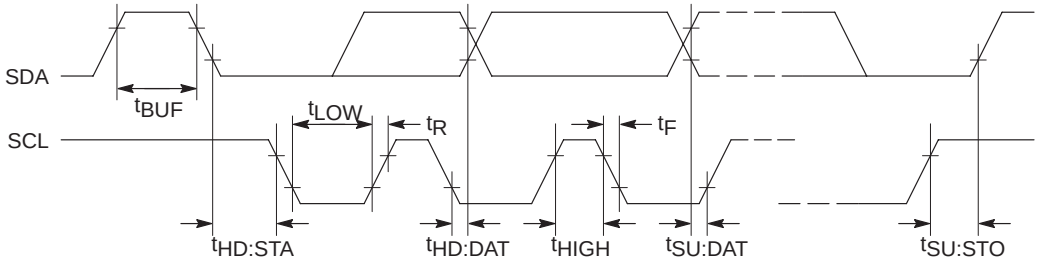
Symbol	Parameter	Test Conditions	Guaranteed Limit			Unit
			Min	Typ	Max	
t_{PD}	Maximum Propagation Delay	V_{ref} = 1.5V, 10mV overdrive	–	1.0	–	μS
		V_{ref} = 1.5V, 100mV overdrive	–	0.2	–	μS

DA COMPARATOR CHARACTERISTICS

Symbol	Parameter	Guaranteed Limit			Unit
		Min	Typ	Max	
DNL	DAC Referential NON–Linearity		±1/4 LSB		
e_{FS}	DAC Full Scale Error			±1 LSB	
e_{ZC}	DAC Zero Scale Error			±1 LSB	

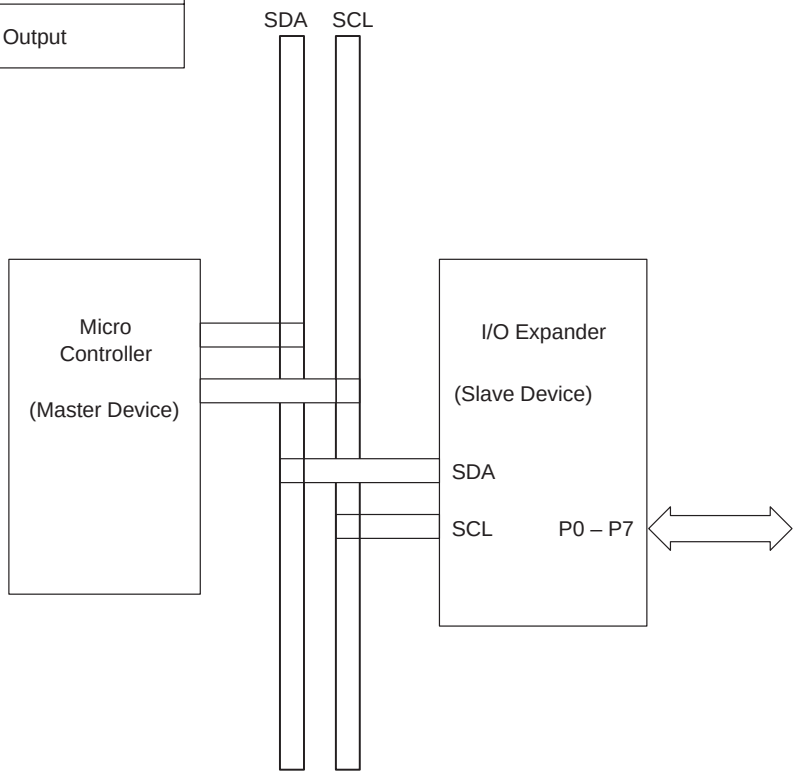
TIMING CHARACTERISTICS

Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
f_{CL}	SCL CLOCK Frequency	0	100	kHz
t_{BUF}	BUS Free Time (Between “STOP” and “START”)	4.7	–	μs
$t_{HD:STA}$	HOLD Time for “START”	4.0	–	μs
t_{LOW}	HOLD Time at SCL CLOCK LOW	4.7	–	μs
t_{HIGH}	HOLD Time at SCL CLOCK HI	4.0	–	μs
$t_{HD:DAT}$	DATA HOLD Time	0	–	μs
$t_{SU:DAT}$	DATA SETUP Time	250	–	ns
t_R	Rise Time (SDA and SCL)	–	1000	ns
t_F	Fall Time (SDA and SCL)	–	300	ns
$t_{SU:STO}$	SETUP Time for “STOP”	4.0	–	μs



READ / WRITE MODES

MODE	SDA		I/O Expander
	Master Device	Slave Device	I/O Port
READ	Receiver	Transmitter	Input
WRITE	Transmitter	Receiver	Output



The JLC1562B Supports the following types of Bus Cycles

1.) WRITE MODE (A)

S	Slave Address & R/W	SACK	Write Data (1)	SACK	P

2.) WRITE MODE (B)

S	Slave Address & R/W	SACK	Write Data (1)	SACK	Write Data (2)	SACK	P

3.) READ MODE (A)

S	Slave Address & R/W	SACK	Read Data	MACK	P

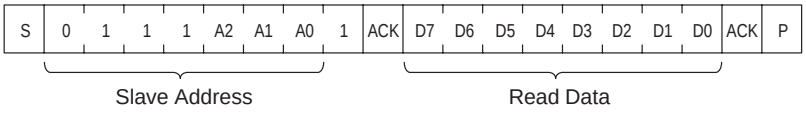
4.) READ MODE (B)

S	Slave Address & R/W	SACK	Read Data (1)	MACK	Read Data (2)	MACK	Read Data (3)	MACK	•••	P

S = START Condition
SACK = Slave Acknowledgement
MACK = Master Acknowledgement
P = STOP Condition

READ WRITE DATA FORMAT

<<READ MODE>>

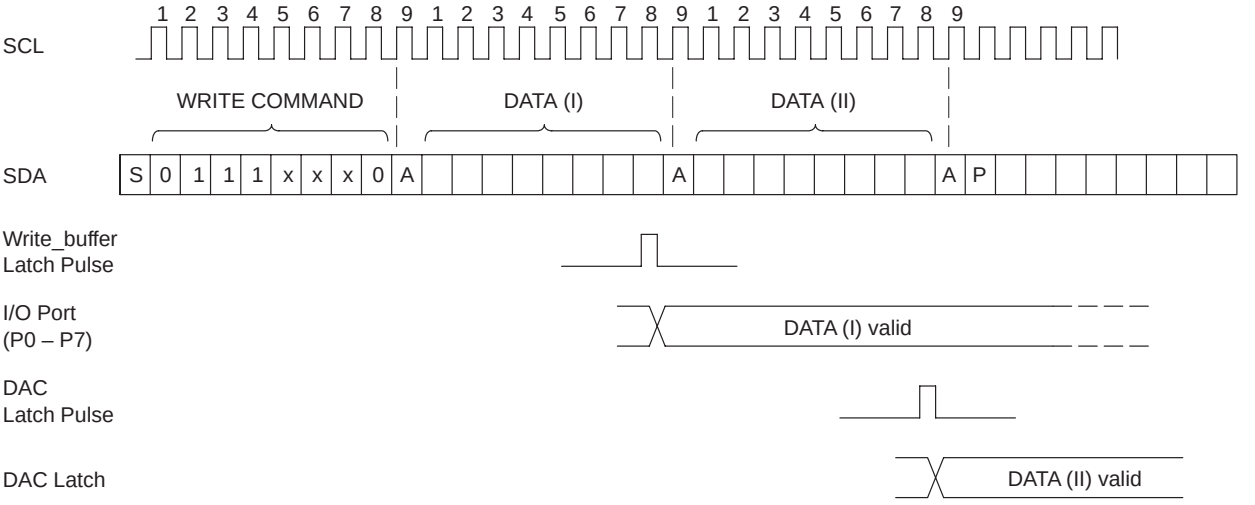


Slave Address	A0 – A2	I/O Expander Device Address (Pins A0 – A2)
	A3 – A6	A6 A5 A4 A3 is hard wired as 0 1 1 1
	R/W	1 : READ ADDRESS
Read Data	D5 – D7	Output of Comparator “A”. (V_{th} = 1/2 V_{DD})
	D0 – D4	Output of Comparator “B”. (V_{th} = 1/2 V_{DD} OR V_{DAC}) READ LATCH Bit Controls when Data Will Be Latched.

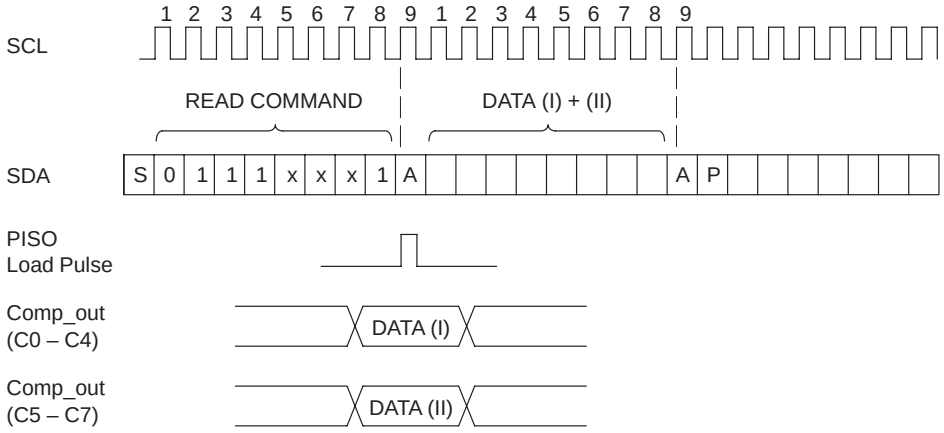
<<WRITE MODE>>

Slave Address	A0 – A2	I/O Expander Device Address (Pins A0 – A2)
	A3 – A6	A6 A5 A4 A3 is hard wired as 0 1 1 1
	R/W	0 : WRITE ADDRESS
Write Data (1)	D0 – D7	Device Pins P0 to P7 Output Bits.
Write Data (2)	D7	READ LATCH CONTROL Latch Control of Signals C0 – C4 in the Device BLOCK DIAGRAM 0 : Data is latched at the ACK after a READ COMMAND. 1 : Data is latched when Comparator “B” switches from 0 to 1. (V_{th}.) Data is reset at the ACK after a READ COMMAND.
	D6	COMPARATOR “B” V_{ref} Control Bit 0 : $V_{ref} = \frac{40}{80} V_{DD}$ 1 : $V_{ref} = V_{DAC}$
	D0 – D5	DAC Input Bits

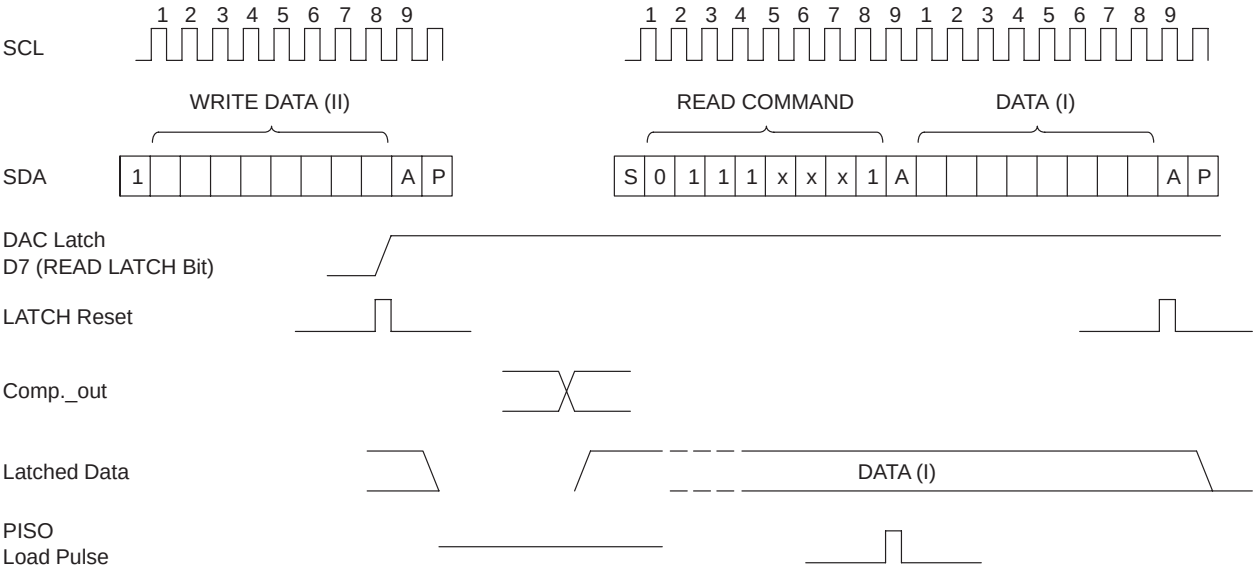
<<WRITE MODE>>



<<READ MODE>> (READ LATCH = 0)

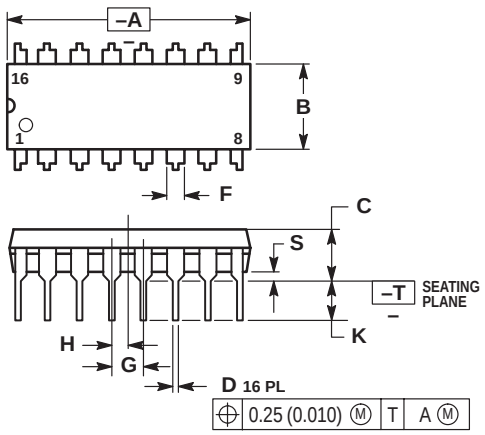


<<READ MODE>> (READ LATCH = 1)



PACKAGE DIMENSIONS

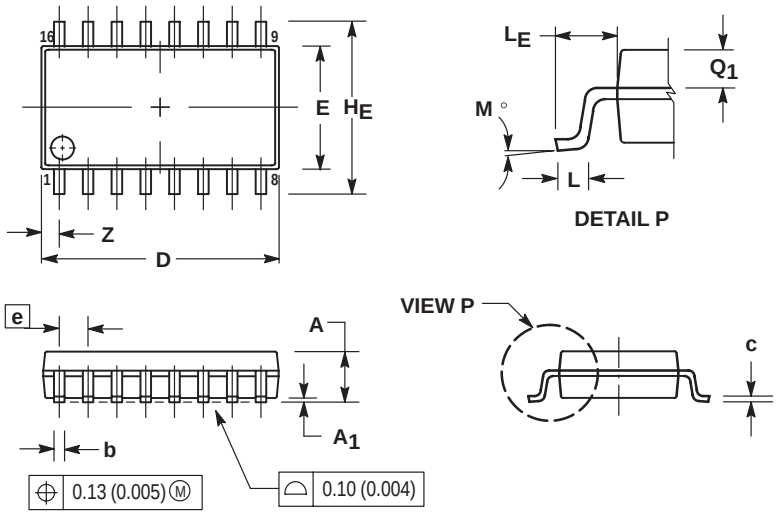
PDIP–16
N SUFFIX
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

F SUFFIX
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	——	2.05	——	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	——	0.78	——	0.031

NOTE: The “E” in this Publication Order Number denotes English version.
The Japanese version of this document is available from Japan as JLC1562B/D

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