

NTMD3P03R2

Power MOSFET -3.05 Amps, -30 Volts

Dual P-Channel SO-8

Features

- High Efficiency Components in a Dual SO-8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for the SO-8 Package is Provided

Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery-Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-30	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	171	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.73	W
Continuous Drain Current @ 25°C	I_D	-2.34	A
Continuous Drain Current @ 70°C	I_D	-1.87	A
Pulsed Drain Current (Note 4)	I_{DM}	-8.0	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Continuous Drain Current @ 25°C	I_D	-3.05	A
Continuous Drain Current @ 70°C	I_D	-2.44	A
Pulsed Drain Current (Note 4)	I_{DM}	-12	A
Thermal Resistance – Junction-to-Ambient (Note 3)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0	W
Continuous Drain Current @ 25°C	I_D	-3.86	A
Continuous Drain Current @ 70°C	I_D	-3.1	A
Pulsed Drain Current (Note 4)	I_{DM}	-15	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = -30\text{ Vdc}$, $V_{GS} = -4.5\text{ Vdc}$, Peak $I_L = -7.5\text{ Apk}$, $L = 5\text{ mH}$, $R_G = 25\ \Omega$)	E_{AS}	140	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

1. Minimum FR-4 or G-10 PCB, $t = \text{Steady State}$.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t = \text{steady state}$.
3. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t \leq 10\text{ seconds}$.
4. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

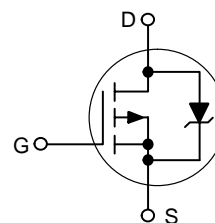


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V_{DSS}	$R_{DS(on)}$ TYP	I_D MAX
-30 V	85 m Ω @ -10 V	-3.05 A

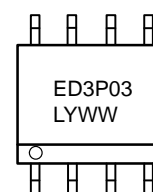
P-Channel



MARKING DIAGRAM

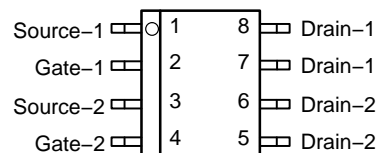


SO-8
CASE 751
STYLE 11



ED3P03 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTMD3P03R2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMD3P03R2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = -250 μ Adc) Temperature Coefficient (Positive)	V _{(BR)DSS}	-30 -	- -30	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = -24 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = -24 Vdc, V _{GS} = 0 Vdc, T _J = 125°C) (V _{DS} = -30 Vdc, V _{GS} = 0 Vdc, T _J = 25°C)	I _{DSS}	- - -	- - -	-1.0 -20 -2.0	μ Adc
Gate-Body Leakage Current (V _{GS} = -20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	-100	nAdc
Gate-Body Leakage Current (V _{GS} = +20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = -250 μ Adc) Temperature Coefficient (Negative)	V _{GS(th)}	-1.0 -	-1.7 3.6	-2.5 -	Vdc
Static Drain-to-Source On-State Resistance (V _{GS} = -10 Vdc, I _D = -3.05 Adc) (V _{GS} = -4.5 Vdc, I _D = -1.5 Adc)	R _{DS(on)}	- -	0.063 0.090	0.085 0.125	Ω
Forward Transconductance (V _{DS} = -15 Vdc, I _D = -3.05 Adc)	g _{FS}	-	5.0	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = -24 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	-	520	750	pF
Output Capacitance		C _{oss}	-	170	325	
Reverse Transfer Capacitance		C _{rss}	-	70	135	

SWITCHING CHARACTERISTICS (Notes 6 and 7)

Turn-On Delay Time	(V _{DD} = -24 Vdc, I _D = -3.05 Adc, V _{GS} = -10 Vdc, R _G = 6.0 Ω)	t _{d(on)}	-	12	22	ns
Rise Time		t _r	-	16	30	
Turn-Off Delay Time		t _{d(off)}	-	45	80	
Fall Time		t _f	-	45	80	
Turn-On Delay Time	(V _{DD} = -24 Vdc, I _D = -1.5 Adc, V _{GS} = -4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	-	16	-	ns
Rise Time		t _r	-	42	-	
Turn-Off Delay Time		t _{d(off)}	-	32	-	
Fall Time		t _f	-	35	-	
Total Gate Charge	(V _{DS} = -24 Vdc, V _{GS} = -10 Vdc, I _D = -3.05 Adc)	Q _{tot}	-	16	25	nC
Gate-Source Charge		Q _{gs}	-	2.0	-	
Gate-Drain Charge		Q _{gd}	-	4.5	-	

BODY-DRAIN DIODE RATINGS (Note 6)

Diode Forward On-Voltage	(I _S = -3.05 Adc, V _{GS} = 0 V) (I _S = -3.05 Adc, V _{GS} = 0 V, T _J = 125°C)	V _{SD}	- -	-0.96 -0.78	-1.25 -	Vdc
Reverse Recovery Time	(I _S = -3.05 Adc, V _{GS} = 0 Vdc, di/dt = 100 A/ μ s)	t _{rr}	-	34	-	ns
		t _a	-	18	-	
		t _b	-	16	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.03	-	μ C

5. Handling precautions to protect against electrostatic discharge is mandatory.

6. Indicates Pulse Test: Pulse Width = 300 μ s max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

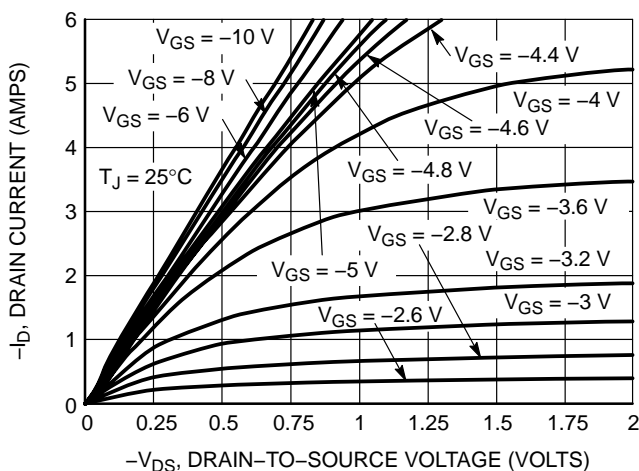


Figure 1. On-Region Characteristics

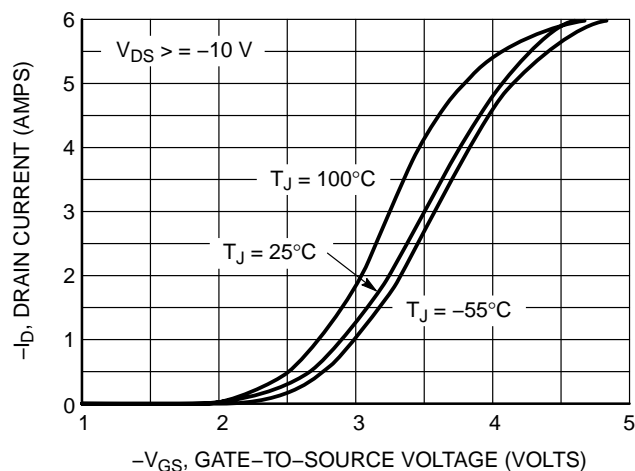


Figure 2. Transfer Characteristics

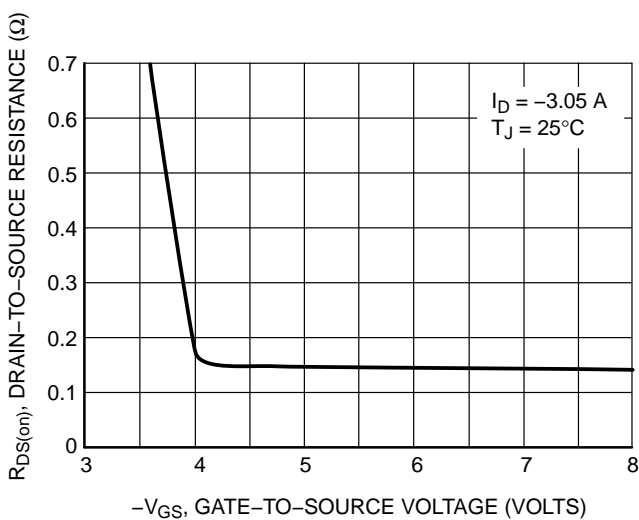


Figure 3. On-Resistance vs. Gate-to-Source Voltage

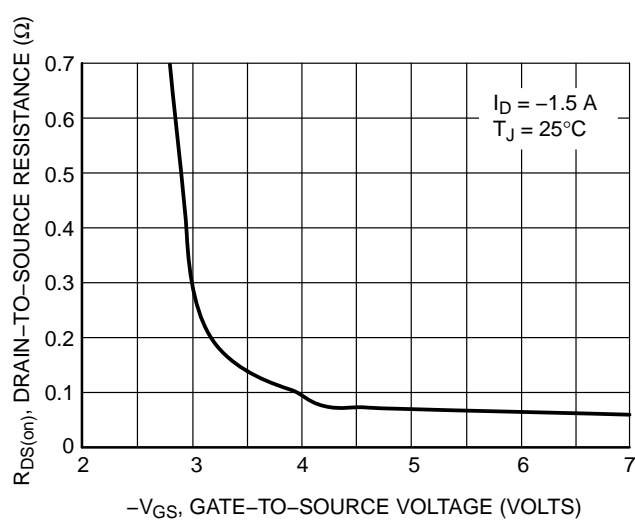


Figure 4. On-Resistance vs. Gate-to-Source Voltage

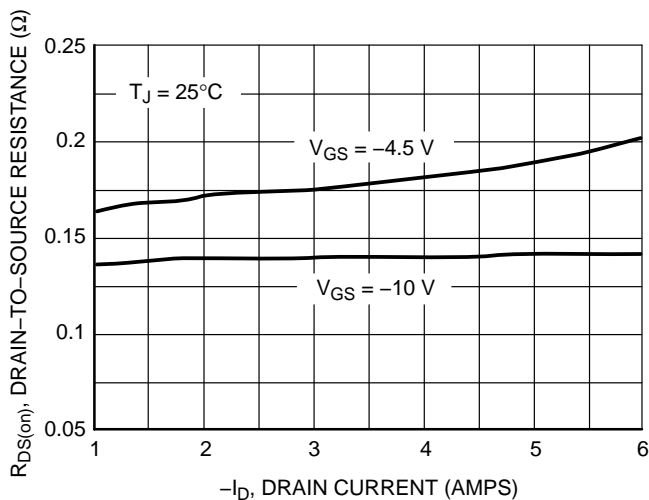


Figure 5. On-Resistance vs. Drain Current and Gate Voltage

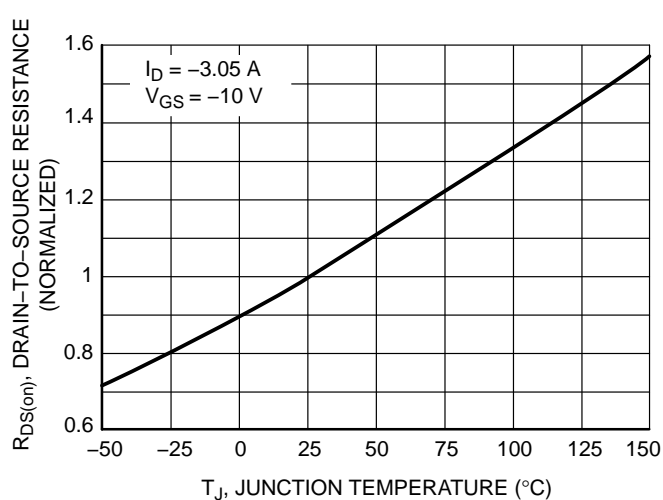


Figure 6. On Resistance Variation with Temperature

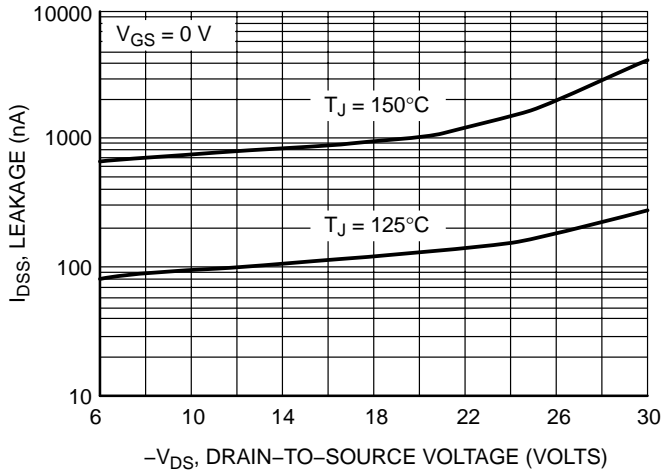


Figure 7. Drain-to-Source Leakage Current vs. Voltage

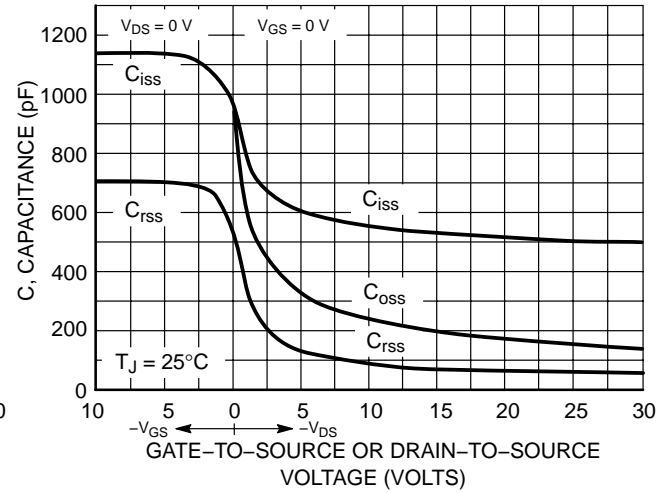


Figure 8. Capacitance Variation

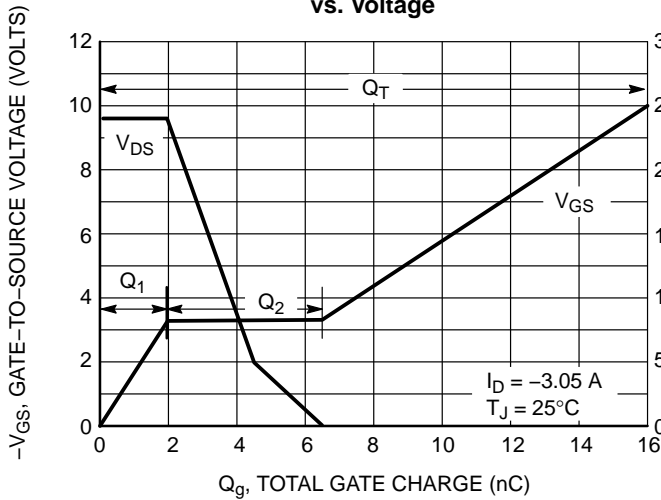


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

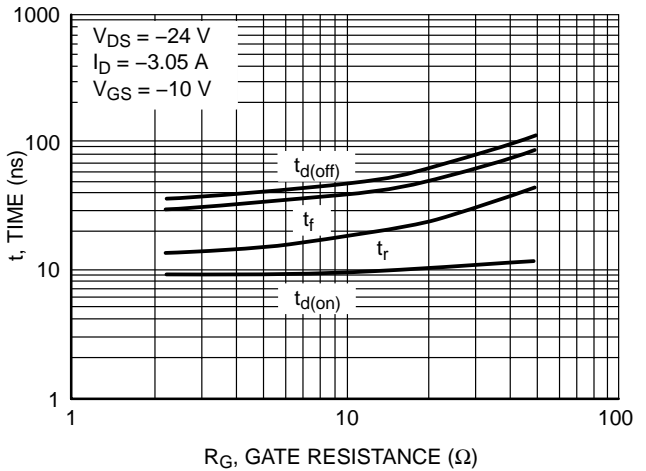


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

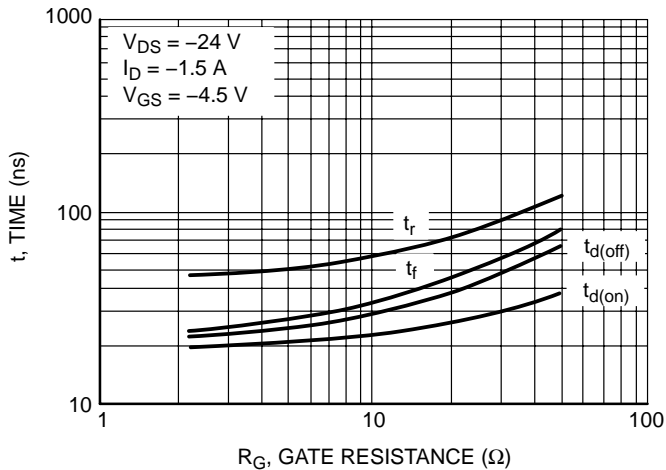


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

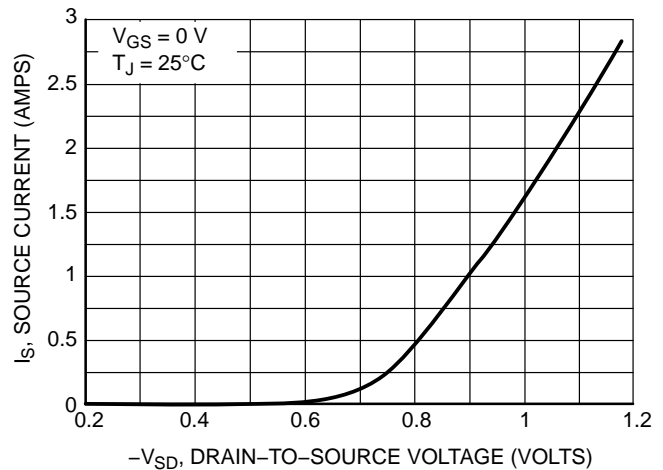


Figure 12. Diode Forward Voltage vs. Current

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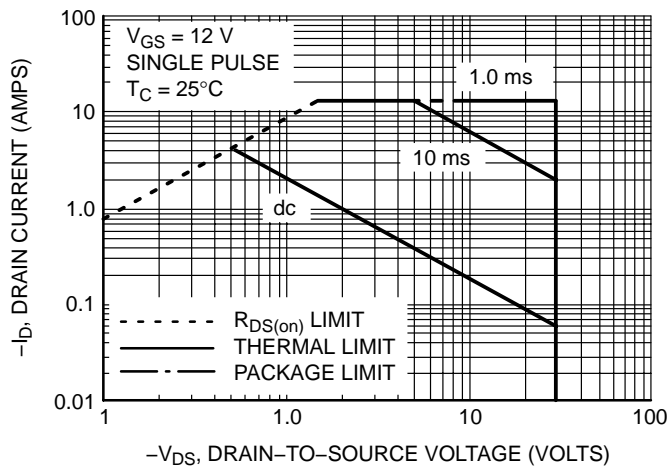


Figure 13. Maximum Rated Forward Biased Safe Operating Area

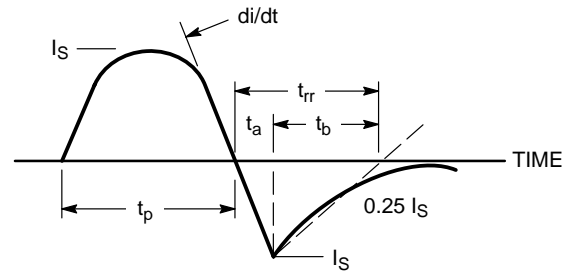


Figure 14. Diode Reverse Recovery Waveform

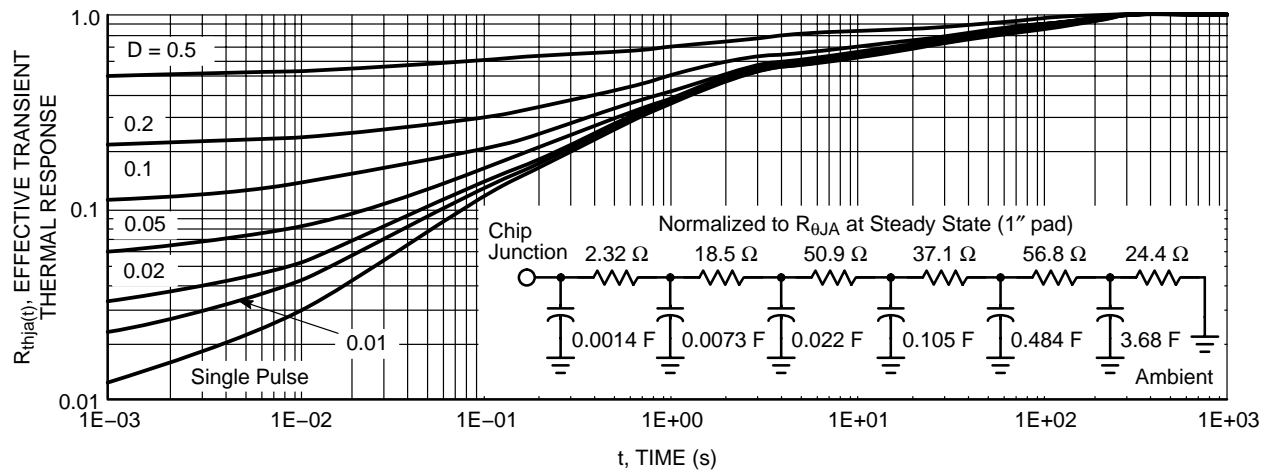
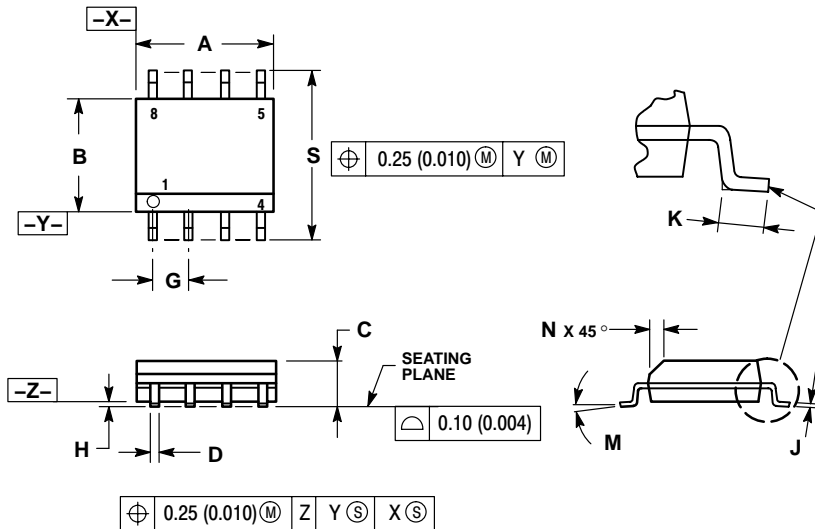


Figure 15. FET Thermal Response

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PACKAGE DIMENSIONS

SO-8
CASE 751-07
ISSUE AB



NOTES:

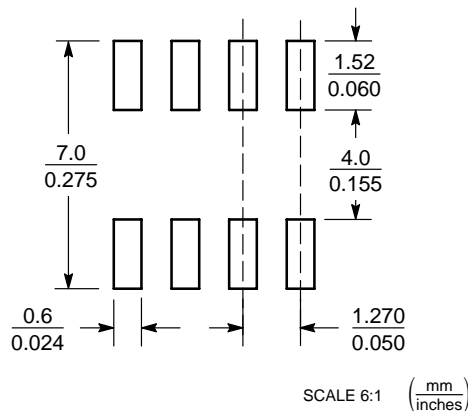
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:

- PIN 1. SOURCE 1
- GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- DRAIN 2
- DRAIN 1
- DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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