



CYPRESS

B9946

# 3.3V, 160-MHz, 1:10 Clock Distribution Buffer

## Product Features

- 160-MHz Clock Support
- LVC MOS/LVTTL Compatible Inputs
- 10 Clock Outputs: Drive up to 20 Clock Lines
- 1X or 1/2X Configurable Outputs
- Output Three-state Control
- 250 ps Maximum Output-to-Output Skew
- Pin Compatible with MPC946
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

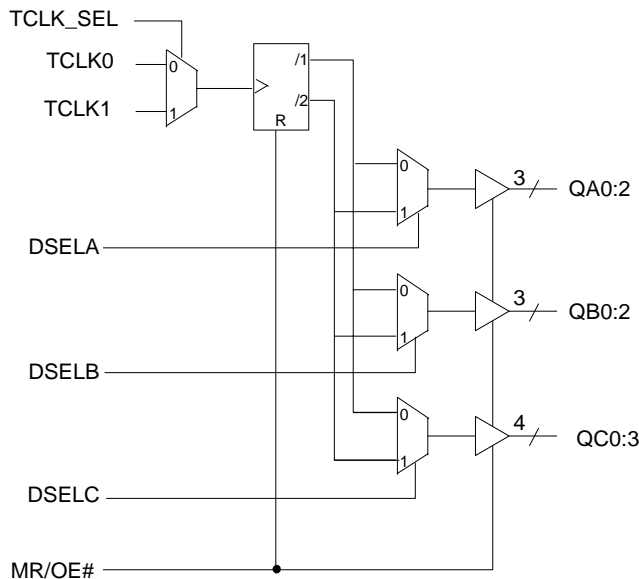
## Description

The B9946 is a low-voltage clock distribution buffer with the capability to select one of two LVC MOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVC MOS/LVTTL compatible. The 10 outputs are 3.3V LVC MOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9946 has an effective fanout of 1:20.

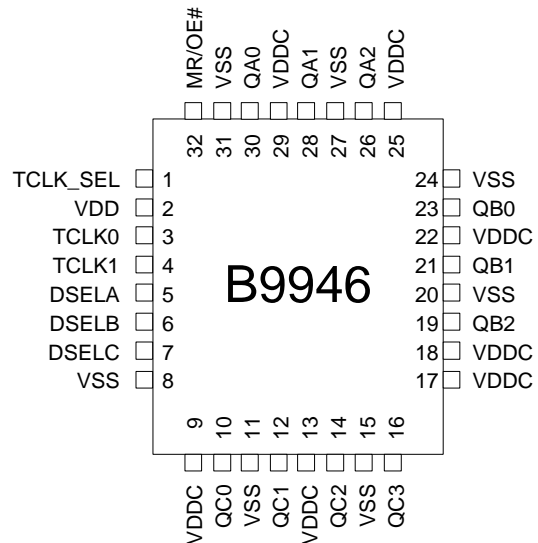
The B9946 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1X to 1/2X outputs.

The B9946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

## Block Diagram



## Pin Configuration



**Pin Description<sup>[1]</sup>**

Pin	Name	PWR	I/O	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	Divider Select Inputs. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated.
9, 13, 17, 18, 22, 25, 29	VDDC			3.3V Power Supply for Output Clock Buffers
2	VDD			3.3V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

**Note:**

1. PD = Internal Pull-Down, PU = Internal Pull-Up.

**Maximum Ratings<sup>[2]</sup>**

Maximum Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Maximum Input Voltage Relative to  $V_{DD}$ : .....  $V_{DD} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $-40^{\circ}C$  to  $+85^{\circ}C$   
 Maximum ESD Protection ..... 2 KV  
 Maximum Power Supply: ..... 5.5V  
 Maximum Input Current: .....  $\pm 20$  mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

**DC Parameters:**  $V_{DDC} = 3.3V \pm 10\%$ ,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

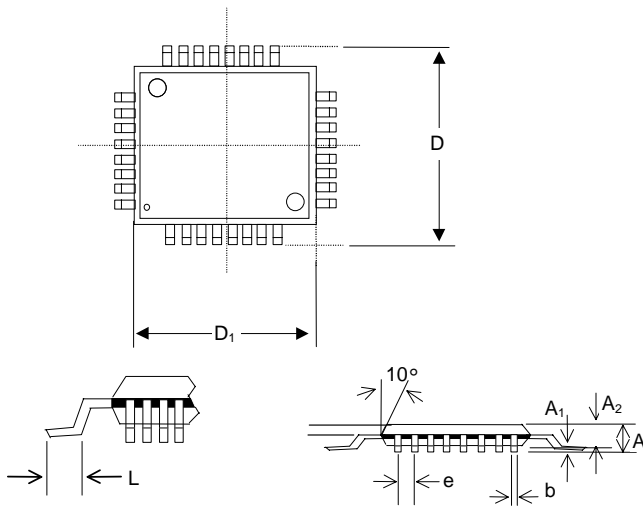
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input Low Voltage		$V_{SS}$		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD}$	V
$I_{IL}$	Input Low Current (@ $V_{IL} = V_{SS}$ )	Note 3			-100	$\mu A$
$I_{IH}$	Input High Current (@ $V_{IL} = V_{DD}$ )				100	$\mu A$
$V_{OL}$	Output Low Voltage	$I_{OL} = 20$ mA, Note 4			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -20$ mA, $V_{DDC} = 3.3V$ , Note 4	2.5			V
$I_{DD}$	Quiescent Supply Current	All $V_{DDC}$ and $V_{DD}$	-	1	2	mA
$C^{in}$	Input Capacitance		-	-	4	pF

**AC Parameters<sup>[5]</sup>:**  $V_{DDC} = 3.3V \pm 10\%$ ,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Maximum Input Frequency <sup>[6]</sup>		160			MHz
Tpd	TTL_CLK to Q Delay <sup>[6]</sup>		5.0	-	11.5	ns
FoutDC	Output Duty Cycle <sup>[6,7]</sup>	Measured at $V_{DDC}/2$	TCYCLE/2 - 1		TCYCLE/2 + 1	ns
tpZL, tpZH	Output enable time (all outputs)		2		10	ns
tpLZ, tpHZ	Output disable time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew <sup>[6,8]</sup>				250	ps
Tskew(pp)	Part-to-Part Skew <sup>[9]</sup>			2.0	4.5	ns
Tr/Tf	Output Clocks Rise/Fall Time <sup>[8]</sup>	0.8V to 2.0V	0.10		1.0	ns

**Notes:**

2. The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. Driving series or parallel terminated  $50\Omega$  (or  $50\Omega$  to  $V_{DD}/2$ ) transmission lines.
5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving  $50\Omega$  transmission lines.
7. 50% input duty cycle.
8. Outputs loaded with 30 pF each
9. Part-to-Part skew at a given temperature and voltage.

**Package Drawing and Dimensions**

**32-Pin TQFP Outline Dimensions**

Symbol	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A <sub>1</sub>	0.002	-	0.006	0.05	-	0.15
A <sub>2</sub>	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D <sub>1</sub>	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	0	0.75

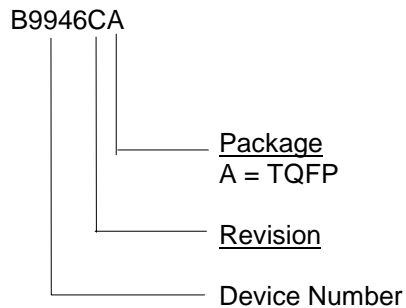
**Ordering Information**

Part Number <sup>[10]</sup>	Package Type	Production Flow
B9946CA	32-Pin TQFP	Industrial, -40°C to +85°C

**Note:**

10. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

**Marking:** Example: Cypress  
 B9946CA  
 Date Code, Lot #



<b>Document Title: B9946 3.3V, 160-MHz, 1:10 Clock Distribution Buffer</b>				
<b>Document Number: 38-07077</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	107113	06/06/01	IKA	Convert from IMI to Cypress
*A	108057	07/03/01	NDP	Changed Commercial to Industrial (See page 4)
*B	109803	01/31/02	DSG	Convert from Word to Frame
*C	122762	12/22/02	RBI	Add power up requirements to maximum ratings information