

Integrated  
Circuit  
Systems, Inc.

# PRELIMINARY

## ICS853016

LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

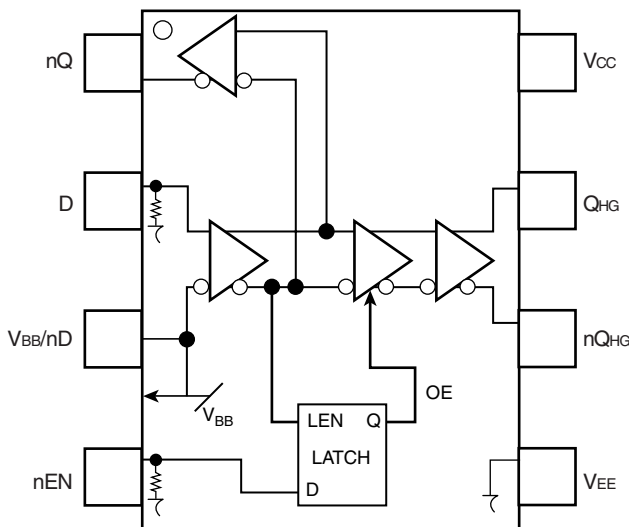
### GENERAL DESCRIPTION

The ICS853016 is a low skew, high performance 1-to-2 Differential-to-3.3V, 5V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853016 is characterized to operate from either a 3.3V or a 5V power supply. Guaranteed duty cycle skew characteristic makes the ICS853016 ideal for those clock distribution applications demanding well defined performance and repeatability.

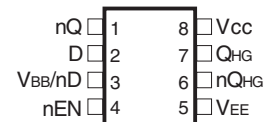
### FEATURES

- (1) Differential 3.3V, 5V LVPECL / ECL output pair and (1) Single-ended 3.3V, 5V LVPECL / ECL output
- (1) Differential D, nD input pair
- D, nD pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >3GHz (typical)
- Translates any single ended input signal to 3.3V to 5V LVPECL levels with resistor bias on nD input
- Duty cycle skew: 10ps (typical)
- Propagation delay: 400ps (typical)
- LVPECL mode operating voltage supply range:  $V_{CC} = 3.0V$  to  $5.5V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -5.5V$  to  $-3.0V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Pin compatible with MC100EP16VCD and MC100EP16VCDT

### BLOCK DIAGRAM



### PIN ASSIGNMENT



#### ICS853016

8-Lead SOIC

3.90mm x 4.90mm x 1.37mm package body

**M Package**

Top View

#### ICS853016

8-Lead TSSOP, 118mil

3mm x 3mm x 0.95mm package body

**G Package**

Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



Integrated  
Circuit  
Systems, Inc.

# PRELIMINARY

## ICS853016

LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	nQ	Output		Single-ended clock output. LVPECL interface levels.
2	D	Input	Pulldown	Non-inverting differential clock input. LVPECL interface levels.
3	$V_{BB}/nD$	Input		Reference voltage output/Inverting differential clock input. LVPECL interface levels.
4	nEN	Input	Pulldown	Enable input. Default LOW when left open. LVCMOS/LVTTL interface levels.
5	$V_{EE}$	Power		Negative supply pin.
6, 7	$nQ_{HG}, Q_{HG}$	Output		Differential clock outputs. LVPECL interface levels.
8	$V_{CC}$	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		$K\Omega$



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	6V (LVPECL mode, $V_{EE} = 0$ )
Negative Supply Voltage, $V_{EE}$	-6V (ECL mode, $V_{CC} = 0$ )
Inputs, $V_I$ (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, $V_I$ (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
$V_{BB}$ Sink/Source, $I_{BB}$	$\pm 0.5mA$
Operating Temperature Range, $T_A$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$	112.7°C/W (0 lfpm)
(Junction-to-Ambient) for 8 Lead SOIC	
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 m/s)
(Junction-to-Ambient) for 8 Lead TSSOP	

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.0V$  TO  $5.5V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.0	3.3	5.5	V
$I_{EE}$	Power Supply Current			30		mA

**TABLE 3B. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1	2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
$V_{OL}$	Output Low Voltage; NOTE 1	1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
$V_{IH}$	Input High Voltage (Single-Ended)	2.075		2.36	2.075		2.36	2.075		2.36	V
$V_{IL}$	Input Low Voltage (Single-Ended)	1.43		1.765	1.43		1.765	1.43		1.765	V
$V_{BB}$	Output Voltage Reference; NOTE 2	1.86		1.98	1.86		1.98	1.86		1.98	V
$V_{PP}$	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	mV
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 3, 4	1.2		3.3	1.2		3.3	1.2		3.3	V
$I_{IH}$	Input High Current	D		150	D		150	D		150	$\mu A$
$I_{IL}$	Input Low Current	D		-10	D		-10	D		-10	$\mu A$

Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to  $V_{CC} - 2V$ .

NOTE 2: Single-ended input operation is limited.  $V_{CC} \geq 3V$  in LVPECL mode.

NOTE 3: Common mode voltage is defined as  $V_{IH}$ .

NOTE 4: For single-ended applications, the maximum input voltage for D is  $V_{CC} + 0.3V$ .



**TABLE 3C. LVPECL DC CHARACTERISTICS,  $V_{CC} = 5.0V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1	3.875	3.975	4.08	3.925	3.995	4.07	3.995	4.03	4.065	V
$V_{OL}$	Output Low Voltage; NOTE 1	3.105	3.245	3.38	3.125	3.22	3.315	3.14	3.235	3.33	V
$V_{IH}$	Input High Voltage (Single-Ended)	3.775		4.06	3.775		4.06	3.775		4.06	V
$V_{IL}$	Input Low Voltage (Single-Ended)	3.13		3.465	3.13		3.465	3.13		3.465	V
$V_{BB}$	Output Voltage Reference; NOTE 2	3.56		3.68	3.56		3.68	3.56		3.68	V
$V_{PP}$	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	mV
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 3, 4	1.2		5	1.2		5	1.2		5	V
$I_{IH}$	Input High Current	D		150	150		150		150		$\mu A$
$I_{IL}$	Input Low Current	D		-10	-10		-10		-10		$\mu A$

Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Single-ended input operation is limited.  $V_{CC} \geq 3V$  in LVPECL mode.

NOTE 3: Common mode voltage is defined as  $V_{IH}$ .

NOTE 4: For single-ended applications, the maximum input voltage for D is  $V_{CC} + 0.3V$ .

**TABLE 3D. ECL DC CHARACTERISTICS,  $V_{CC} = 0V$ ;  $V_{EE} = -5.5V$  TO  $-3.0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1	-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
$V_{OL}$	Output Low Voltage; NOTE 1	-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
$V_{IH}$	Input High Voltage(Single-Ended)	-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
$V_{IL}$	Input Low Voltage(Single-Ended)	-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
$V_{BB}$	Output Voltage Reference; NOTE 2	-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
$V_{PP}$	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	mV
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 3, 4	$V_{EE}+1.2V$		0	$V_{EE}+1.2V$		0	$V_{EE}+1.2V$		0	V
$I_{IH}$	Input High Current	D		150	150		150		150		$\mu A$
$I_{IL}$	Input Low Current	D		-10	-10		-10		-10		$\mu A$

Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Single-ended input operation is limited.  $V_{CC} \geq 3V$  in LVPECL mode.

NOTE 3: Common mode voltage is defined as  $V_{IH}$ .

NOTE 4: For single-ended applications, the maximum input voltage for D is  $V_{CC} + 0.3V$ .



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

**ICS853016**

LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

**TABLE 4. AC CHARACTERISTICS,  $V_{CC} = 0V$ ;  $V_{EE} = -5.5V$  TO  $-3.0V$  OR  $V_{CC} = 3.0V$  TO  $5.5V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Output Frequency		TBD			>3			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay; NOTE 1	(Differential) nQ		TBD		350			TBD		ps
		(Differential) $Q_{HG}$ , $nQ_{HG}$		TBD		400			TBD		ps
		(Single-Ended) nQ		TBD		400			TBD		ps
		(Single-Ended) $Q_{HG}$ , $nQ_{HG}$		TBD		450			TBD		ps
$t_{sk}(odc)$	Duty Cycle Skew; NOTE 2, 3		TBD			10			TBD		ps
$t_R/t_F$	Output Rise/ Fall Time 20% to 80%	nQ		TBD		300			TBD		ps
		$Q_{HG}$ , $nQ_{HG}$		TBD		150			TBD		ps

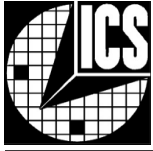
All parameters are measured at  $f \leq 1.7GHz$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured for only differential operation from the cross point of the inputs to the cross point of the outputs.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



Integrated  
Circuit  
Systems, Inc.

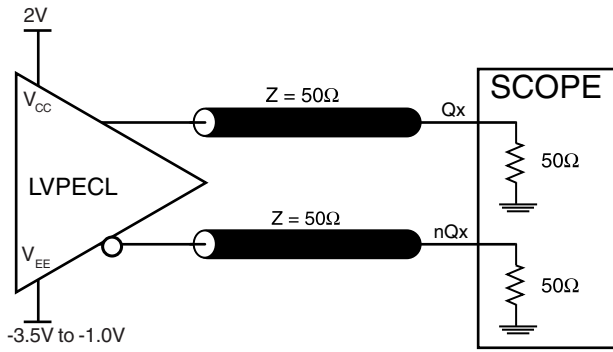
**PRELIMINARY**

**ICS853016**

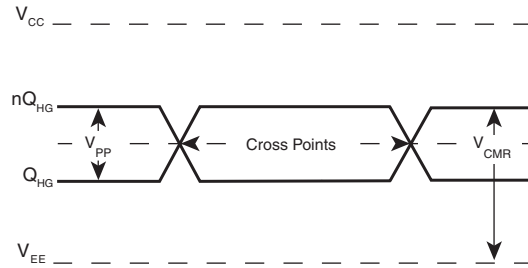
LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

**PARAMETER MEASUREMENT INFORMATION**



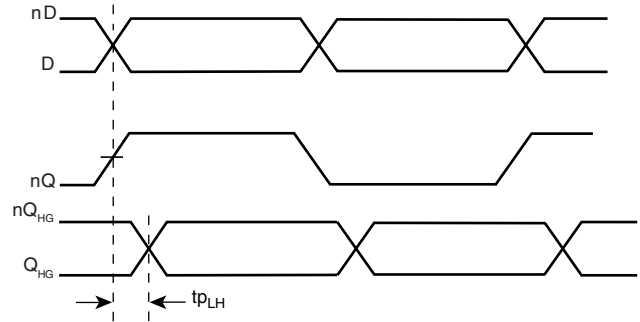
**OUTPUT LOAD AC TEST CIRCUIT**



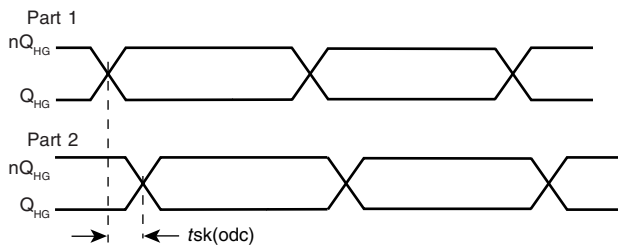
**DIFFERENTIAL INPUT LEVEL**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



**DUTY CYCLE SKEW**



## APPLICATION INFORMATION

### WIRING THE INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1 shows an example of the input that can be wired to accept single ended LVPECL levels.

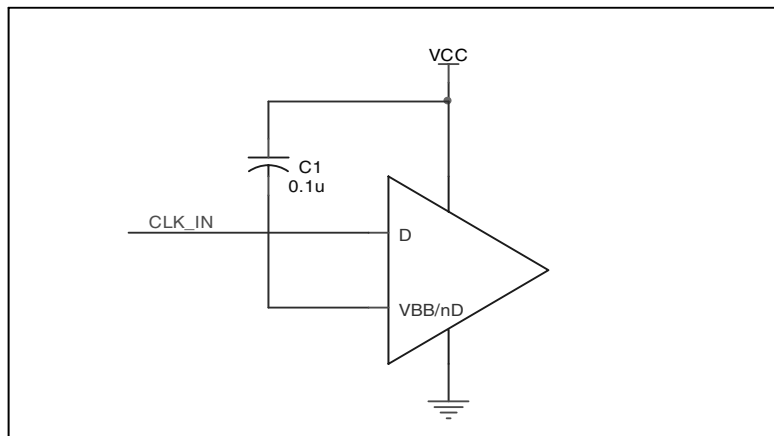


FIGURE 1. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

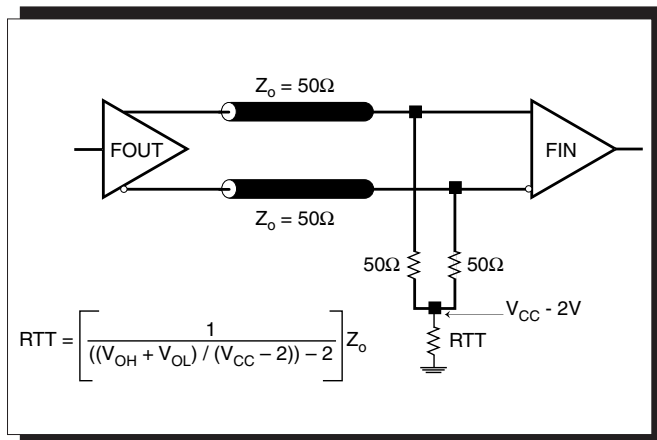


**TERMINATION FOR 3.3V LVPECL OUTPUTS**

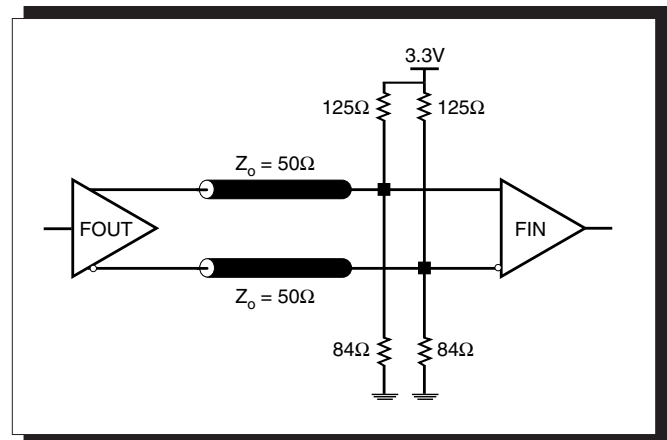
The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



**FIGURE 2A. LVPECL OUTPUT TERMINATION**

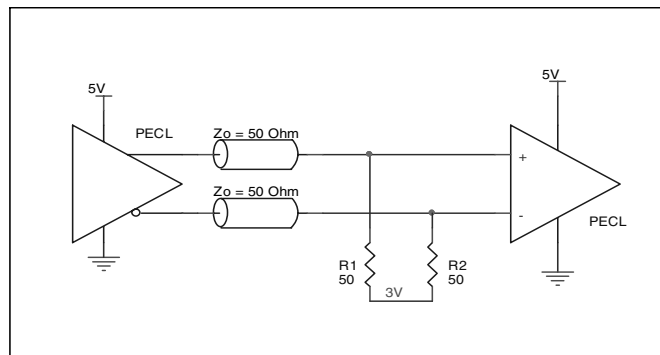


**FIGURE 2B. LVPECL OUTPUT TERMINATION**

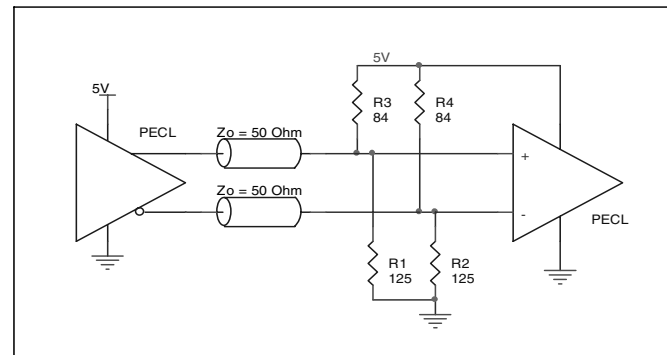
**TERMINATION FOR 5V LVPECL OUTPUT**

This section shows examples of 5V LVPECL output termination. *Figure 3A* shows standard termination for 5V LVPECL. The termination requires matched load of 50Ω resistors pull down to

$V_{CC} - 2V = 3V$  at the receiver. *Figure 3B* shows Thevenin equivalence of *Figure 3A*. In actual application where the 3V DC power supply is not available, this approach is normally used.

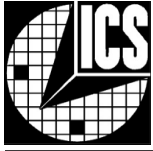


**FIGURE 3A. STANDARD 5V PECL OUTPUT TERMINATION**



**FIGURE 3B. 5V PECL OUTPUT TERMINATION EXAMPLE**





## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853016. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS853016 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 5.5V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 5.5V * 30mA = 165mW$
- Power (outputs)<sub>MAX</sub> = **30.94mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30.94mW = 61.88mW$

**Total Power**<sub>MAX</sub> (3.8V, with all outputs switching) =  $165mW + 61.88mW = 226.88mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5A below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.227W * 103.3^\circ C/W = 108.4^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 5A. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

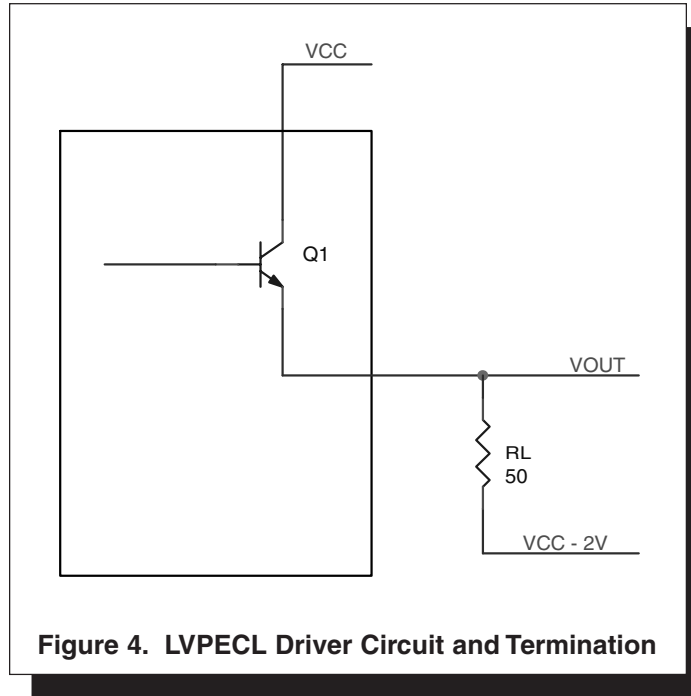
**TABLE 5B. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 4.



**Figure 4. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.935V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.67V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.67V$$

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 30.94mW$



Integrated  
Circuit  
Systems, Inc.

# PRELIMINARY

## ICS853016

LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

### RELIABILITY INFORMATION

**TABLE 6A.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD SOIC**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TABLE 6B.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD TSSOP**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

#### TRANSISTOR COUNT

The transistor count for ICS853016 is: 163



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

**ICS853016**

LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

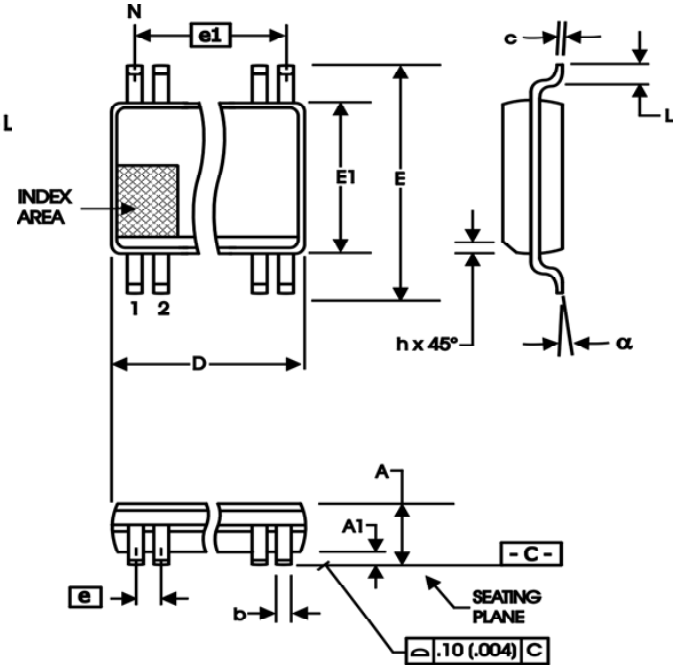
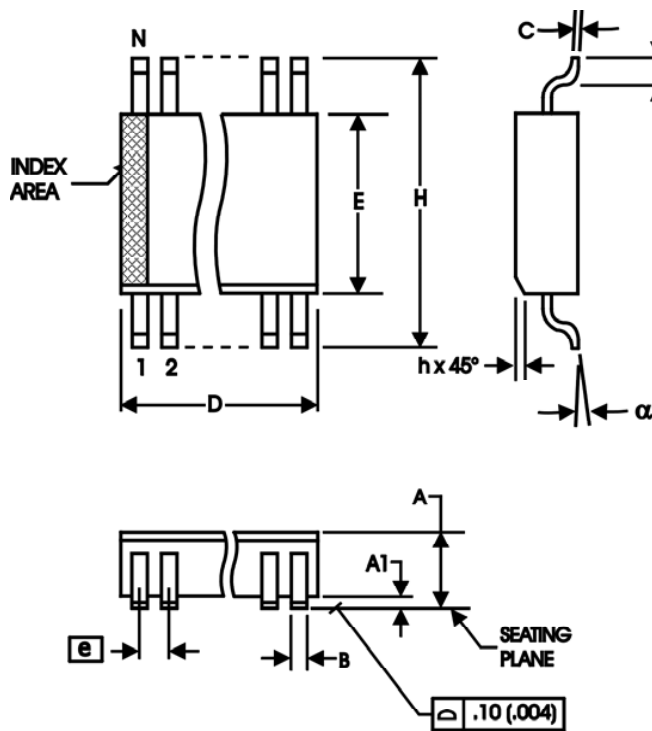


TABLE 7A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
e	0.65 BASIC	
e1	1.95 BASIC	
L	0.40	0.80
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-187



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

**ICS853016**

LOW SKEW, 1-TO-2

DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL FANOUT BUFFER

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS853016AM	853016A	8 lead SOIC	96 per tube	-40°C to 85°C
ICS853016AMT	853016A	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C
ICS853016AG	016A	8 lead TSSOP	100 per tube	-40°C to 85°C
ICS853016AGT	016A	8 lead TSSOP on Tape and Reel	2500	-40°C to 85°C

The aforementioned trademark, HiPerClockS™ is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.