Design of Power Factor Correction Circuit Using Greenline™ Compact Power Factor Controller MC33260

ON Semiconductor®
http://onsemi.com

APPLICATION NOTE

Prepared by
Ming Hian Chew
ON Semiconductor Analog Applications Engineering

Introduction

The MC33260 is an active power factor controller that functions as a boost pre–converter which, meeting international standard requirement in electronic ballast and off–line power supply application. MC33260 is designed to drive a free running frequency discontinuous mode, it can also be synchronized and in any case, it features very effective protections that ensure a safe and reliable operation.

This circuit is also optimized to offer extremely compact and cost effective PFC solutions. It does not entail the need of auxiliary winding for zero current detection hence a simple coil can be used instead of a transformer if the MC33260 Vcc is drawn from the load (please refer to page 19 of the data sheet). While it requires a minimum number of external components, the MC33260 can control the follower boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered.

Also able to function in a traditional way (constant output voltage regulation level), any intermediary solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

This application note will discuss on the design of power factor correction circuit with MC33260 with traditional boost constant output voltage regulation level operation and follower boost variable output voltage regulation level operation. For derivation of the design equations related to the IC please refer to MC33260 data sheet.

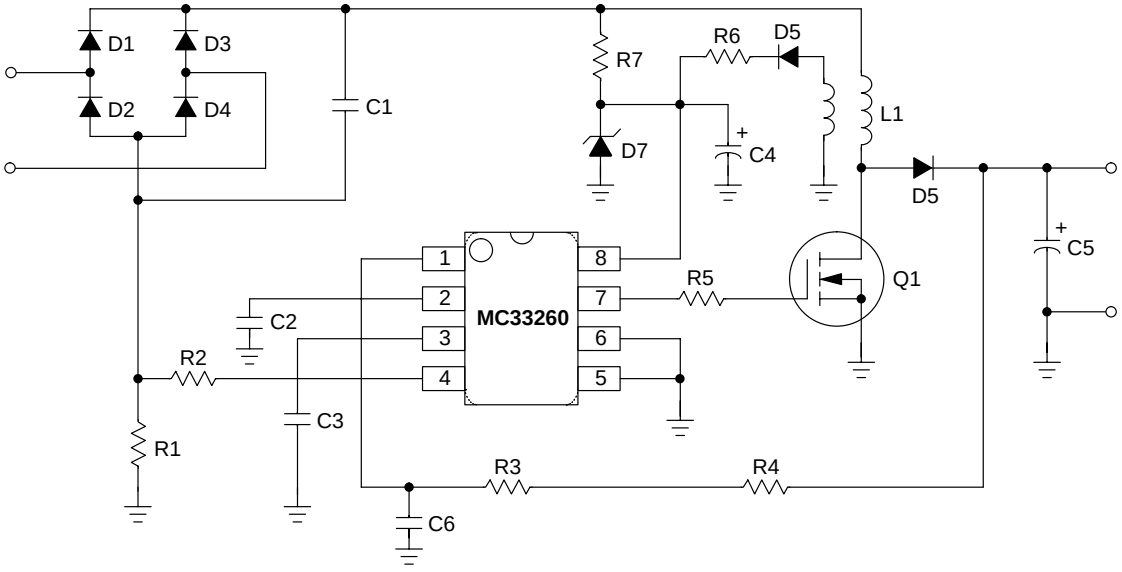

Figure 1. Application Schematic of MC33260

PFC Techniques

Many PFC techniques have been proposed, boost topology, which can operate in continuous and discontinuous mode, is the most popular. Typically, continuous mode is more favorable for high power application for having lower peak current. On the other hand, for less than 500 W application, discontinuous mode offers smaller inductor size, minimal parts count and lowest cost. This paper will discuss design of PFC with MC33260, which operates in critical conduction mode.

Discontinuous Conduction Mode Operation

Critical conduction mode operation presents two major advantages in PFC application. For critical conduction mode, the inductor current must fall to zero before start the next cycle. This operation results in higher efficiency and

June, 2002 – Rev. 1
Publication Order Number:
AND8016/D

eliminates boost rectifier reverse recovery loss as MOSFET cannot turn–on until the inductor current reaches zero.

Secondly, since there are no dead–time gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current. The converter works right on critical conduction mode, which results in variable frequency operation.

Inductor Waveform

$$\frac{V}{L} = \frac{di}{dt} \quad (1)$$

Equation (1) is the center of the operation of PFC boost converter where $V=V_{in}(t)$, the instantaneous voltage across the inductor. Assuming the inductance and the on–time over each line half–cycle are constant, di is actually the peak current, I_{Lpk}, this is because the inductor always begins charging at zero current.

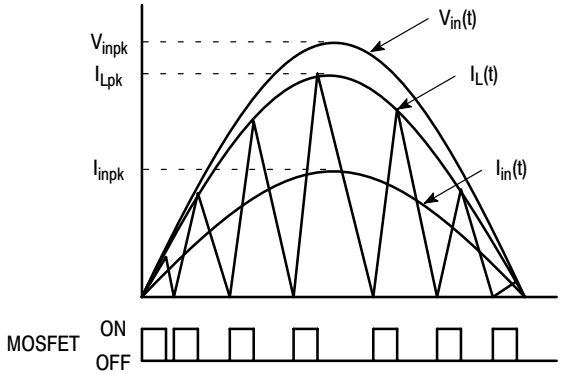

Figure 2. Inductor Waveform

Design Criteria

The basic design specification concerns the following:

- Mains Voltage Range: $V_{ac(LL)} - V_{ac(HL)}$
- Regulated DC Output Voltage: V_o
- Rated Output Power: P_o
- Expected Efficiency, η

PFC Power Section Design

Instantaneous Input Voltage, $V_{in}(t)$

Peak Input Voltage, V_{inpk}

Both $V_{in}(t)$ and V_{inpk} are related by below equation

$$V_{in}(t) = V_{inpk}\sin(\omega t) \quad (2)$$

$$\text{where} \quad V_{inpk} = \sqrt{2}\,V_{inrms} \quad (3)$$

Instantaneous Input Current, $I_{in}(t)$

Peak Input Current, I_{inpk},

Both $I_{in}(t)$ and I_{inpk} are related by below equation

$$I_{in}(t) = I_{inpk}\sin(\omega t), \quad (4)$$

$$\text{where} \quad I_{inpk} = \sqrt{2}\,I_{inrms} \quad (5)$$

Input power of the PFC circuit, P_{in} can be expressed in following equation, by substituting equation (3) and (5).

$$P_{in} = V_{inrms}I_{inrms} = \frac{V_{inpk}}{\sqrt{2}} \cdot \frac{I_{inpk}}{\sqrt{2}} = \frac{V_{inpk}I_{inpk}}{2} \quad (6)$$

The output power, P_o is given by:

$$P_o = V_oI_o = \eta P_{in} \quad (7)$$

PFC circuit efficiency is needed in the design equation, for low line operation, it is typically set at 92% while 95% for high line operation. Substituting equation (6) into equation (7),

$$P_o = \eta P_{in} = \eta\,\frac{V_{inpk}I_{inpk}}{2} \quad (8)$$

Express the above equation in term of I_{inpk},

$$I_{inpk} = \frac{2P_o}{\eta V_{inpk}} = \frac{\sqrt{2}\,P_o}{\eta V_{inrms}} \quad (9)$$

The average input current is equal to average inductor current, $I_{L(avg)}$,

$$I_{L(avg)} = I_{in} \quad (10)$$

It has been understood that peak inductor current, I_{Lpk} is exactly twice the average inductor current, $I_{L(avg)}$ for critical conduction operation.

$$I_{Lpk} = 2I_{L(avg)} = \frac{2\sqrt{2}\,P_o}{\eta V_{inrms}} \quad (11)$$

Since I_{Lpk} is maximum at minimum required ac line voltage, $V_{ac(LL)}$,

$$I_{Lpk} = \frac{2\sqrt{2}\,P_o}{\eta V_{ac(LL)}} \quad (12)$$

Switching Time

In theory, the on–time, $t_{(on)}$ is constant. In practice, $t_{(on)}$ tends to increase at the ac line zero crossings due to the charge on output capacitor C_{out}. Let $V_{ac} = V_{ac(LL)}$ for initial $t_{(on)}$ and $t_{(off)}$ calculations.

On–time

By solving inductor equation (1), on–time required to charge the inductor to the correct peak current is:

$$t_{(on)} = I_{Lpk}\frac{L_P}{Vinpk} \quad (13)$$

Substituting equation (3) and (12) into equation (13), results in:

$$t_{(on)} = \frac{2\sqrt{2}\,P_o}{\eta V_{ac(LL)}} \cdot \frac{L_P}{\sqrt{2}\,V_{ac(LL)}} = \frac{2P_oL_P}{\eta V^2_{ac(LL)}} \quad (14)$$

Off–time

The instantaneous switch off–time varies with the line and load conditions, as well as with the instantaneous line voltage. Off–time is analyzed by solving equation (1) for the inductor discharging where the voltage across the inductor is V_o minus V_{in}.

$$t_{(off)} = \frac{I_{Lpk} L_P}{V_o - V_{inpk} \sin(\omega t)} \quad (15)$$

Multiplying nominator and denominator with $V_{inpk}\sin\omega(t)$ results in:

$$t_{(off)} = \frac{\frac{I_{Lpk} L_P}{V_{inpk} \sin(\omega t)}}{\frac{V_o - V_{inpk} \sin(\omega t)}{V_{inpk} \sin(\omega t)}} = \frac{t_{(on)}}{\frac{V_o}{\sqrt{2}\, Vinpk |\sin(\theta)|} - 1} \quad (16)$$

where $\omega t = \theta$

The off–time, $t_{(off)}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.

The off–time is at a minimum at ac line crossings. This equation is used to calculate $t_{(off)}$ as Theta approaches zero.

$$t_{(off)min} = \frac{I_{Lpk} L_P}{V_o}, \theta = 0^\circ \quad (17)$$

Switching Frequency

$$f = \frac{1}{t_{(on)} + t_{(off)}} \quad (18)$$

Switching frequency changes with the steady state line and load operating conditions along with the instantaneous input line voltage. Typically, the PFC converter is designed to operate above the audible range after accommodating all circuit and component tolerances. 25 kHz is a good first approximation. Higher frequency operation that can significantly reduce the inductor size without negatively impacting efficiency or cost should also be evaluated.

The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $t_{(off)}$ approaches zero producing an increase in switching frequency.

Inductor Value

Maximum on–time needs to be programmed into the PFC controller timing circuit. Both $t_{(on)max}$ and $t_{(off)max}$ will be individually calculated and added together to obtain the maximum conversion period, t_{total}. This is required to obtain the inductor value.

$$t_{(on)max} = \frac{2 P_o L_P}{\eta V^2_{ac(LL)}} \quad (19)$$

$$t_{(off)max} = \frac{I_{Lpk} L_P}{V_o - V_{inpk}}, (\theta) \approx 90^\circ \quad (20)$$

The exact inductor value can be determined by solving equation (21) by substituting equation (19) and (20) at the selected minimum operating frequency.

$$t_{total} = t_{(on)max} + t_{(off)max} \quad (21)$$

Equation (21) becomes

$$t_{total} = \frac{\sqrt{2} P_o L_P V_o}{V^2_{ac(LL)} \eta \left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right)} \quad (22)$$

By rearranging in term of L_p,

$$L_p = \frac{t_{total}\left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right) \eta V^2_{ac(LL)}}{\sqrt{2} V_o P_o} \quad (23)$$

Equation (23) can be rewritten by substituting rearranged equation (12) in term of $\sqrt{2}P_o$.

$$L_p = \frac{2 \times t_{total}\left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right) V_{ac(LL)}}{V_o I_{Lpk}} \quad (24)$$

Let the switching cycle t = 40μs for universal input (85 to 265 V_{ac}) operation and 20 μs for fixed input (92 to 138 V_{ac}, or 184 to 276 V_{ac}) operation.

Inductor Design Summary

The required energy storage of the boost inductor is:

$$W_L = \frac{1}{2} L_P I^2_{Lpk} \quad (25)$$

The number of turns required for a selected core size and material is:

$$N_P = \frac{L_P I_{Lpk} 10^6}{B_{max} A_e} \quad (26)$$

where B_{max} is in Teslas and A_e is in square millimeters (mm^2)

The required air gap to achieve the correct inductance and storage is expressed by:

$$l_{gap} = \frac{4\pi 10^{-7} N^2_p A_e}{L_P} \text{ mm} \quad (27)$$

Design of Auxiliary Winding

MC33260 does not entail an auxiliary winding for zero current detection. Hence if DC voltage can be tapped from the SMPS or electronic ballast connected to the output of PFC, this step can be skipped. Then an inductor is what it needs.

The auxiliary winding exhibits a low frequency ripple (100–120 Hz). The Vcc capacitor must be large enough (about 47 μF) to minimize voltage variations. As a rule of thumb, you can use the below equation to estimate the auxiliary turn number:

$$N_{aux} = \frac{N_p \cdot V_{aux}}{V_L} = \frac{N_p \cdot V_{aux}}{V_o - V_{ac(HL)}} \quad (28)$$

The MC33260 V_{CC} maximum voltage being 16 V, one must add a resistor (in the range of 22 Ω) and a 15 V zener to protect the circuit against excessive voltages. Vaux should be chosen above the Under–Voltage Lockout threshold (10 V) and below the zener voltage.

Selection of Output Capacitor

The choice of output capacitance value is dictated by the required hold–up time, t_{hold} or the acceptable output ripple voltage, V_{orip} for a given application. As a rule of thumb, can start with 1 μF/watt.

Selection of Semiconductors

Maximum currents and voltages must first be determined for over all operating conditions to select the MOSFET and boost rectifier. As a rule of thumb, derate all semiconductors to about 75–80% of their maximum ratings. This implying the need of devices with at least 500 V breakdown voltage. Bipolar transistors are an acceptable alternative to MOSFET if the switching frequency is maintained fairly low. High voltage diodes with recovery times of 200 ns, or less should be used for the boost rectifier. One series of the popular devices is the MURXXX Ultrafast Rectifier Series from ON Semiconductor.

Maximum power MOSFET conduction losses.

$$P_{(on)max} \approx \frac{1}{6} \times R_{ds(on)} \times I^2_{Lpk} \left(1 - \frac{1.2 \times V_{ac(LL)}}{V_o}\right) \quad (29)$$

Designing the Oscillator Circuit

For traditional boost operation, C_T is chosen with below equation:

$$C_T \geq \frac{2 \times K_{osc} \times L_P \times P_{in} \times V^2_o}{V^2_{ac(LL)} \times R^2_o} - C_{int} \quad (30)$$

Design of Regulation and Overvoltage Protection Circuit

The output voltage regulation level can be adjusted by R_o,

$$R_o \approx \frac{V_o}{200\ \mu A} \quad (31)$$

Designing the Current Sense Circuit

The inductor current is converted into a voltage by inserting a ground referenced resistor, R_{CS} in series with the input diode bridge. Therefore a negative voltage proportional to the inductor current is built.

The current sense resistor losses, P_{Rcs}:

$$P_{Rcs} = \frac{1}{6} \times R_{CS} \times I^2_{Lpk} \quad (32)$$

Overcurrent protection resistor, R_{OCP} can be determined with below equation:

$$R_{OCP} = \frac{R_{CS} \times I_{Lpk}}{I_{OCP}} \quad (33)$$

Current Limiting With Boost Topology Power Factor Correction Circuit

Unlike buck and flyback circuits, because there is no series switch between input and output in the boost topology, high current occurring with the start–up inrush current surge charging the bulk capacitor and fault load conditions cannot be limited or controlled without additional circuitry.

The MC33260 Zero Current Detection uses the current sensing information to prevent any power switch turn on as long as some current flows through the inductor. Then, during start–up, the power MOSFET is not allowed to turn on while in–rush current flows. Then there is no risk to have the power switch destroyed at start–up because of the in–rush current.

In the same way, in an overload case, the power MOSFET is kept off as long as there is a direct output capacitor charge current, i.e., when the input voltage is higher than the output voltage. Consequently, overload working is fully safe for the power MOSFET. This is one of the major advantages compared to MC33262 and competition.

Current Limiting for Start–up Inrush

Initially V_o is zero, when the converter is turned on, the bulk capacitor will charge resonantly to twice Vin. The voltage can be as high as 750 V if V_{in} happens to be at the peak high–line 265 V condition (375 V). The peak resonant charging current through the inductor will be many times greater than normal full load current. the inductor must be designed to be much larger and more expensive to avoid saturation. The boost shunt switch cannot do anything to prevent this and could be worse if turned on during start–up.

The inrush current and voltage overshoot during the start–up phase is intolerable. A fuse is not suitable, as it will blow each time the supply is turned on.

There are several methods that may be used to solve the start–up problem:

1. Start–up Bypass Rectifier

This is implemented by adding an additional rectifier bypassing the boost inductor. The bypass rectifier will divert the start–up inrush current away from the boost inductor as shown in Figure 3. The bulk capacitor charges through D_{bypass} to the peak AC line voltage without resonant overshoot and without excessive inductor current. D_{bypass} is

reverse–biased under normal operating conditions. If load overcurrent pulls down V_o, D_{bypass} conducts, but this is probably preferable to having the high current flowing through boost inductor.

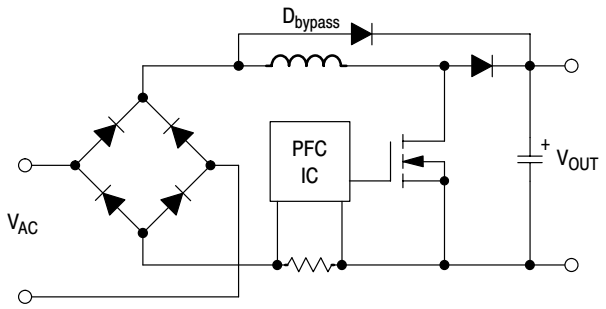

Figure 3. Rectifier bypass of start–up inrush current

2. External Inrush Current Limiting Circuit

For low power system, a thermistor in series with the pre–converter input will limit the inrush current. Concern is the thermistor may not respond fast enough to provide protection after a line dropout of a few cycles.

A series input resistor shunted by a Triac or SCR is a more efficient approach. A control circuit is necessary. This method can function on a cycle–by–cycle basis for protection after a dropout.

Load Overcurrent Limiting

If an overcurrent condition occurs and exceeds the boost converter power limit established by the control circuit, V_o will eventually be dragged down below the peak value of the AC line voltage. If this happens, current will rise rapidly and without limit through the series inductor and rectifier. This may result in saturation of the inductor and components will fail. The control circuit holds off the shunt switch, since the current limit function is activated. It cannot help to turn the switch ON – the inductor current will rise even more rapidly and switch failure will occur.

Typically, a power factor correction circuit is connected to another systems like switched mode power supply or electronic ballast. These downstream converters typically will have current limiting capability, eliminating concern about load faults. However, a downstream converter or the bulk capacitor might fail. Hence there is a possibility of a short circuit at the load.

If it is considered necessary to limit the current to a safe value in the event of a downstream fault, some means external to the boost converter must be provided.

Design Example I – Traditional Boost Constant Output Voltage Regulation Level Operation Power Factor Correction

The basic design specification concerns the following:

- Mains Voltage Range: $V_{ac(LL)} – V_{ac(HL)} = 85 – 265\ V_{ac}$
- Regulated DC Output Voltage: $V_o = 400\ V_{dc}$
- Rated Output Power: $P_o = 80$ W
- Expected Efficiency, $\eta > 90\%$

A. The input power, Pin is given by

$$P_{in} = \frac{P_o}{\eta} = \frac{80}{0.92} = 86.96\ W$$

B. Input diode current is maximum at $V_{inrms} = V_{ac(LL)}$

$$I_{inpk} = \frac{\sqrt{2}P_o}{\eta V_{ac(LL)}} = \frac{\sqrt{2} \times 80}{0.92 \times 85} = 1.447\ A$$

C. Inductor design

1. Inductor peak current:

$$I_{Lpk} = 2I_{inpk} = 2 \times 1.447 = 2.894\ A$$

2. Inductor value:

$$L_p = \frac{2 \times t_{total}\left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right)V_{ac(LL)}}{V_o I_{Lpk}}$$

$$= \frac{2 \times 40 \times 10^{-6}\left(\frac{400}{\sqrt{2}} - 85\right)85}{400 \times 2.894} = 1.162\ mH$$

Let the switching cycle t = 40 μs for universal input (85 to 265 V_{ac}) operation.

3. The number of turns required for a selected core size and material is:

$$N_P = \frac{L_P I_{Lpk} 10^6}{B_{max} A_e} = \frac{1.162 \times 10^{-3} \times 2.894 \times 10^{-6}}{0.3 \times 60}$$

$$= 186.8\ turns \approx 187\ turns$$

Using EPCOS E 30/15/7, B_{max} =0.3 T and $A_e = 60\ mm^2$.

4. The required air gap to achieve the correct inductance and storage is:

$$l_{gap} = \frac{4\pi 10^{-7} N_p^2 A_e}{L_P}$$

$$= \frac{4\pi \times 10^{-7} \times 187^2 \times 60 \times 10^{-6}}{1.162 \times 10^{-3}}$$

$$= 2.269\ mm$$

5. Design of Auxiliary Winding

$$N_{aux} = \frac{V_{aux} N_P}{\left(V_o - V_{ac(HL)}\right)} = \frac{14 \times 187}{(400 - 265)}$$

$$= 19.4\ turns \approx 20\ turns$$

Round up to 20 turns to make sure enough voltage at the auxiliary winding.

D. To determine the output capacitor

As rule of thumb, for 80 W output, start with 100 μF, 450 V capacitor.

E. Calculation of MOSFET conduction losses

A 8A, 500V MOSFET, MTP8N50E is chosen. The on resistance, $R_{ds(on)} \approx 1.75\ \Omega$@100°C. Therefore, maximum power MOSFET conduction losses is:

$$P_{(on)max} \approx \frac{1}{6} \times R_{ds(on)} \times I^2_{Lpk}\ 1 - \frac{1.2 \times V_{ac(LL)}}{V_o}$$

$$= \frac{1}{6} \times 1.75 \times 2.894^2\ 1 - \frac{1.2 \times 85}{400} = 1.82\ W$$

F. Design of regulation and overvoltage protection circuit

The output voltage regulation level can be adjusted by R_o,

$$R_o \approx \frac{V_o}{200\ \mu A} = \frac{400}{200\ \mu A} = 2\ M\Omega$$

Use two 1 MΩ resistors in series.

G. Designing the oscillator circuit

For traditional boost operation, C_T is chosen with below equation:

$$C_T \geq \frac{2 \times K_{osc} \times L_P \times P_{in} \times V^2_o}{V^2_{ac(LL)} \times R^2_o} - C_{int} =$$

$$\frac{2 \times 6400 \times 1.162mH \times 86.96 \times 400^2}{85^2 \times 2M\Omega^2} - 15pF = 7.16nF$$

Use 10 nF capacitor.

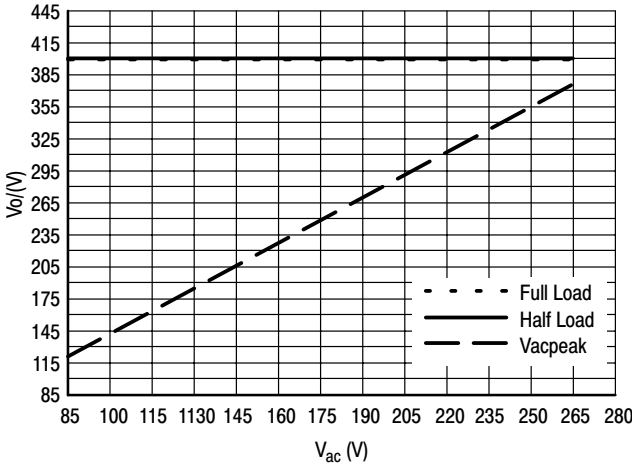

Figure 4. Theoretical V_o versus V_{ac} with C_T = 10nF

H. Design of the current sense circuit

Choose $R_{cs} = 0.68\ \Omega$

1. So the current sense resistor losses, P_{Rcs}:

$$P_{Rcs} = \frac{1}{6} \times R_{CS} \times I^2_{Lpk} = \frac{1}{6} \times 1 \times 2.894^2 = 0.949\ W$$

Therefore the power rating of R_{CS} is chosen to be 2 W.

2. Overcurrent protection resistor, R_{OCP} can be determined with below equation:

$$R_{OCP} = \frac{R_{CS} \times I_{Lpk}}{I_{OCP}} = \frac{0.68 \times 2.894}{205\ \mu A} = 9600\ \Omega$$

Use 10000 Ω resistor. This provide current limit at 3.01 A versus calculated value of I_{Lpk} = 2.894 A.

80 W, Universal Input, Traditional Boost Constant Output Voltage Level Regulation Operation Power Factor Correction Circuit Part List

Index	Value	Comment	Index	Value	Comment
C1	0.63 μF@600 V	Filtering Capacitor	R6	22 Ω@0.25 W	Aux Winding Resistor
C2	680 nF	Pin 2 $V_{control}$ Capacitor	R7	100 KΩ@2 W	Start–up Resistor
C3	10 nF	Pin 3 Oscillator Capacitor	R8	1N5406	Input Diode
C4	100 μF@50 V	Aux Capacitor, E–Cap	D1	1N5406	Input Diode
C5	100μF@450V	Output Capacitor, E–Cap	D2	1N5406	Input Diode
C6	1 nF@50 V	Feedback Filtering Capacitor	D3	1N5406	Input Diode
R1	0.68 Ω@2 W	Current Sense Resistor	D4	1N4937	Aux Winding Diode
R2	10 KΩ@0.25 W	OCP Sensing Resistor	D5	MUR460	Boost Diode
R3	1 MΩ@0.25 W	Feedback Resistor	D6	1N5245	Aux 15 V Zener Diode
R4	1 MΩ@0.25 W	Feedback Resistor	D7	MTP8N50E	Power MOSFET
R5	10 Ω@0.25 W	Gate Resistor	Q1	1.162 mH	Inductor

* E 30/15/7, N67 Material from EPCOS
Primary – 187 turns of # 23 AWG, Secondary – 19 turns of # 23 AWG.
Gap length 2.269mm total for a primary inductance L_P of 1.162mH.

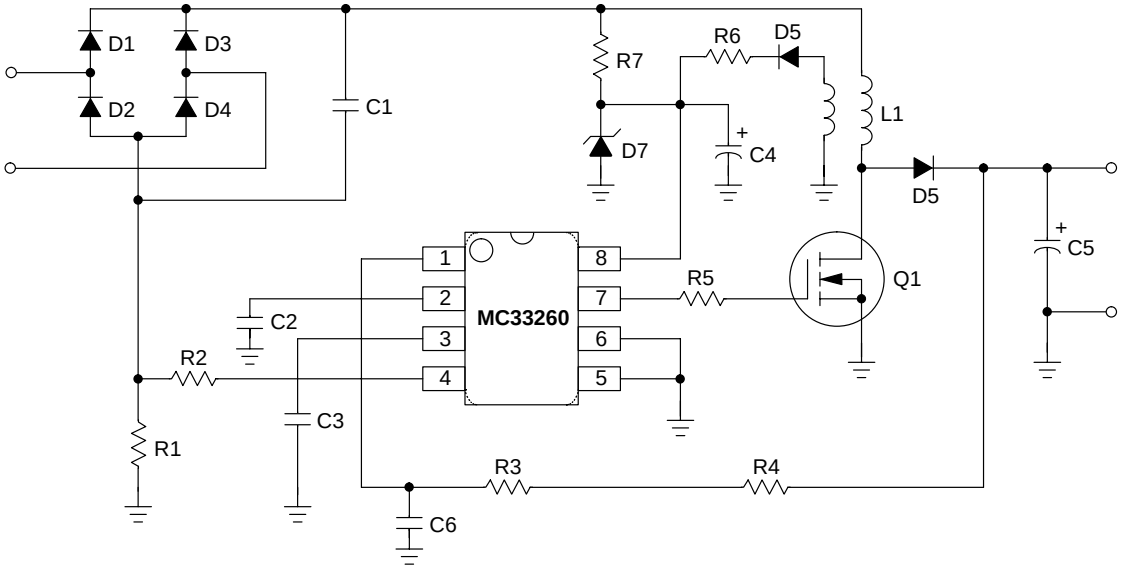

Figure 5. 80 W Universal Input, Traditional Boost Constant Output Voltage Regulation Level Operation Power Factor Correction Circuit

Design Table for Universal Input, Traditional Boost Constant Output Voltage Regulation Level Operation Power Factor Correction

P_o	25	50	75	100	125	150	200	(Watts)
L_P	3.720	1.860	1.240	0.930	0.744	0.620	0.465	(mH)
C_o	33	68	100	100	150	150	220	(μF)
R_{CS}	2	1	0.68	0.5	0.39	0.33	0.25	Ω
R_{OCP}	10000	10000	10000	9100	9100	9100	9100	Ω
C_{in}	0.22	0.63	0.63	1.0	1.0	1.0	1.0	(μF)
C_T	10	10	10	10	10	10	10	(nF)
Q	MTP4N50E		MTP8N50E			MTW14N50E		
D^{out}	MUR160		MUR460					
D_{in}	1N4007		1N5406					

Design Example II – Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction

The basic design specification concerns the following:

- Mains Voltage Range: $V_{ac(LL)} - V_{ac(HL)} = 85 – 265\ V_{ac}$
- Maximum Regulated DC Output Voltage: $V_o = 400\ V_{dc}$
- Minimum Regulated DC Output Voltage: $V_{omin} = 140\ V_{dc}$
- Rated Output Power: $P_o = 80$ W
- Expected Efficiency, $\eta > 90\%$

A. The input power, P_{in} is given by

$$P_{in} = \frac{P_o}{\eta} = \frac{80}{0.92} = 86.96\ W$$

B. Input diode current is maximum at $V_{inrms} = V_{ac(LL)}$

$$I_{inpk} = \frac{\sqrt{2}P_o}{\eta V_{ac(LL)}} = \frac{\sqrt{2} \times 80}{0.92 \times 85} = 1.447\ A$$

C. Inductor design

1. Inductor peak current:

$$I_{Lpk} = 2I_{inpk} = 2 \times 1.447 = 2.894\ A$$

2. Inductor value, for follower boost operation, $V_o = V_{omin}$:

$$L_p = \frac{2 \times t_{total}\left(\frac{V_{omin}}{\sqrt{2}} - V_{ac(LL)}\right)}{V_{omin} I_{Lpk}}$$

$$= \frac{2 \times 40 \times 10^{-6}\left(\frac{140}{\sqrt{2}} - 85\right)85}{140 \times 2.894} = 0.235\ \mu H$$

Let the switching cycle t = 40 μs for universal input (85 to 265 V_{ac}) operation.

3. The number of turns required for a selected core size and material is:

$$N_P = \frac{L_P I_{Lpk} 10^6}{B_{max} A_e} =$$

$$\frac{0.235 \times 10^{-3} \times 2.894 \times 10^6}{0.3 \times 32.1} = 70.6\ \text{turns} \approx 71\ \text{turns}$$

Using EPCOS E 20/10/6, N67 material, B_{max} =0.3 T and A_e = 32.1 mm^2.

4. The required air gap to achieve the correct inductance and storage is:

$$l_{gap} = \frac{4\pi 10^{-7} N_p^2 A_e}{L_P}$$

$$= \frac{4\pi \times 10^{-7} \times 71^2 \times 32.1 \times 10^{-6}}{0.235 \times 10^{-3}}$$

$$= 0.856\ mm$$

5. Design of Auxiliary Winding

$$N_{aux} = \frac{V_{aux} N_P}{\left(V_o - V_{ac(HL)}\right)} = \frac{14 \times 71}{(400 - 265)}$$

$$= 7.4\ \text{turns} \approx 8\ \text{turns}$$

Round up to 8 turns to make sure enough voltage at the auxiliary winding.

D. To determine the output capacitor

As rule of thumb, for 80 W output, start with 100 μF, 450 V capacitor.

E. Calculation of MOSFET conduction losses

A 4A, 500 V MOSFET, MTP4N50E is chosen. The on resistance, $R_{ds(on)} \approx 1.75\ \Omega$@100°C. Therefore, maximum power MOSFET conduction losses is:

$$P_{(on)max} \approx \frac{1}{6} \times R_{ds(on)} \times I_{Lpk}^2 \left(1 - \frac{1.2 \times V_{ac(LL)}}{V_{omin}}\right)$$

$$= \frac{1}{6} \times 1.75 \times 2.894^2 \left(1 - \frac{1.2 \times 85}{140}\right) = 0.66\ W$$

F. Design of regulation and overvoltage protection circuit

The output voltage regulation level can be adjusted by R_o,

$$R_o \approx \frac{V_o}{200\ \mu A} = \frac{400}{200\ \mu A} = 2\ M\Omega$$

Use two 1MΩ resistors in series.

G. Designing the Oscillator Circuit

For follower boost operation, C_T is chosen with below equation:

$$C_T \geq \frac{2 \times K_{osc} \times L_P \times P_{in} \times V_o^2}{V_{ac(LL)}^2 \times R_o^2} - C_{int} =$$

$$\frac{2 \times 6400 \times 0.234mH \times 86.96 \times 140^2}{85^2 \times 2\ M\Omega^2} - 15pF = 162\ pF$$

Use 150 pF capacitor.

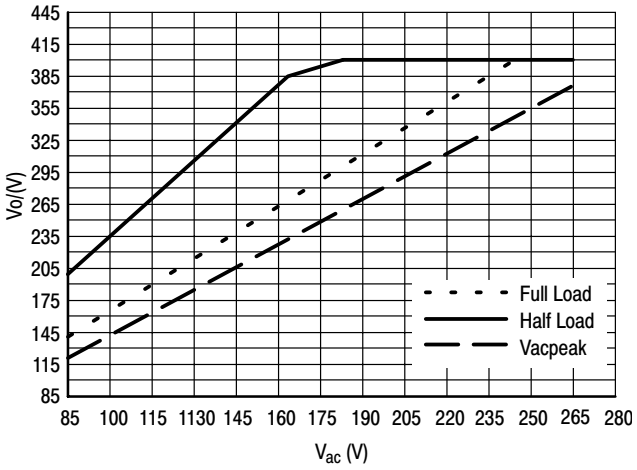

Figure 6. Theoretical V_o versus V_{ac} with C_T = 150pF

H. Design of the Current Sense Circuit

Choose R_{cs} = 0.68 Ω

1. So the current sense resistor losses, P_{Rcs}:

$$P_{Rcs} = \frac{1}{6} \times R_{CS} \times I_{Lpk}^2$$

$$= \frac{1}{6} \times 0.68 \times 2.894^2 = 0.949\ W$$

2. Overcurrent protection resistor, R_{OCP} can be determined with below equation:

$$R_{OCP} = \frac{R_{CS} \times I_{Lpk}}{I_{OCP}} = \frac{0.68 \times 2.894}{205\ \mu A} = 9600\ \Omega$$

Use 10000 Ω resistor. This provide current limit at 3.01 A versus calculated value of I_{Lpk} = 2.894 A.

80 W, Universal Input, Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction Circuit Part List

Index	Value	Comment	Index	Value	Comment
C1	0.63 μF@600 V	Filtering Capacitor	R6	22 Ω@0.25 W	Aux Winding Resistor
C2	680 nF	Pin 2 $V_{control}$ Capacitor	R7	100 KΩ@2 W	Start–up Resistor
C3	150 pF	Pin 3 Oscillator Capacitor	D1	1N5406	Input Diode
C4	100 μF@50 V	Aux Capacitor, E–Cap	D2	1N5406	Input Diode
C5	100 μF@450 V	Output Capacitor, E–Cap	D3	1N5406	Input Diode
C6	1 nF@50 V	Feedback Filtering Capacitor	D4	1N5406	Input Diode
R1	0.68 Ω@2 W	Current Sense Resistor	D5	1N4937	Aux Winding Diode
R2	10 KΩ@0.25 W	OCP Sensing Resistor	D6	MUR460	Boost Diode
R3	1 MΩ@0.25 W	Feedback Resistor	D7	1N5245	Aux 15 V Zener Diode
R4	1 MΩ@0.25 W	Feedback Resistor	Q1	MTP4N50E	Power MOSFET
R5	10 Ω@0.25 W	Gate Resistor	L1*	0.235 mH	Inductor

* E 20/10/6, N67 Material from EPCOS
Primary – 71 turns of # 23 AWG, Secondary – 8 turns of # 23 AWG.
Gap length 0.865 mm total for a primary inductance L_P of 0.235 mH.

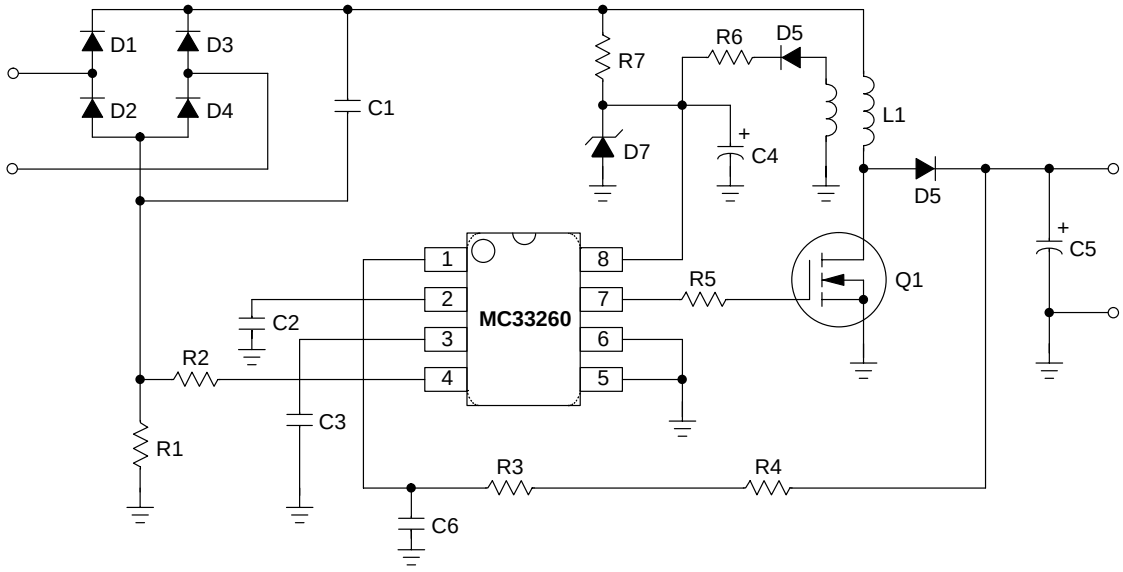

Figure 7. 80 W Universal Input, Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction Circuit

Design Table for Universal Input, Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction

P_o	25	50	75	100	125	150	200	(Watts)
L_P	0.752	376	0.251	0.188	0.150	0.102	0.094	(mH)
C_o	33	68	100	100	150	150	220	(μF)
R_{CS}	2	1	0.68	0.5	0.39	0.33	0.25	Ω
R_{OCP}	10000	10000	10000	9100	9100	9100	9100	Ω
C_{in}	0.22	0.63	0.63	1.0	1.0	1.0	1.0	(μF)
C_T	0.162	0.162	0.162	0.162	0.162	0.162	0.162	(nF)
Q	MTD2N50E		MTP4N50E		MTP8N50E			
D_{out}	MUR160		MUR460					
D_{in}	1N4007		1N5406		1N5406			

Notes

Greenline is a trademark of Semiconductor Components Industries, LLC.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.