

# DATA SHEET

## **PSMN070-200B; PSMN070-200P** N-channel TrenchMOS<sup>(TM)</sup> transistor

Product specification

August 1999

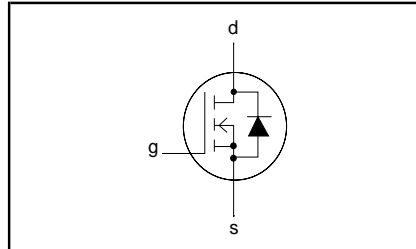


**N-channel TrenchMOS<sup>(TM)</sup> transistor PSMN070-200B; PSMN070-200P**

**FEATURES**

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

**SYMBOL**



**QUICK REFERENCE DATA**

$V_{DSS} = 200\text{ V}$
$I_D = 35\text{ A}$
$R_{DS(ON)} \leq 70\text{ m}\Omega$

**GENERAL DESCRIPTION**

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

**Applications:-**

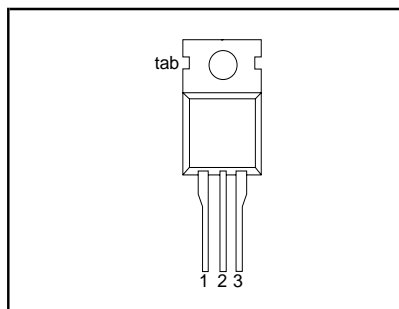
- d.c. to d.c. converters
- switched mode power supplies

The PSMN070-200P is supplied in the SOT78 (TO220AB) conventional leaded package.  
The PSMN070-200B is supplied in the SOT404 surface mounting package.

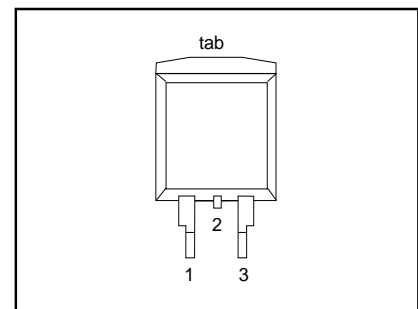
**PINNING**

PIN	DESCRIPTION
1	gate
2	drain <sup>1</sup>
3	source
tab	drain

**SOT78 (TO220AB)**



**SOT404 (D<sup>2</sup>PAK)**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DSS}$	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	200	V
$V_{DGR}$	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	200	V
$V_{GS}$	Gate-source voltage		-	$\pm 20$	V
$I_D$	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	35	A
		$T_{mb} = 100\text{ }^\circ\text{C}$	-	25	A
$I_{DM}$	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	140	A
$P_D$	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	250	W
$T_j, T_{stg}$	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

<sup>1</sup> It is not possible to make connection to pin:2 of the SOT404 package

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**AVALANCHE ENERGY LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{AS}$	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 35$ A; $t_p = 100$ $\mu$ s; $T_j$ prior to avalanche = 25°C; $V_{DD} \leq 50$ V; $R_{GS} = 50$ $\Omega$ ; $V_{GS} = 10$ V; refer to fig:15	-	462	mJ
$I_{AS}$	Non-repetitive avalanche current		-	35	A

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	0.6	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 package, pcb mounted, minimum footprint	60 50	- -	K/W K/W

**ELECTRICAL CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$	200 178	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2.0 1.0 -	3.0 - -	4.0 - 6	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 17$ A $T_j = 175^\circ\text{C}$	-	60	70 203	m $\Omega$ m $\Omega$
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 10$ V; $V_{DS} = 0$ V	-	2	100	nA
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 175^\circ\text{C}$	-	0.05	10 500	$\mu$ A $\mu$ A
$Q_{g(tot)}$	Total gate charge	$I_D = 35$ A; $V_{DD} = 160$ V; $V_{GS} = 10$ V	-	77	-	nC
$Q_{gs}$	Gate-source charge		-	16	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	28	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 100$ V; $R_D = 2.7$ $\Omega$ ; $V_{GS} = 10$ V; $R_G = 5.6$ $\Omega$	-	22	-	ns
$t_r$	Turn-on rise time		-	100	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	80	-	ns
$t_f$	Turn-off fall time		-	90	-	ns
$L_d$	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
$C_{iss}$	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	4570	-	pF
$C_{oss}$	Output capacitance		-	370	-	pF
$C_{rss}$	Feedback capacitance		-	160	-	pF

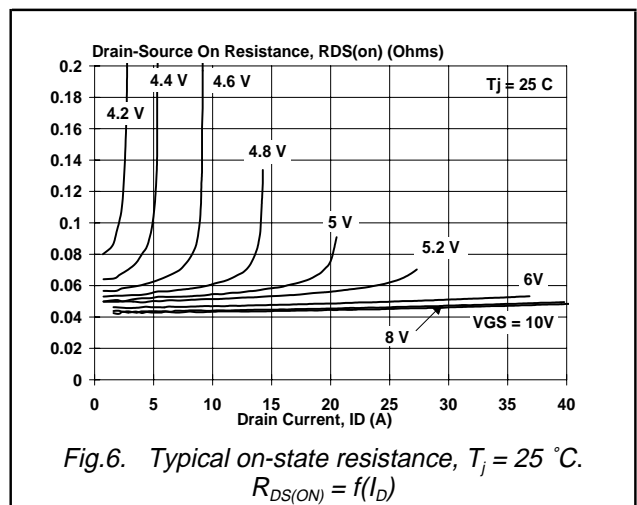
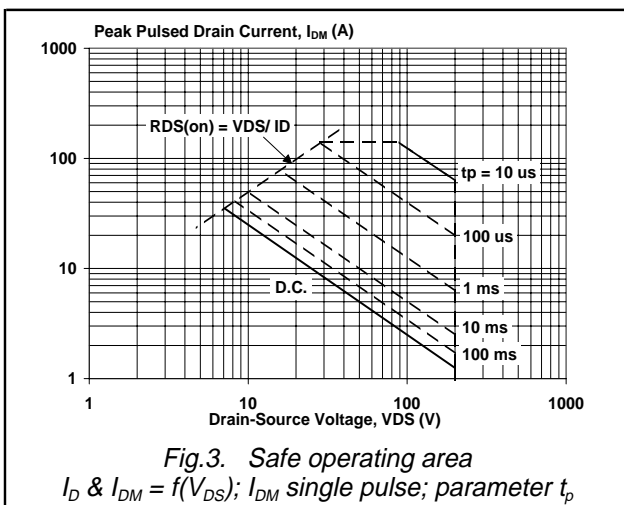
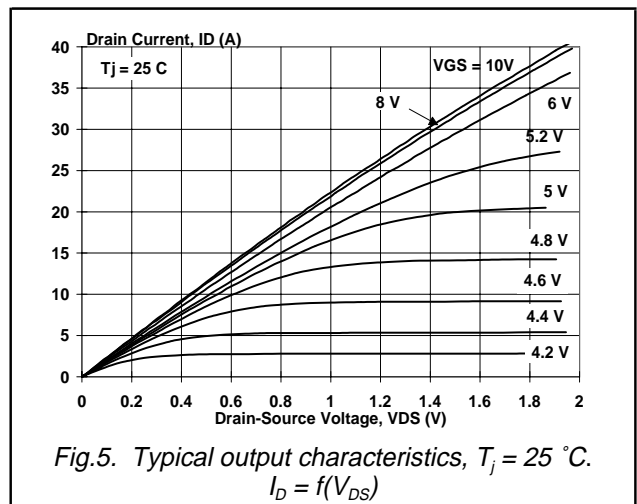
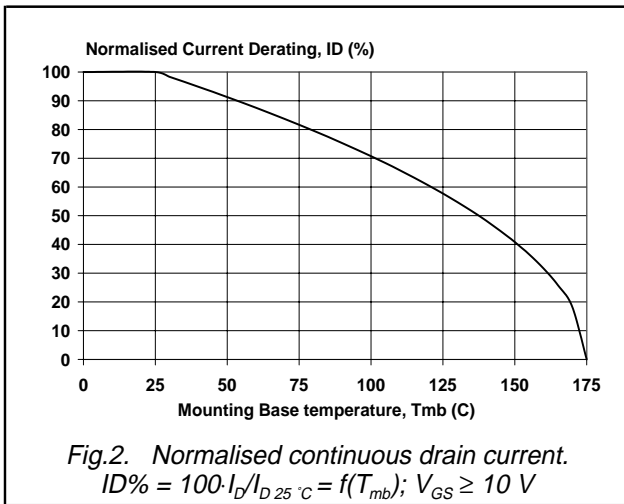
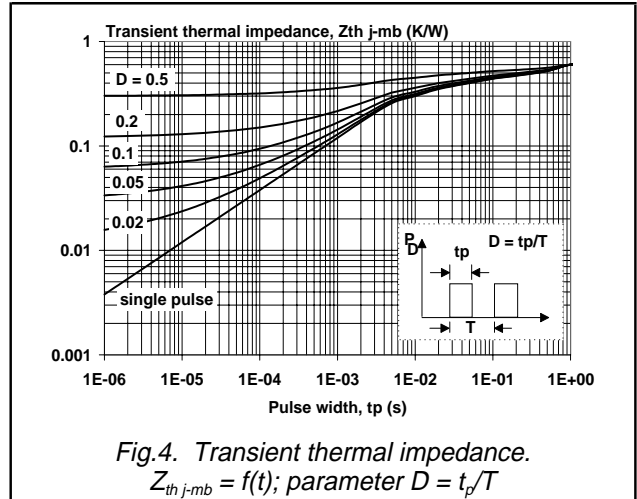
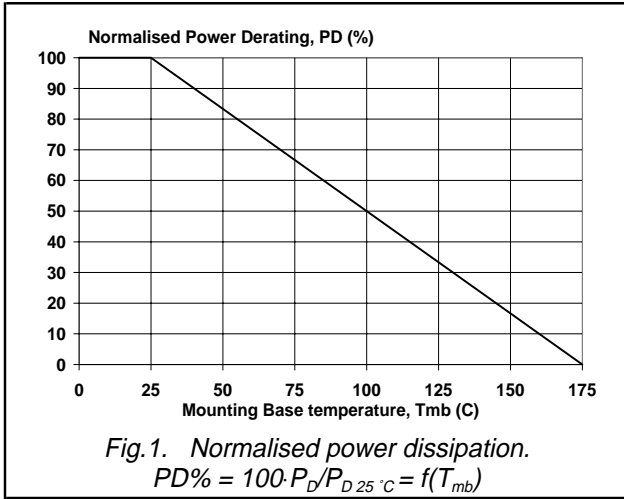
**SiliconMAX**N-channel TrenchMOS<sup>(TM)</sup> transistor PSMN070-200B; PSMN070-200P**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_S$	Continuous source current (body diode)		-	-	35	A
$I_{SM}$	Pulsed source current (body diode)		-	-	140	A
$V_{SD}$	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V
$t_{rr}$	Reverse recovery time	$I_F = 20\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	160	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	1.0	-	$\mu\text{C}$

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N-channel TrenchMOS<sup>(TM)</sup> transistor

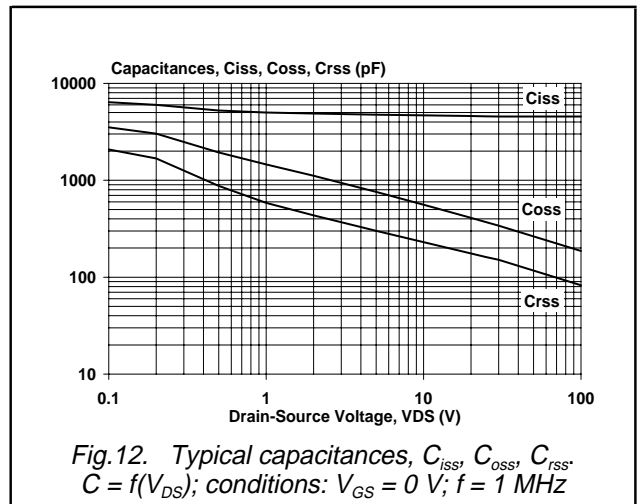
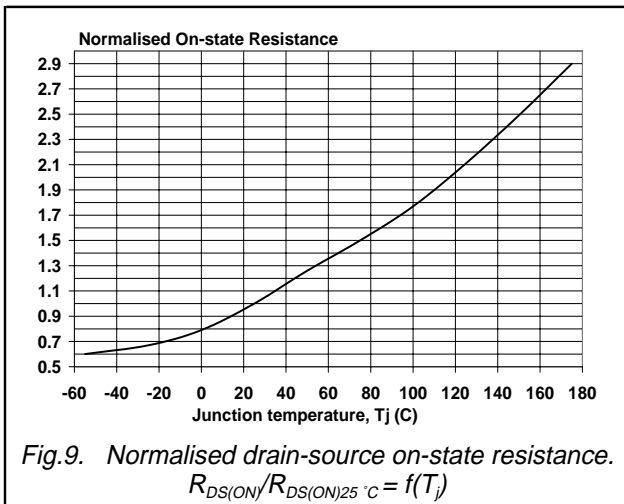
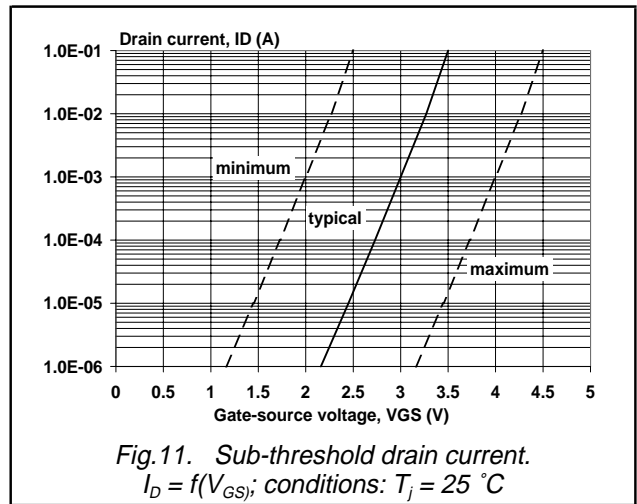
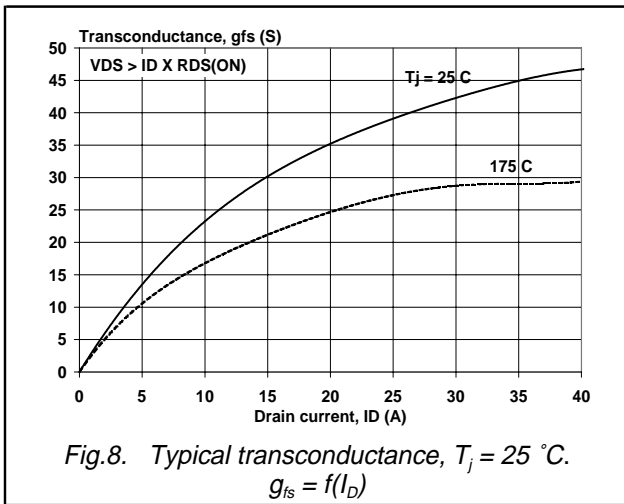
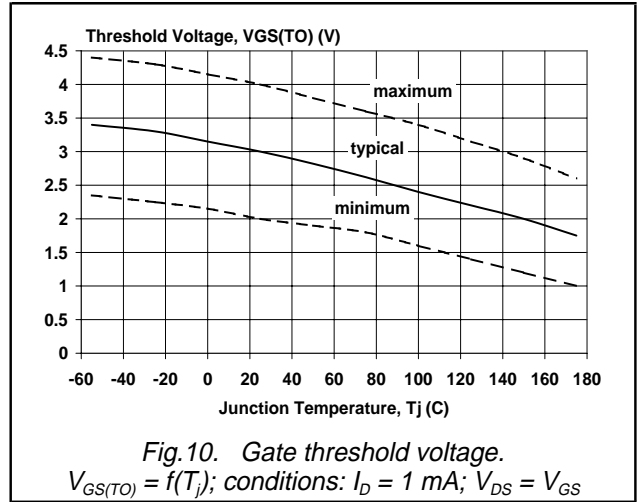
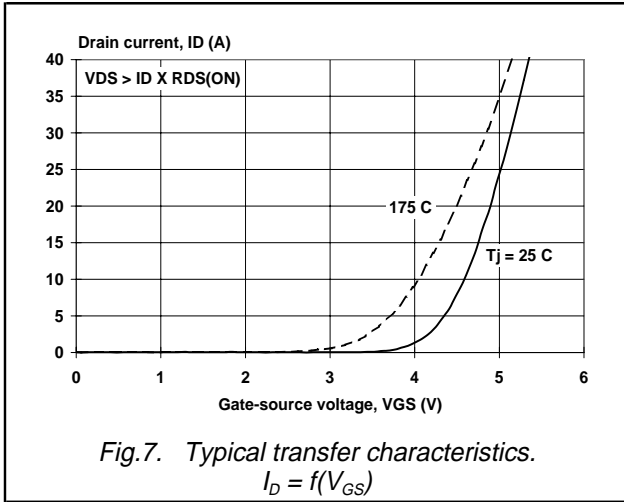
PSMN070-200B; PSMN070-200P



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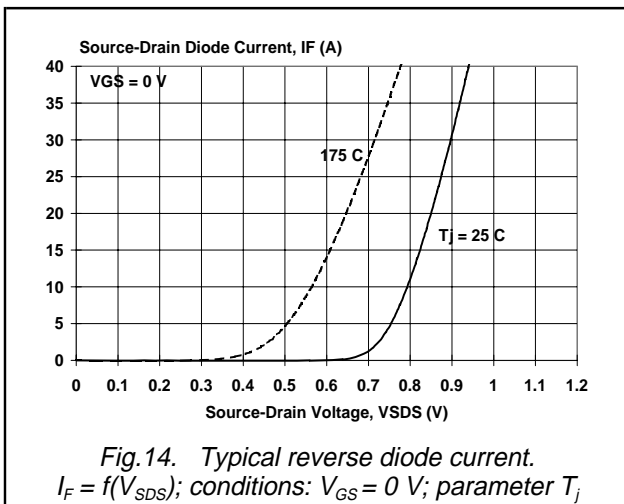
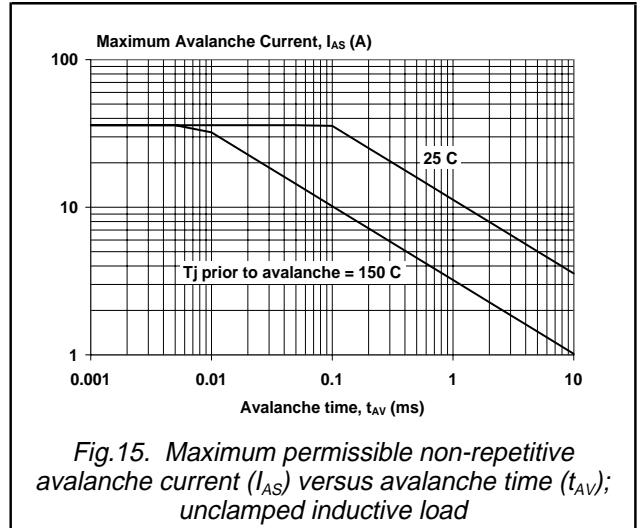
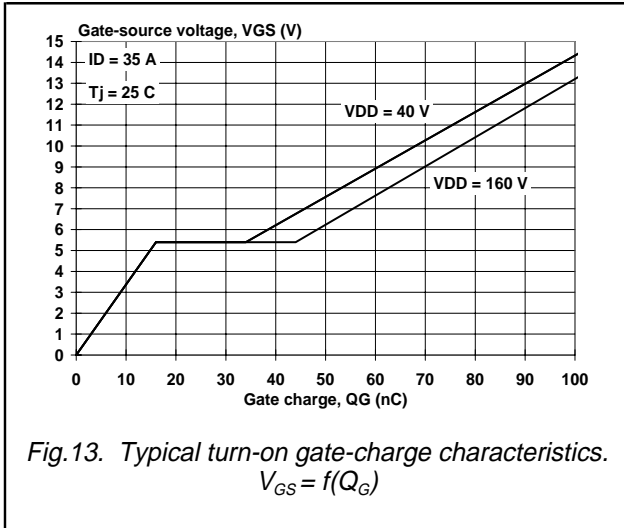
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N-channel TrenchMOS<sup>(TM)</sup> transistor

PSMN070-200B; PSMN070-200P





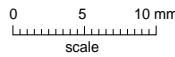
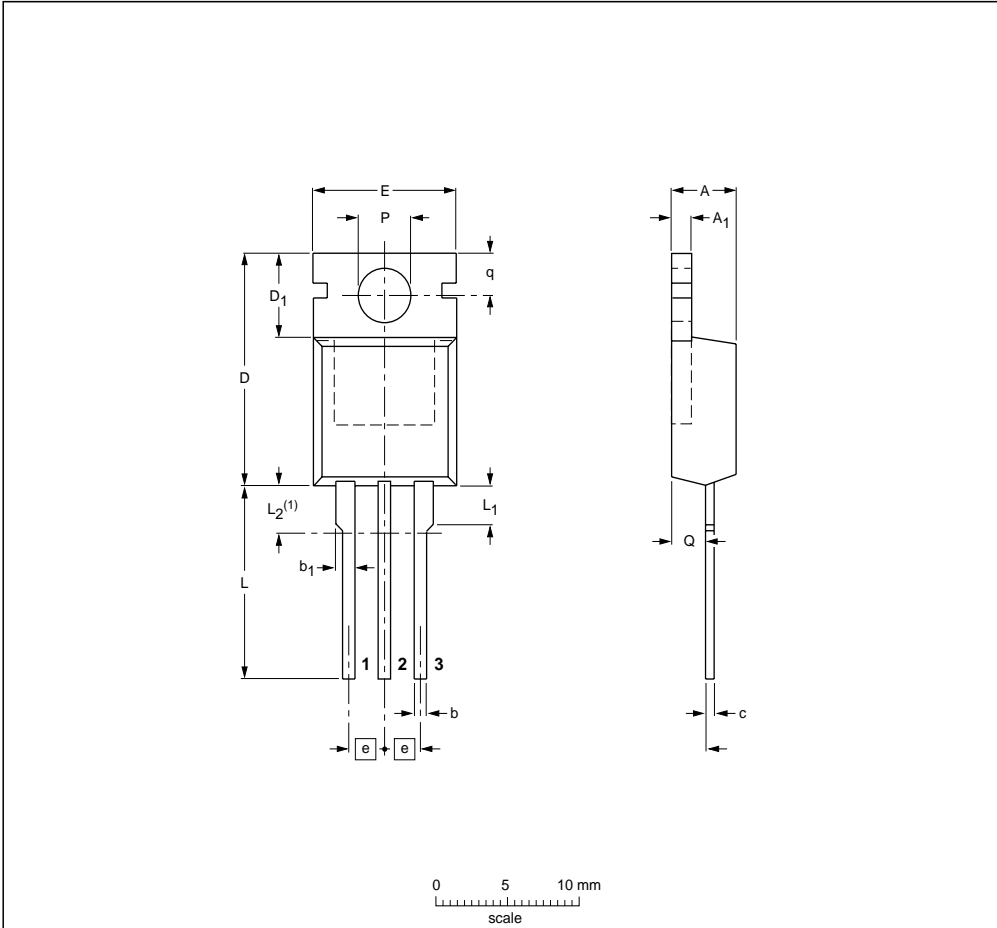
N-channel TrenchMOS<sup>(TM)</sup> transistor

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**MECHANICAL DATA**

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

**Note**

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220				97-06-11

Fig.16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

**Notes**

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

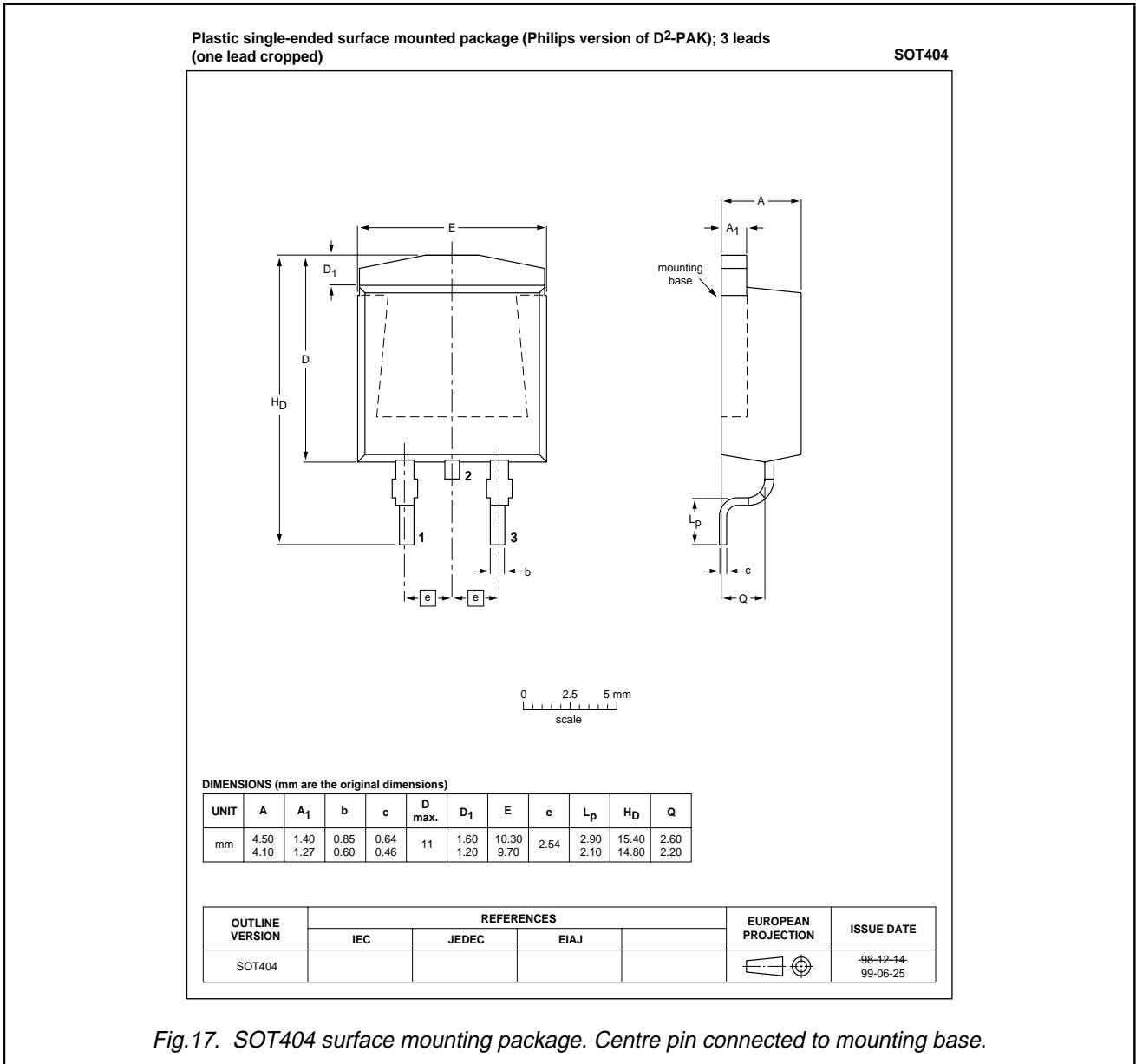




N-channel TrenchMOS<sup>(TM)</sup> transistor

PSMN070-200B; PSMN070-200P

**MECHANICAL DATA**



**Notes**

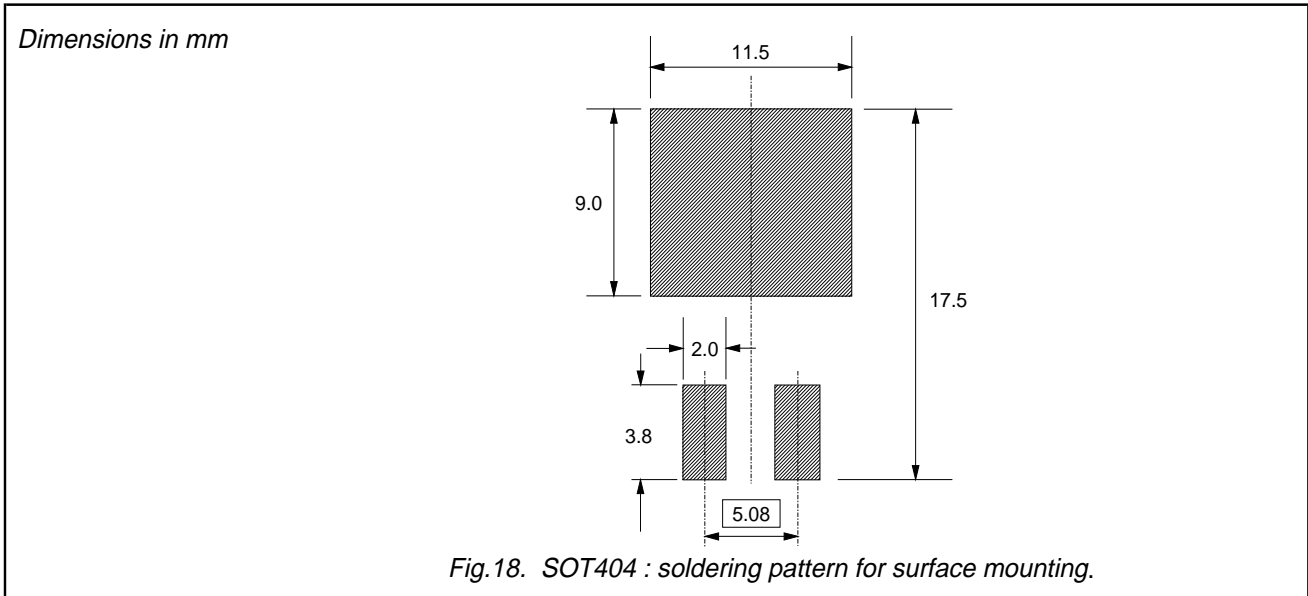
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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N-channel TrenchMOS<sup>(TM)</sup> transistor

PSMN070-200B; PSMN070-200P

**MOUNTING INSTRUCTIONS**



**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
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**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
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**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
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**Portugal:** see Spain

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**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
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Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
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Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
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