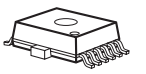
Dual Low Drop Voltage Regulator

TLE 4473 GV53

TLE 4473 GV52

Features

- Output 1: 300 mA, 3.3 V (±3%) or 2.6 V (±3%)
- Output 2: 180 mA, 5 V (±2%)
- Low quiescent current consumption
- Disable function separately for both outputs
- Wide operation range: up to 42 V
- Very low dropout voltage
- 2 independent reset circuits
- Watchdog
- Output protected against short circuit
- Wide temperature range: -40 °C to 150 °C
- Overtemperature protection
- Overload protection



P-DSO-12-2, -3, -6

Functional Description

The TLE 4473 is a monolithic integrated voltage regulator with two very low-drop outputs, Q1 for loads up to 300 mA and Q2 providing a maximum of 180 mA. An input voltage in the range of 5.6 V ≤ V_I ≤ 45 V is transformed to V_{Q2} = 5.0 V (±2%) and V_{Q1} = 3.3 V ±3% (TLE 4473 GV53) or V_{Q1} = 2.6 V ±3% (TLE 4473 GV52). The device is also available with dual 5 V output voltage, please refer to the TLE 4473 GV55 data sheet. Two inhibit pins allow a flexible power management. Both outputs can independently be enabled or disabled. Thus the current consumption of the application can be reduced to a minimum. The quiescent current of the TLE 4473 with both outputs disabled is < 1 µA. The TLE 4473 is designed to supply microprocessor systems and sensors under the severe conditions of automotive applications and is therefore equipped with additional protection functions against overload, short circuit and overtemperature.

The device operates in the wide junction temperature range of -40 °C to 150 °C.

Type	Ordering Code	Package
TLE 4473 GV53	Q67007-A9668	P-DSO-12-6
TLE 4473 GV52	Q67007-A9683	P-DSO-12-6

The low drop regulator features a reset with adjustable power on delay for each of the outputs. In addition the output for the microcontroller supply comes up with a watchdog in order to supervise a microcontroller.

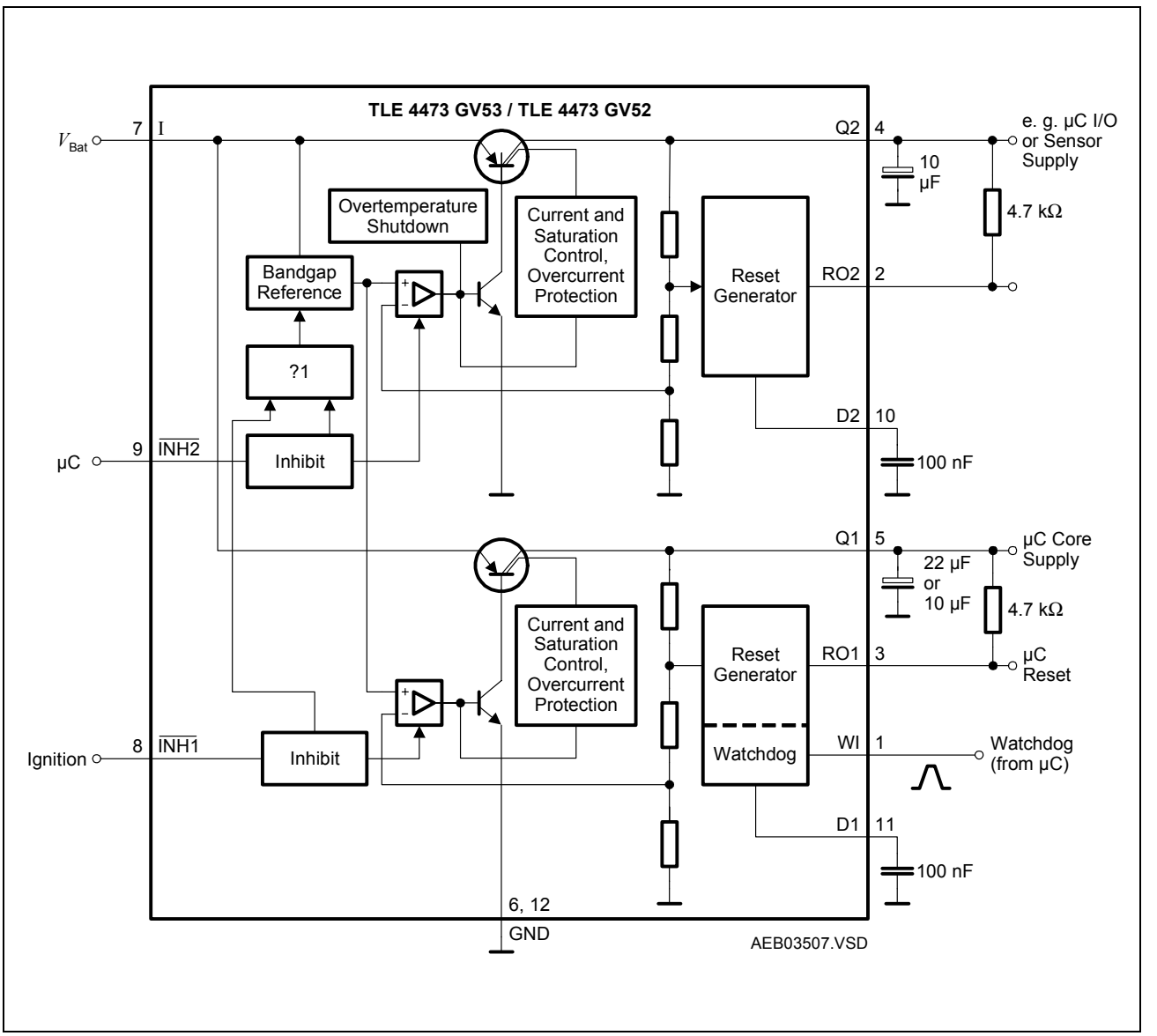


Figure 1 Block Diagram with Typical External Components

Reset and Watchdog Behaviour:

The reset output RO1 is in high-state if the voltage on the delay capacitor C_{D1} is greater or equal V_{DL1}. The delay capacitor C_{D1} is charged with the current I_{DC1} for output voltages greater than the reset threshold V_{RT1}. If the output voltage drops below V_{RT1} (“reset condition”), the delay capacitor C_{D1} will be discharged rapidly. If V_{D1} reaches V_{DL1}, the reset output RO1 is set to low.

At power-on, the charging process of C_{D1} starts from 0 V, which leads to the equation

$$t_{D,\,on} = \frac{C_{D1} \times V_{DU1}}{I_{DC1}} \quad (1)$$

for the power-on reset delay time.

When the voltage at the delay capacitor has reached V_{DU1} and RO1 was set to high, the watchdog circuit is enabled and discharges C_{D1} with the constant current I_{DD1}.

If there is no rising edge observed at the watchdog input, C_{D1} will be discharged down to V_{DL1}, where the reset output RO1 will be set to low and C_{D1} will be charged again with the current I_{DC1} until V_{D1} reaches V_{DU1} and reset will be set high again.

If a watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period, C_{D1} is charged again and the reset output stays high. After V_{D1} has reached V_{DU1}, the periodical cycle starts again.

The watchdog timing is shown in **Figure 2**. The maximum duration between two watchdog pulses corresponds to the minimum watchdog trigger time $T_{WI,tr}$. Higher capacitances on pin D1 result in larger watchdog trigger time:

$$T_{WI,tr}\big|_{max} = 0.42\ \text{ms/nF} \times C_{D1} \quad (2)$$

If the output voltage Q2 decreases below V_{RT2} , the external capacitor C_{D2} is discharged. When the voltage at this capacitor drops below V_{DL2}, a reset signal is generated at pin 11 (RO2), i.e. the reset output is set to low-level. If the output voltage rises above the reset threshold, C_{D2} will be charged with the constant current I_{DC2}. After the power-on-reset time, the voltage at the capacitor reaches V_{DU2} and the reset output will be set to high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_{D2} using **Equation (1)** analogous for Q2.

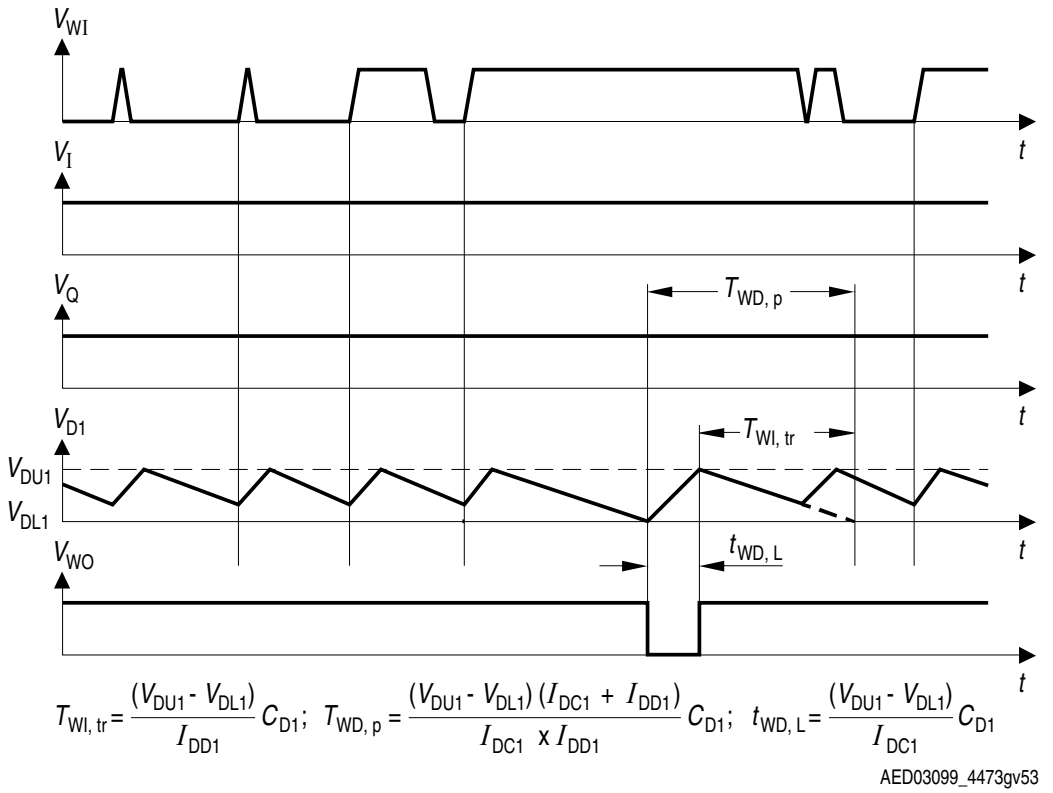
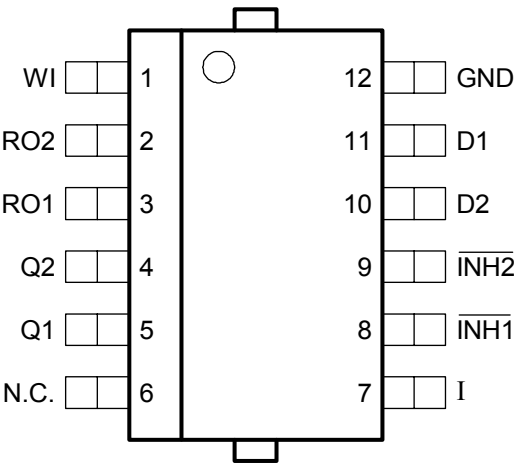


Figure 2 Watchdog Timing Schedule



Pin 6 and heat slug should be connected to GND

Figure 3 **Pin Configuration TLE 4473 GV53, TLE 4473 GV52** (top view)

Table 1 **Pin Definitions and Functions (TLE 4473 GV53, TLE 4473 GV52)**

Pin No.	Symbol	Function
1	WI	**Watchdog input;** input for watchdog pulses, positive edge triggered
2	RO2	**Reset output for Q2;** open collector output
3	RO1	**Reset and watchdog output for Q1;** open collector output
4	Q2	**Output voltage 2 (5 V);** block to GND with a capacitor $C_{Q2} \geq 22\ \mu F$, ESR < 5 Ω at 10 kHz or $C_{Q2} \geq 10\ \mu F$, ESR < 4 Ω at 10 kHz
5	Q1	**Output voltage 1 (3.3 V/2.6 V);** block to GND with a capacitor $C_{Q1} \geq 10\ \mu F$, ESR < 5 Ω at 10 kHz
6	N.C.	**Not connected;** connect to GND
7	I	**Input voltage;** block to GND directly at the IC with a ceramic capacitor.
8	$\overline{\text{INH1}}$	**Inhibit input 1;** low level at $\overline{\text{INH2}}$ and $\overline{\text{INH1}}$ disables Q2 and Q1
9	$\overline{\text{INH2}}$	**Inhibit input 2;** low level disables Q2
10	D2	**Reset Delay 2;** connect a capacitor to set reset delay for Q2
11	D1	**Reset Delay 1;** connect a capacitor to GND to set reset delay and watchdog timing for Q1
12	GND	**Ground**
Heatsink	N. C.	**Not connected;** connect to GND

Table 2 Absolute Maximum Ratings

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input I					
Voltage	V_I	-42	45	V	–
Current	I_I	–	–	mA	Internally limited
Stand-by Output Q2					
Voltage	V_{Q2}	-0.3	18	V	–
Current	I_{Q2}	–	–	mA	Internally limited
Main Output Q1					
Voltage	V_{Q1}	-0.3	18	V	–
Current	I_{Q1}	–	–	mA	Internally limited
Inhibit Input $\overline{\text{INH1}}$					
Voltage	$V_{\overline{\text{INH1}}}$	-42	45	V	–
Current	$I_{\overline{\text{INH1}}}$	-2	2	mA	–
Inhibit Input $\overline{\text{INH2}}$					
Voltage	$V_{\overline{\text{INH2}}}$	-42	45	V	–
Current	$I_{\overline{\text{INH2}}}$	-2	2	mA	–
Reset Output RO1					
Voltage	V_{RO1}	-0.3	18	V	–
Current	I_{RO1}	–	–	mA	Internally limited
Reset Output RO2					
Voltage	V_{RO2}	-0.3	18	V	–
Current	I_{RO2}	–	–	mA	Internally limited
Reset Delay D1					
Voltage	V_{D1}	-0.3	7	V	–
Current	I_{D1}	-5	5	mA	–
Reset Delay D2					
Voltage	V_D	-0.3	7	V	–
Current	I_D	-5	5	mA	–

Table 2 Absolute Maximum Ratings (cont'd)

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Watchdog Input WI					
Voltage	V_{RADJ}	-0.3	7	V	–
Current	I_{RADJ}	-5	5	mA	–
Temperatures					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–
ESD Protection					
Electrostatic Discharge Voltage	V_{ESD}	–2	2	kV	Human Body Model

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.6	42	V	Q1 & Q2
		4.5	42	V	only Q1 regulating
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances P-DSO-12-6					
Junction pin	$R_{thj\text{-}pin}$	–	3	K/W	–
Junction ambient	$R_{thj\text{-}a}$	–	115	K/W	PCB Heat Sink Area 0 mm^2 1)
Junction ambient	$R_{thj\text{-}a}$	–	100	K/W	PCB Heat Sink Area 100 mm^2 1)
Junction ambient	$R_{thj\text{-}a}$	–	60	K/W	PCB Heat Sink Area 300 mm^2 1)
Junction ambient	$R_{thj\text{-}a}$	–	48	K/W	PCB Heat Sink Area 600 mm^2 1)

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35 µ Cu; 5 µ Sn; zero airflow.

Note: In the operating range the functions given in the circuit description are fulfilled. Integrated protection functions are designed to prevent IC destruction under fault conditions. Protection functions are not designed for repetitive operation.

Electrical Characteristics

V_{I1} =13.5 V; V_{INH1} =V_{INH2}= 5V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
REGULATOR 2:						
Output Q2						
Output voltage	V_{Q2}	4.90	5.0	5.10	V	1 mA < I_{Q2}< 180 mA; 6 V < V_I< 28 V
Output current limitation	I_{Q2}	200	300	600	mA	V_{Q2} = 4.5 V
Output drop voltage; $V_{DRQ2} = V_{I2} - V_{Q2}$	V_{DRQ2}	–	300	600	mV	I_{Q2} = 100 mA; 1)
Load regulation	$\Delta V_{Q2,Lo}$	–	15	50	mV	1 mA < I_{Q2} < 200 mA;
Line regulation	$\Delta V_{Q2,Li}$	–	5	20	mV	I_{Q2} = 1 mA; 6 V < V_I < 28 V
Power supply ripple rejection	$PSRR$	–	65	–	dB	f_r = 100 Hz; V_r = 1 V_{pp}
Current Consumption						
Quiescent current; stand-by $I_q = I_I - I_{Q2}$	I_q	–		165	µA	TLE 4473 GV52; I_{Q2} = 500 µA; T_j = 25 °C; V_{INH1} < $V_{INH1\ OFF}$ (Q1 off)
		–		205	µA	TLE 4473 GV52; I_{Q2}= 500 µA; T_j = 85 °C; V_{INH1} < $V_{INH1\ OFF}$ (Q1 off)
		–		180	µA	TLE 4473 GV53; I_{Q2} = 500 µA; T_j = 25 °C; V_{INH1} < $V_{INH1\ OFF}$ (Q1 off)
		–		210	µA	TLE 4473 GV53; I_{Q2}= 500 µA; T_j = 85 °C; V_{INH1} < $V_{INH1\ OFF}$ (Q1 off)
		–		235	µA	I_{Q2} = 500 µA; V_{INH1} < $V_{INH1\ OFF}$ (Q1 off)

Electrical Characteristics (cont'd)

V_{I1} =13.5 V; V_{INH1} =V_{INH2}= 5V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption (cont'd)						
Quiescent current; stand-by $I_q = I_I - I_{Q2}$	I_q			5	mA	I_{Q2} = 100 mA; V_{INH1} < $V_{INH1\ OFF}$(Q1 off)
Quiescent current; inhibited	I_q	–	–	1	µA	V_{INH1}=V_{INH2}= 0V; T_J < 85°C
Inhibit Input $\overline{INH2}$						
Turn-on Voltage	$V_{\overline{INH2}\ ON}$	–	–	2.3	V	V_{Q2} on
Turn-off Voltage	$V_{\overline{INH2}\ OFF}$	0.8	–	–	V	V_{Q2} off
H-input current	$I_{\overline{INH2}\ ON}$	– 1	0.5	3	µA	V_{INH2} = 5 V
L-input current	$I_{\overline{INH2}\ OFF}$	– 1	0.1	1	µA	0 V < V_{INH2} < 0.8 V
Reset Timing D2						
Charge current	I_{DC2}	5.0	9.0	13.0	µA	V_{D2} = 0.7 V
Upper timing threshold	V_{DU2}	1.6	1.8	2.2	V	–
Lower timing threshold	V_{DL2}	0.3	0.45	0.6	V	–
Saturation Voltage	$V_{D2,SAT}$			100	mV	V_{Q2} < V_{RT2}
Reset delay time	T_{RD2}	12	20	28	ms	C_{D2} = 100 nF
Reset reaction time	T_{rr}	–		10	µs	C_{D2} = 100 nF

Electrical Characteristics (cont'd)

V_{I1} =13.5 V; V_{INH1} =V_{INH2}= 5V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reset Output RO2						
Reset switching threshold	V_{RT2}	4.5	4.65	4.8	V	–
Reset output current	I_{RO2}	–	–	1.4	mA	Collector current of RO1, power good, reset still delayed. V_{Q2}=5V, V_{D2}=0V,V_{RO2}=0.3V
Reset output low voltage	V_{RO2L}	–	0.15	0.3	V	$V_{Q2} \geq$ 1 V, V_{D2}=0V, I_{RO2}= 0.5mA
Reset high voltage	V_{RO2H}	4.5	–	–	V	$R_{RO2,ext}$=4.7kΩ
REGULATOR 1:						
Output Q1						
Output voltage	V_{Q12}	3.20	3.3	3.40	V	TLE 4473 GV53 1 mA < I_{Q1}< 300 mA; 4.5 V < V_I< 28 V
Output voltage	V_{Q12}	2.52	2.60	2.68	V	TLE 4473 GV52 1 mA < I_{Q1}< 300 mA; 4.5 V < V_I< 28 V
Output current limitation	I_{Q1}	350	500	600	mA	V_{Q1} = 3.0 V (TLE 4473 GV53); V_{Q1} = 2.3 V (TLE 4473 GV52)
Load regulation	$\Delta V_{Q1,Lo}$	–	5	50	mV	5 mA < I_{Q1} < 300 mA;
Line regulation	$\Delta V_{Q1,Li}$	–	5	20	mV	I_{Q1} = 5 mA; 6 V < V_I< 28 V
Power-Supply-Ripple-Rejection	$PSRR$	–	65	–	dB	f_r= 100 Hz; V_r = 1V_{pp}

Electrical Characteristics (cont'd)

V_{I1} =13.5 V; V_{INH1} =V_{INH2}= 5V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Quiescent current; $I_q = I_I - I_{Q1} - I_{Q2}$	I_q	–	200	265	µA	TLE 4473 GV52; I_{Q1} = 500 µA; Q1 on; Q2 off; T_j < 85°C
		–	210	280	µA	TLE 4473 GV53; I_{Q1} = 500 µA; Q1 on; Q2 off; T_j < 85°C
		–	7	20	mA	I_{Q1} = 300 mA I_{Q2} = 500 µA, V_{Q1} & V_{Q2} on
		–	250	500	µA	I_{Q2} = I_{Q1} = 500 µA; V_{Q1} & V_{Q2} on
Inhibit Input $\overline{\text{INH1}}$						
Turn-on Voltage	$V_{\overline{INH1}\ ON}$	–	–	2.3	V	V_{Q1} on
Turn-off Voltage	$V_{\overline{INH1}\ OFF}$	0.8	–	–	V	V_{Q1} off
H-input current	$I_{\overline{INH1}\ ON}$	– 1	0.5	3	µA	V_{INH1}= 5 V
L-input current	$I_{\overline{INH1}\ OFF}$	– 1	0.1	1	µA	0 V < V_{INH1}< 0.8 V
Watchdog and Reset Timing D1						
Charge current	I_{DC1}	3.0	7.0	11.0	µA	V_{D1} = 0.7 V
Discharge current	I_{DD1}	1.1	1.5	3.7	µA	V_{D1} = 0.7 V
Upper timing threshold	V_{DU1}	0.7	1.1	1.6	V	–
Lower timing threshold	V_{DL1}	0.2	0.35	0.6	V	–

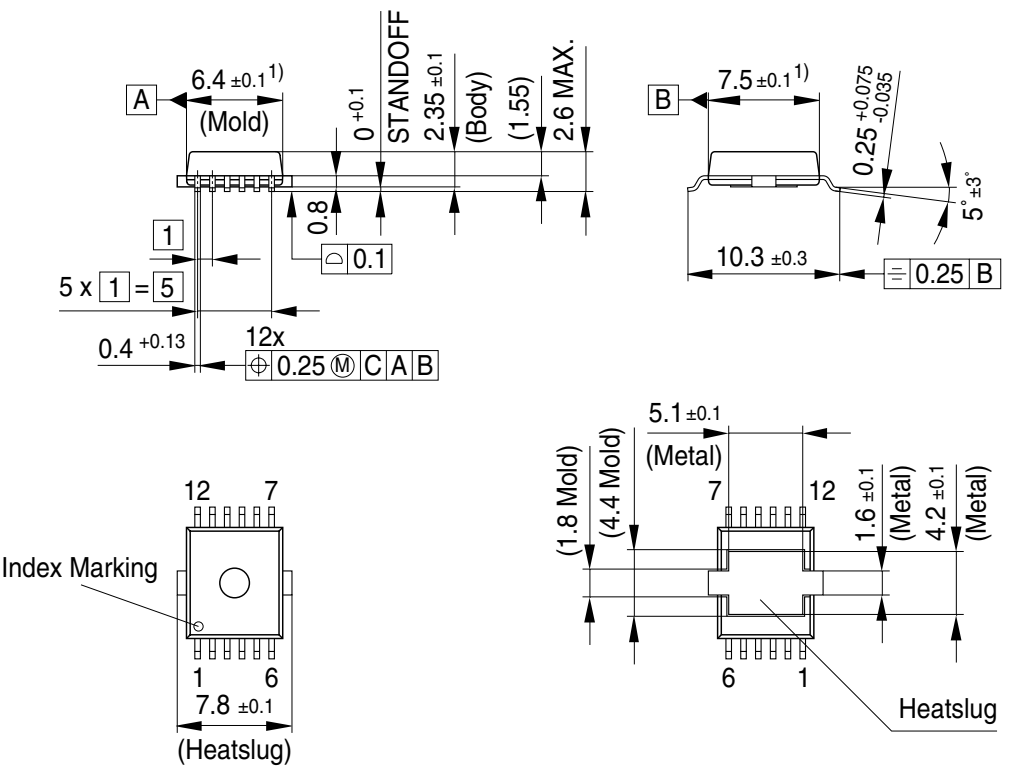
Electrical Characteristics (cont'd)

V_{I1} =13.5 V; V_{INH1} =V_{INH2}= 5V; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog and Reset Timing D1 (cont'd)						
Saturation Voltage	$V_{D1,SAT}$			100	mV	V_{Q1} < V_{RT2}
Watchdog trigger time	$T_{WI,tr}$	24	32	40	ms	C_{D1} = 100 nF
Reset delay time	T_{RD1}	11	17	23	ms	C_{D1} = 100 nF
Reset reaction time	T_{rr}	–		5.0	µs	C_{D1} = 100 nF
Reset Output RO1						
Reset switching threshold	V_{RT1}	2.97	3.08	3.18	V	TLE 4473 GV53
		2.34	2.42	2.50	V	TLE 4473 GV52
Reset threshold headroom	V_{R1HEAD}	100	–	–	mV	TLE 4473 GV53
Reset threshold headroom	V_{R1HEAD}	80	–	–	mV	TLE 4473 GV52
Reset output current	I_{RO1}	–	–	1.4	mA	Collector current of RO1, power good, reset still delayed. V_{Q1}= 3.30 V (TLE 4473 GV53), V_{Q1} = 2.60 V (TLE 4473 GV52); V_{Q2}=5.0 V; V_{D1}=0 V,V_{RO1}=0.3 V
Reset output low voltage	V_{RO1L}	–	0.1	0.3	V	V_{Q1} ≥ 1 V, V_{D1}=0V, I_{RO1}=0.5mA
Reset output high voltage	V_{RO1H}	2.45	–	–	V	$R_{RO1,ext}$=4.7kΩ connected to Q1;TLE 4473 GV52
Reset output high voltage	V_{RO1H}	3.15	–	–	V	$R_{RO1,ext}$=4.7kΩ connected to Q1;TLE 4473 GV53

1) Drop voltage = V_I – V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09349

Figure 4 **P-DSO-12-6** (Plastic Dual Small Outline)

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SMD = Surface Mounted Device

Dimensions in mm

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