DATA SHEET

74HC/HCT9323A

Programmable ripple counter with oscillator (3-State)

Objective specification

1995 Oct 27

IC06 Data Handbook

Philips
Semiconductors

PHILIPS

Programmable ripple counter with oscillator (3-State)

74HC/HCT9323A

FEATURES

- 8-pin space saving package
- Programmable 3-stage ripple counter
- Suitable for over-tone crystal application up to 85MHz (V_{CC} = 5V ± 10%)
- 3-State output buffer
- Two internal capacitors
- Recommended operating range for use with third overtone crystals 3V to 6V
- Oscillator stop function ($\overline{MR}$)
- Output capability: bus driver → (15 LSTTL)
- I_{CC} category: MSI

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits
- CIO (Compact Integrated Oscillator)
- Third-overtone crystal operation

DESCRIPTION

The 74HC/HCT9323A are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT 9323A are oscillators designed for quartz crystal combined with a programmable 3-State counter, a 3-State output buffer and an overriding asynchronous master reset ($\overline{MR}$). With the two select inputs S1 and S2 the counter can be switched in the divide-1, 2, 4 or 8 mode. If left floating the clock is divided by 8. The oscillator is designed to operate either in the fundamental or third overtone mode depending on the crystal and external components applied. On-chip capacitors minimize external component count for third overtone crystal applications.

The oscillator may be replaced by an external clock signal at input X1. In this event the other oscillator pin (X2) must be floating. The counter advances on the negative-going transition of X1. A LOW level on $\overline{MR}$ resets the counter, stops the oscillator and sets the output buffer in the 3-State condition. $\overline{MR}$ can be left floating since an internal pull-up resistor will make the $\overline{MR}$ inactive. In the HCT version, the $\overline{MR}$ input and the two mode select pins S1 and S2 are TTL compatible, but the X1 input has CMOS input switching levels and may be driven by a TTL output using a pull-up resistor connected to V_{CC}.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C, $t_r = t_f$ = 6ns

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			HC	HCT	
t_{PLH} t_{PHL}	Propagation delay X1 to OUT (S1 = S2 = LOW)	C_L = 50pF; V_{CC} = 5V	8	8	ns
f_{max}	Maximum clock frequency		150	150	MHz
C_I	Input capacitance except X1 and X2		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package				pF

NOTES:

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = (C_{PD} \times V_{CC}^2 \times f_I) + (C_L + V_{CC}^2 \times f_O) + (I_{pull\text{-}up} \times V_{CC})$

where:

f_I = inputfrequency in MHz..
f_O = output frequency in MHz.
V_{CC} = Supply voltage in V.
C_L = Output load capacitance in pF.
$I_{pull\text{-}up}$ = Pull-up currents in µA.

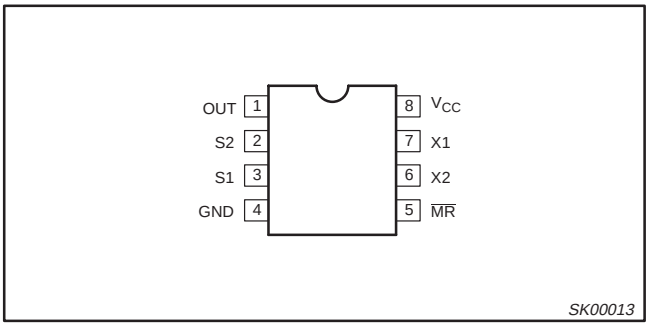
For HC and HCT an external clock is applied to X1 with:

$t_r = t_f \leq$ 6ns, V_I is GND to V_{CC}, $\overline{MR}$ = HIGH.
$I_{pull\text{-}up}$ is the summation of $-I_I$ (µA) of S1 and S2 inputs at the LOW state.

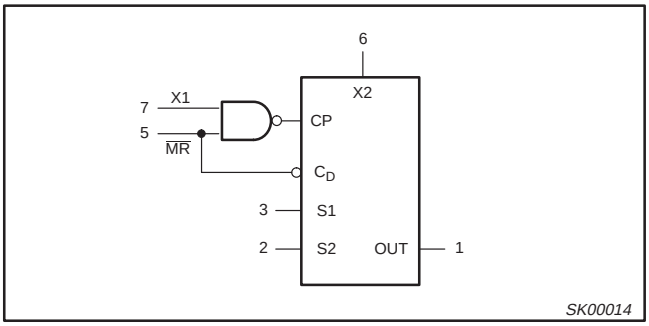
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER NUMBER	DWG NUMBER
8-Pin Plastic SO	0°C to +70°C	74HC/HCT9323A D	SOT96-1

PIN CONFIGURATION



IEC LOGIC SYMBOL



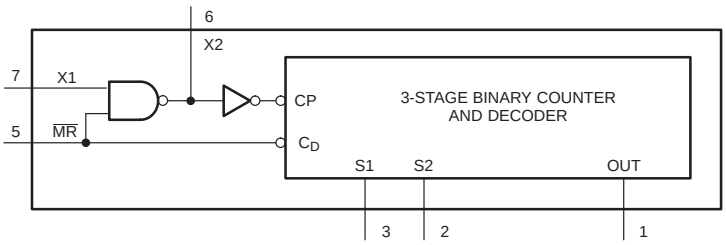
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OUT	Counter output
3, 2	S1-S2	Mode select inputs for divide by 1, 2, 4 or 8
4	GND	Ground (0V)
5	$\overline{MR}$	Master reset (active LOW)
6	X2	Oscillator pin
7	X1	Clock input/oscillator pin
8	V_{CC}	Positive supply voltage

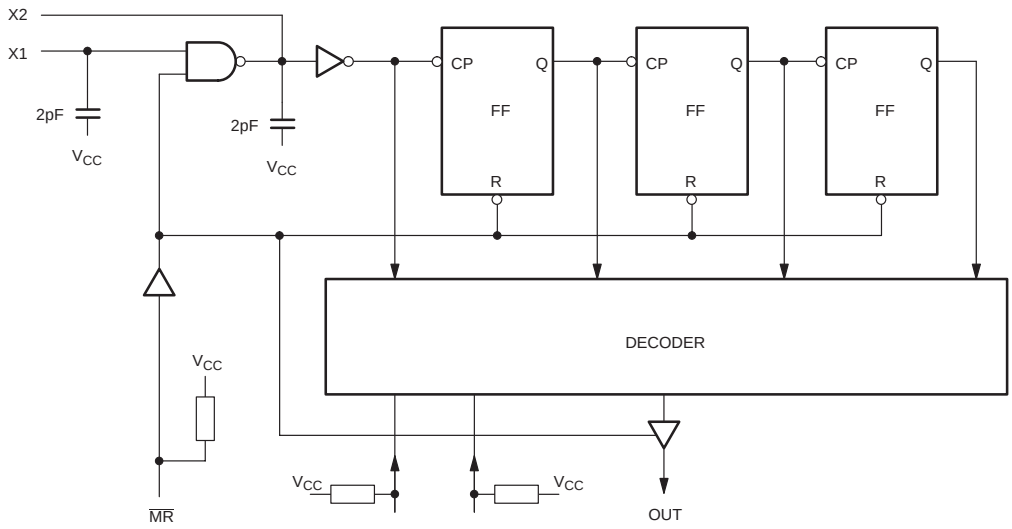
FUNCTION TABLE

INPUTS		OUTPUTS
S1	S2	OUT
0	0	f_I
0	1	$f_I/2$
1	0	$f_I/4$
1	1	$f_I/8$

FUNCTIONAL DIAGRAM



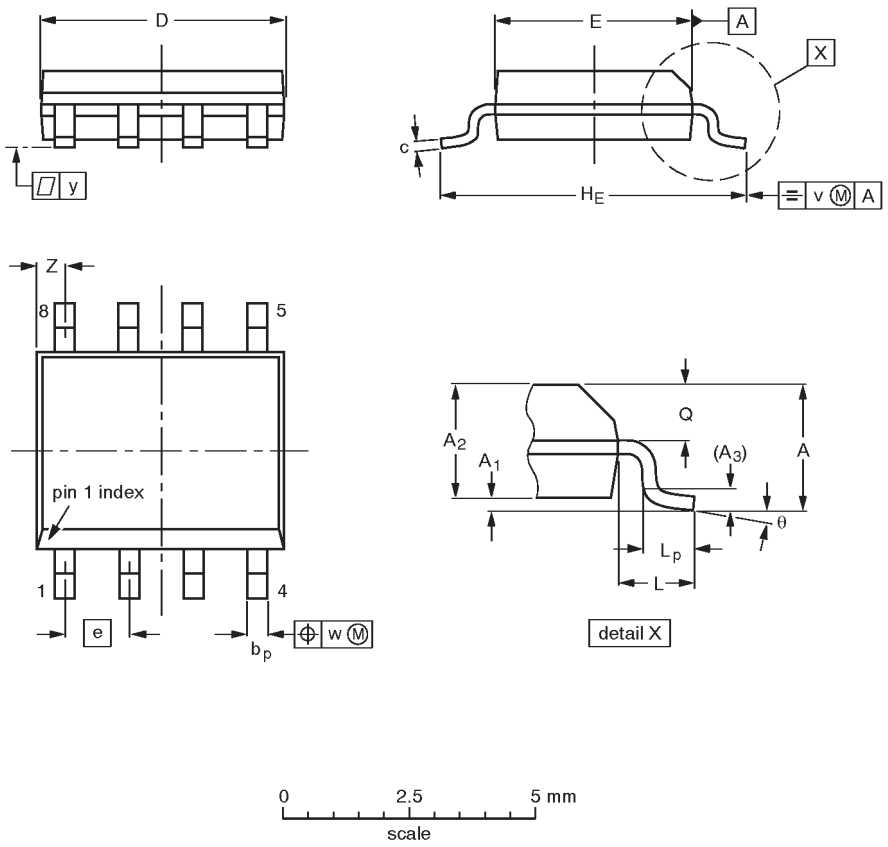
LOGIC DIAGRAM



Internal capacitors typical 2pF each, including stray capacitors on pins X1 and X2, total capacitance will be typical 7pF per pin

SK00016

SO8: plastic small outline package; 8 leads; body width 3.9mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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