Features

- **Driver Stages**
  - **Four DMOS 150 mA Low-side Relay Drivers with Current Limitation**
  - **One Gate Driver for External N-channel FET with Charge Pump and Bootstrap**
  - **Two Universal Outputs (10 mA High Side and 60 mA Low Side)**
  - **One 20 mA Warning Lamp Driver**
- **Power Supplies**
  - **5V/150 mA Linear Regulator**
  - **5V/30 mA Linear Regulator (also Active in Standby Mode)**
  - **Internal Power Supply**
  - **Switchable System Supply Voltage Output**
- **Monitoring and Protection**
  - **12V Monitoring**
  - **Watchdog with Reset**
  - **Two Comparators for Current Measurement**
  - **Adjustable Undervoltage Warning Level**
  - **Overtemperature Protection with Hysteresis**
  - **Two 5V Comparators**
  - **Wide Supply Voltage Range from 5.8V up to 26V**
  - **8-bit SPI Interface**
  - **Low Current Consumption in Standby Mode 80 µA**
  - **TTL and CMOS Compatible Inputs**
  - **2 kV ESD Protection**
  - **Transient Protection According to ISO/TR 7637-1 Level 4 (Except Load Dump)**

Pb Lead Free

Applications

As an Automotive Failsafe System IC, the ATA6814 is ideal for driver and monitoring functions in ambitious solutions with increased safety requests such as parking brakes, power steering, and other applications with DC motor control.

Automotive Failsafe System IC

ATA6814

Preliminary

Rev. 4849B–AUTO–09/05

1. Description

The ATA6814 is a monolithically-integrated multi-functional IC designed in Atmel's state-of-the-art 0.8 µm BCDMOS technology. With its built-in driver stages, voltage supplies and monitoring functions, it is an ideal cost saving failsafe system IC.

The communication with an external microcontroller is provided by an 8-bit SPI interface.

Four protected and current limited driver stages are available to control relays and additionally there is a gate driver including charge pump and bootstrap to control an external FET.

Three LEDs for status information can be controlled via three separate outputs: The high-side driver at pin OUTP has monitoring functions for overcurrent and current threshold. The low-side drivers at the pins WLN and OUTN also have monitoring functions for overcurrent, current threshold, and voltage monitoring.

Two internal bandgap references control and monitor two independent 5V supply voltages. In standby mode the internal IC-supply is provided by one of them; the other one is switched off, in order to reduce the power consumption to a minimum. All internal blocks are supplied by a specific internal voltage regulator.

The system supply voltage and all internally-generated voltages are monitored and in case of over or undervoltage all drivers are switched off. Via the SPI the system supply voltage can be switched to provide power for external components.

The car battery voltage (KL 30) is monitored by an adjustable monitoring function.

An oscillator with an external RC circuitry and a fully-integrated auxiliary oscillator which can be set via the pin RREF are the clock references for the watchdog and all other time constants. Both oscillators monitor each other.

The independent watchdog circuitry monitors the microcontroller's correct operation.

Two differential amplifiers support the use of external A/D converters for current measurement.

Two comparators are provided to monitor the 5V supply of external devices like sensors.

Figure 1-1. Block Diagram

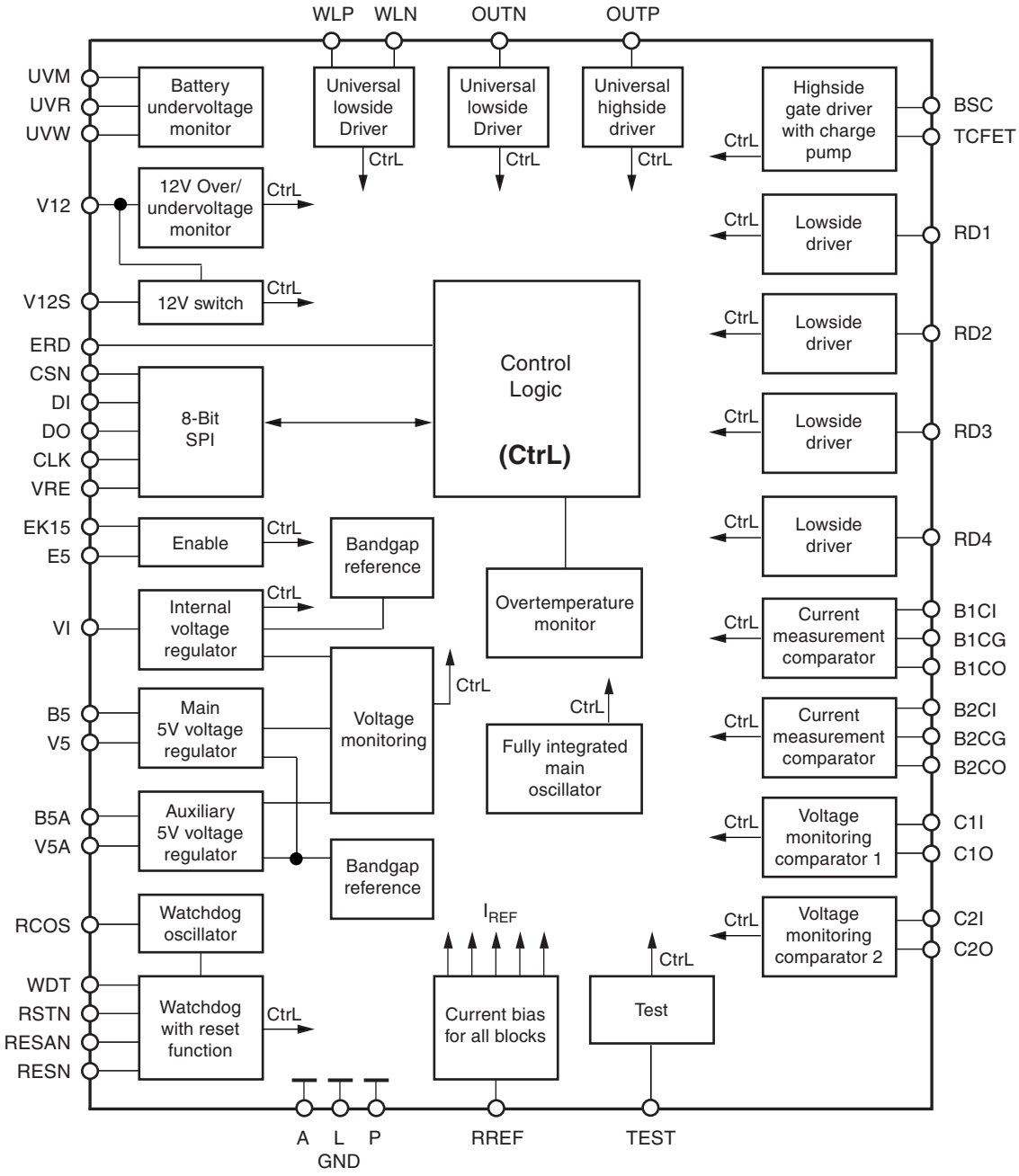
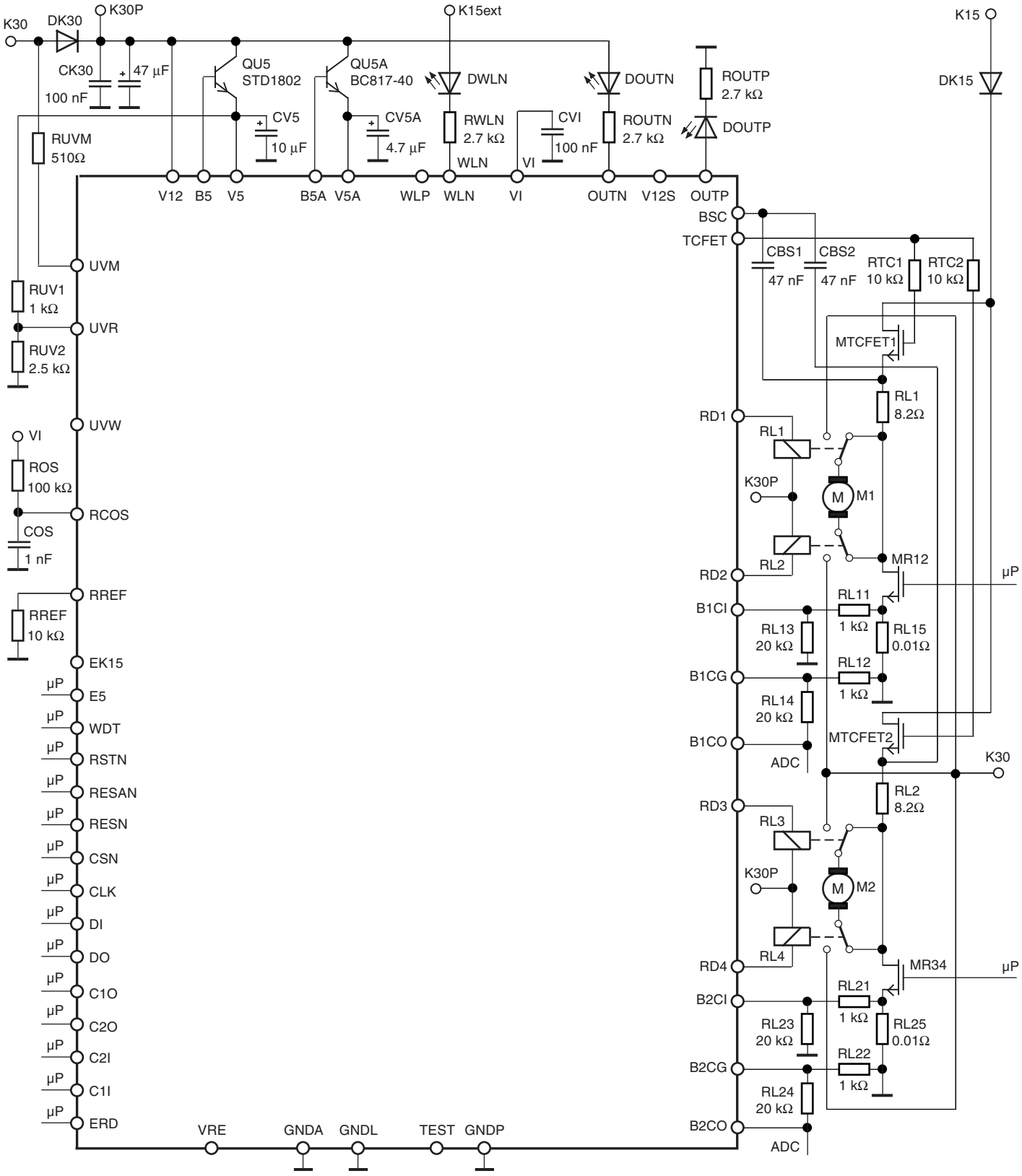


Figure 1-2. Application Circuit



2. Pin Configuration

Figure 2-1. Pinning QFN48

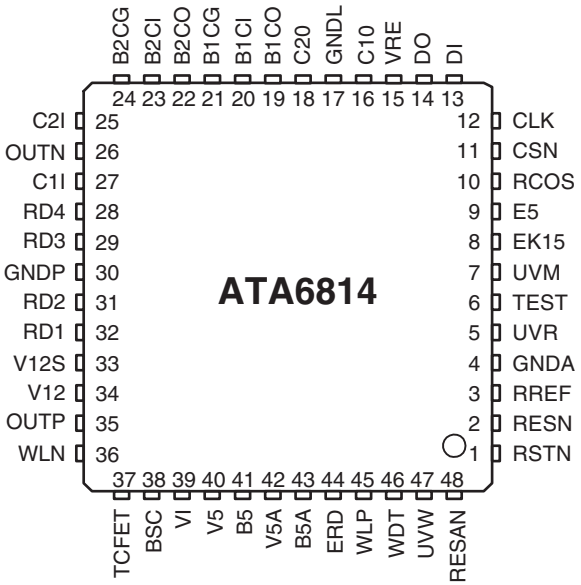


Table 2-1. Pin Description

Pin	Symbol	Function
1	RSTN	Reset input
2	RESN	Reset output
3	RREF	Reference resistor
4	GNDA	Analog ground
5	UVR	Undervoltage reference input
6	TEST	Test
7	UVM	Undervoltage measurement input
8	EK15	Enable (K15 based)
9	E5	Enable (5V based)
10	RCOS	Resistor-capacitor oscillator
11	CSN	Chip-select input
12	CLK	Clock input
13	DI	Data input
14	DO	Data output
15	VRE	External voltage regulator output
16	C1O	Comparator 1 output
17	GNDL	Logic ground
18	C2O	Comparator 2 output
19	B1CO	Bridge 1 current output
20	B1CI	Bridge 1 current input
21	B1CG	Bridge 1 current ground

Table 2-1. Pin Description (Continued)

Pin	Symbol	Function
22	B2CO	Bridge 2 current output
23	B2CI	Bridge 2 current input
24	B2CG	Bridge 2 current ground
25	C2I	Comparator 2 input
26	OUTN	Low-side driver output
27	C1I	Comparator 1 input
28	RD4	Relay driver 4 output
29	RD3	Relay driver 3 output
30	GNDP	Power ground
31	RD2	Relay driver 2 output
32	RD1	Relay driver 1 output
33	V12S	12V switch
34	V12	12V supply voltage
35	OUTP	High-side driver output
36	WLN	Warning lamp output
37	TCFET	Test current FET
38	BSC	Bootstrap capacitor
39	VI	Internal 5V supply
40	V5	5V supply
41	B5	Base 5V supply
42	V5A	Auxiliary 5V supply
43	B5A	Base auxiliary 5V supply
44	ERD	Enable relay driver input
45	WLP	Warning lamp polarity input
46	WDT	Watchdog trigger input
47	UVW	Undervoltage warning output
48	RESAN	Auxiliary reset output

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Condition	Symbol	Min.	Max.	Unit
Supply voltage		V12	–0.3	+26	V
Supply voltage	t < 500 ms	V12	–0.3	+45	V
Voltage at pins CLK, DI, E5, ERD, WDT, WLP, CSN, RSTN, VRE, DO, C1O, C2O, RESN, RESAN, UVR, UVW, RREF, VI, TEST, B1CI, B1CG, B1CO, B2CI, B2CG, B2CO, RCOS	V() ≤ V5 + 0.3V	V()	–0.3	+5.5	V
Current in pins CLK, DI, E5, ERD, WDT, WLP, CSN, RSTN, VRE, DO, C1O, C2O, RESN, RESAN, UVR, UVW, RREF, VI, TEST, B1CI, B1CG, B1CO, B2CI, B2CG, B2CO, RCOS		I()	–10	+10	mA
Voltage at RD1, RD2, RD3, RD4, WLN, OUTN, OUTP, EK15, BSC, TCFET, UVM		V()	–0.3	+45	V
Current in RD1, RD2, RD3, RD4, WLN, OUTN		I()	–150	+150	mA
Current in OUTP		I()	–10	+10	mA
Voltage at V5, V5A		V()	–0.3	+5.5	V
Current in V5		I()	–150	+10	mA
Current in V5A		I()	–50	+10	mA
Voltage at V12S		V()	–0.3	+45	V
Current in V12S		I()	–60	+10	mA
ESD protection at all pins	MIL-STD-883, Method 3015, HBM 100 pF discharged through 1.5 kΩ	Vd()		2	kV
Junction temperature	Operation	$T_{j,op}$	–40	+150	°C
	Peak	$T_{j,peak}$	–40	+165	°C
Storage temperature		T_s	–55	+125	°C

4. Thermal Resistance

Parameters	Condition	Symbol	Min.	Max.	Unit
Operating ambient temperature range		T_{amb}	–40	+105	°C
Thermal resistance, chip to case		R_{thJC}		10	K/W
Soldering temperature		T_{ms}		260	°C

5. Electrical Characteristics

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Total Device**								
1.1	Permissible supply voltage	All functions Reduced operation mode(1)		V12	6.5 5.8		26 6.5	V V	A
1.2	Supply current		V12	I(V12)			10	mA	A
1.3	Supply current	Standby, V12 = 14V, I(V5A) = –10 µA	V12	I(V12)			80	µA	A
1.4	Leakage current low	V() = 0V to V12, V12 = 14V	WLN, OUTN, RD1 to RD4	Ilk()lo,stb	–1		+1	µA	A
1.5	Leakage current high	V() = 0V to V12, V12 = 14V V(BSC) = 14V	OUTP, V12S, BSC	Ilk()hi,stb	–1		+1	µA	A
1.6	Supply current	All V5 based I/O pins open	V5	I(V5)			0.5	mA	A
1.7	Supply current	RESAN open	V5A	I(V5A)			50	µA	A
1.8	Pull-up current to V5	V() = 0.7 × V5	CSN	Ipu()	–100		–10	µA	A
1.9	Pull-up current to VI	V() = 0.7 × VI	RSTN	Ipu()	–100		–10	µA	A
1.10	Pull-up current to V5	V() = 0V	CSN	Ipu()	–200		–20	µA	A
1.11	Pull-up current to VI	V() = 0V	RSTN	Ipu()	–200		–20	µA	A
1.12	Pull-down current	V() = 0.2 × V5	CLK, DI, E5, ERD, WDT	Ipd()	10		100	µA	A
1.13	Pull-down current	V() = 0.2 × VI	WLP	Ipd()	10		100	µA	A
1.14	Pull-down current	V() = V5	CLK, DI, E5, ERD, WDT	Ipd()	20		200	µA	A
1.15	Pull-down current	V() = VI	WLP	Ipd()	20		200	µA	A
1.16	Pull-up voltage to V5	Vpu() = V() – V5, I() = –10 µA	CSN	Vpu()	–0.6			V	A
1.17	Pull-up voltage to VI	Vpu() = V() – VI, I() = –10 µA	RSTN	Vpu()	–0.6			V	A
1.18	Pull-down voltage	I() = 10 µA	CLK, DI, E5, ERD, WDT, WLP	Vpd()			0.6	V	A
1.19	Input threshold voltage high		CLK, CSN, DI, E5, ERD, RSTN, WDT, WLP	Vt()hi			2	V	A
1.20	Input threshold voltage low		CLK, CSN, DI, E5, ERD, RSTN, WDT, WLP	Vt()lo	0.85			V	A
1.21	Input hysteresis voltage	Vt()hys = Vt()hi – Vt()lo	CLK, CSN, DI, E5, ERD, RSTN, WDT, WLP	Vt()hys	0.2		1	V	A
1.22	Saturation voltage low	I() = 0.1 mA, outputs low	C1O, C2O, VRE, DO, RESAN, RESN, UVW	Vs()lo			0.2	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.23	Saturation voltage low	I() = 1.6 mA, outputs low	C1O, C2O, VRE, DO, RESAN, RESN, UVW	Vs()lo			0.4	V	A
1.24	Saturation voltage high	Vs() = V5 – V(), I() = –0.1 mA, outputs high	C1O, C2O, DO, RESN, UVW	Vs()hi			0.5	V	A
1.25	Saturation voltage high	Vs() = V5A – V(), I() = –0.1 mA, RESAN high	RESAN	Vs()hi			0.5	V	A
1.26	Saturation voltage high	Vs() = V5 – V(), I() = –1.6 mA, outputs high	C1O, C2O, DO, RESN, UVW	Vs()hi			1	V	A
1.27	Saturation voltage high	Vs() = V5A – V(), I() = –1.6 mA, RESAN high	RESAN	Vs()hi			1	V	A
1.28	Rise time	C_{load} = 10 pF, V() from low = 10% -> high = 90% V5	C1O, C2O, DO, RESN, UVW	tr()			200	ns	B
1.29	Rise time	C_{load} = 10 pF, V() from low = 10% -> high = 90% V5A	RESAN	tr()			200	ns	B
1.30	Fall time	C_{load} = 10 pF, V() from high = 90% -> low = 10% V5	C1O, C2O, DO, RESN, UVW	tf()			200	ns	B
1.31	Fall time	C_{load} = 10 pF, V() from high = 90% -> low = 10% V5A	RESAN	tf()			200	ns	B
1.32	Leakage current	DO = off, V() = 0V to V5	DO	I()lk	–10		+10	µA	A
1.33	Short circuit current low	V() = V5, pins = low	C1O, C2O, DO, RESN, UVW	Isc()lo	8		40	mA	A
1.34	Short circuit current low	V() = V5A, RESAN = low	RESAN	Isc()lo	8		40	mA	A
1.35	Short circuit current high	V() = 0V, pins = high	C1O, C2O, VRE, DO, RESAN, RESN, UVW	Isc()hi	–30		–8	mA	A
1.36	Saturation voltage high	Vs() = VI – V(), I() = –0.1 mA, VRE high	VRE	Vs()hi			0.5	V	A
1.37	Saturation voltage high	Vs() = VI – V(), I() = –1.6 mA, VRE high	VRE	Vs()hi			1	V	A
1.38	Short circuit current low	V() = VI, VRE = low	VRE	Isc()lo	8		40	mA	A
1.39	Rise time	C_{load} = 10 pF, V() from low = 10% -> high = 90% VI	VRE	tr()			200	ns	B
1.40	Fall time	C_{load} = 10 pF, V() from high = 90% -> low = 10% VI	VRE	tf()			200	ns	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2	**Bandgap, Bias**								
2.1	Voltage at RREF	RREF = 10 kΩ ±2%	RREF	V(RREF)	1.18	1.23	1.28	V	A
3	**Temperature Monitoring**								
3.1	Thermal shutdown temperature	Overcurrent in WLN, OUTN or OUTP for t > 200 µs		$T1_{off}$	120		145	°C	A
3.2	Thermal re-entry temperature	Overcurrent in WLN, OUTN or OUTP for t > 200 µs		$T1_{on}$	105		135	°C	A
3.3	Thermal hysteresis 1	$T1_{hys} = T1_{off} - T1_{on}$		$T1_{hys}$	5		20	°C	A
3.4	Thermal shutdown temperature			$T2_{off}$	140		165	°C	A
3.5	Thermal re-entry temperature			$T2_{on}$	125		155	°C	A
3.6	Thermal hysteresis 2	$T2_{hys} = T2_{off} - T2_{on}$		$T2_{hys}$	5	12	20	°C	A
4	**Enable/Standby**								
4.1	Input resistor		EK15	RiEK15	60	100	150	kΩ	A
4.2	Upper enable threshold		EK15	$VEK15_{on}$			2.5	V	A
4.3	Lower enable threshold		EK15	$VEK15_{off}$	1.5			V	A
4.4	Enable hysteresis		EK15	$VEK15_{hys}$	200		600	mV	A
4.5	Enable time based on watchdog oscillator period		EK15	te(EK15)	1		6		A
5	**V12 Voltage Monitoring**								
5.1	Lower undervoltage threshold		V12	VtU_{lo}	4.8			V	A
5.2	Upper undervoltage threshold		V12	VtU_{hi}			5.8	V	A
5.3	Undervoltage hysteresis	$VtU_{hys} = VtU_{hi} - VtU_{lo}$	V12	VtU_{hys}	200		600	mV	A
5.4	Lower overvoltage threshold		V12	VtO_{lo}	26			V	A
5.5	Upper overvoltage threshold		V12	VtO_{hi}			32	V	A
5.6	Overvoltage hysteresis	$VtO_{hys} = VtO_{hi} - VtO_{lo}$	V12	VtO_{hys}	0.5		1.8	V	A
5.7	Under/overvoltage filter time		V12	tfi	50		100	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6	**Linear Regulator**								
6.1	Output voltage	I(V5) = –150 mA to 0 mA, ß(NPN) > 120 mA, Uce,sat(NPN) < 0.8V, f_T > 100 MHz U_{be}(NPN) < 0.8V at –40°C, U_{be}(NPN) < 0.7V at 27°C, U_{be}(NPN) < 0.6V at 105°C	V5	V5	4.85	5	5.15	V	A
6.2	Line regulation	V12 = 8V to 18V, I(V5) = –150 mA	V5	$V5_{lir}$	–10		+10	mV	A
6.3	Load regulation	V12 = 14V, I(V5) = –50 mA to –150 mA	V5	$V5_{lor}$	–20		+20	mV	A
6.4	Allowed capacitor		V5	CV5	7		22	µF	C
6.5	Allowed capacitor		V5	ESR,CV5	0.5		10	Ω	C
6.6	Lower threshold undervoltage	RESN = low	V5	VtU(V5)low	4.5			V	A
6.7	Upper threshold undervoltage	RESN = high	V5	VtU(V5)high			4.8	V	A
6.8	Lower threshold overvoltage	RESN = high	V5	VtO(V5)low	5.2			V	A
6.9	Upper threshold overvoltage	RESN = low	V5	VtO(V5)high			5.5	V	A
6.10	Hysteresis Under/overvoltage		V5	Vt(V5)hys	50		200	mV	A
6.11	Under/overvoltage filter time		V5	tfi(V5)	8		30	µs	A
6.12	Short circuit current	V(B5) = 0V	B5	Isc(B5)	1.5		8	mA	A
6.13	Pull-down resistor	V(B5) = 1V	B5	Rpd(B5)	50		250	kΩ	A
6.14	Pull-down current	V(B5) = 6V	B5	Ipd(B5)	10		50	µA	A
6.15	Saturation voltage high	Vs(B5) = V12 – V(B5), V12 = 5.8V to 6.5V, I(B5) = –1.25 mA T_j = –40°C T_j = 27°C T_j = 105°C	B5	Vs(B5)high			 0.15 0.25 0.35	 V V V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	**V5A Auxiliary Linear Regulator**								
7.1	Output voltage	I(V5A) = –30 mA to 0 mA, ß(NPN) > 200, Uce,sat(NPN) < 1V, U_{be}(NPN) < 0.8V at –40°C, U_{be}(NPN) < 0.7V at 27°C, U_{be}(NPN) < 0.6V at 105°C	V5A	V5A	4.65	5	5.35	V	A
7.2	Line regulation	V12 = 8V to 18V, I(V5A) = –30 mA	V5A	$V5A_{lir}$	–10		+10	mV	A
7.3	Load regulation	V12 = 14V, I(V5A) = –10 mA to –30 mA	V5A	$V5A_{lor}$	–20		+20	mV	A
7.4	Minimum capacitor		V5A	CV5A	3.3		10	µF	C
7.5	Minimum capacitor		V5A	ESR,V5A	0.5		10	Ω	C
7.6	Lower threshold undervoltage	RESAN = low	V5A	VtU(V5A) low	4			V	A
7.7	Upper threshold undervoltage	RESAN = high	V5A	VtU(V5A) high			4.6	V	A
7.8	Lower threshold overvoltage	RESAN = high	V5A	VtO(V5A) low	5.4			V	A
7.9	Upper threshold overvoltage	RESAN = low	V5A	VtO(V5A) high			6	V	A
7.10	Hysteresis under/ overvoltage		V5A	Vt(V5A) hys	50		200	mV	A
7.11	Under/overvoltage filter time	Not in standby mode	V5A	tfi(V5A)	8		30	µs	A
7.12	Short circuit current	V(B5A) = 0V	B5A	Isc(B5A)	0.3		1.5	mA	A
7.13	Pull-down resistor	V(B5A) = 1V	B5A	Rpd(B5A)	50		250	kΩ	A
7.14	Pull-down current	V(B5A) = 6V	B5A	Ipd(B5A)	10		50	µA	A
7.15	Saturation voltage high	Vs(B5A) = V12 – V(B5A), V12 = 5.8V to 6.5V, I(B5A) = –150 µA T_j = –40°C T_j = 27°C T_j = 105°C	B5A	Vs(B5A) hi			 0.35 0.45 0.55	 V V V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**Internal Voltage Supply VI**								
8.1	Output voltage	C(VI) = 100 nF, I(VI) = –1 mA to 0 mA	VI	VI	4.35		5.35	V	A
8.2	Lower threshold undervoltage	RESN = low	VI	VtU_{lo}	3			V	A
8.3	Upper threshold undervoltage	RESN = high	VI	VtU_{hi}			4.3	V	A
8.4	Lower threshold overvoltage	RESN = high	VI	VtO_{lo}	5.4			V	A
8.5	Upper threshold overvoltage	RESN = low	VI	VtO_{hi}			6	V	A
8.6	Hysteresis undervoltage		VI	VtU_{hys}	0.4		1	V	A
8.7	Hysteresis overvoltage		VI	VtO_{hys}	50		200	mV	A
8.8	Short-circuit current	VI = 0V	VI	Isc()	20		150	mA	A
9	**Current Measurement, x = 1, 2**								
9.1	Output voltage low	I(BxCO) = 20 µA, BxCO = low	BxCO	Vs()lo	–10		+30	mV	A
9.2	Saturation voltage	I(BxCO) = –750 µA, BxCO = high, Vs(BxCO)hi = V5 – V(BxCO)	BxCO	Vs()hi			100	mV	A
9.3	Short-circuit current low	BxCO = low, V(BxCO) = V5	BxCO	Isc()lo	0.5		2	mA	A
9.4	Short-circuit current high	BxCO = high, V(BxCO) = 0V	BxCO	Isc()hi	–25		–2.5	mA	A
9.5	Input offset voltage V(BxCO) – (V(BxCI) – V(BxCG))	Vos() = V(BxCI) – V(BxCG) T_j = –40°C T_j = 27°C T_j = 105°C	BxCO	Vos()	–3.5 –3 –3.5		+3.5 +3 +3.5	mV mV mV	A
9.6	Leakage current	V(BxCI), V(BxCG) = –0.7V to +0.35V	BxCI BxCG	Ilk()	–1.75	–1	–0.25	µA	A
9.7	Input voltage range		BxCI BxCO	Vi()	–0.7		+0.35	V	A
9.8	Difference in leakage current	V(BxCI), V(BxCG) = –0.7V to +0.35V, dIlk(BxCI, BxCG),	B1CI, B1CG and B2CI, B2CG	dIlk()	–0.25		+0.25	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	**Relay Driver RDx, x = 1 to 4**								
10.1	Saturation voltage low	I(RDx) = 150 mA, T < T_{off} T_j = –40°C T_j = 27°C T_j = 105°C	RDx	Vs()lo			0.4 0.5 0.6	V V V	A
10.2	Short circuit current low	V(RDx) = 2V to V12, T < T_{off}	RDx	Isc()lo	250	300	400	mA	A
10.3	Leakage current	V(RDx) = 0V to 40V, T < T_{off}	RDx	Ilk()	–5		+5	µA	A
10.4	Free-wheeling voltage	I(RDx) = 10 mA, RDx = high, L = 0.2H	RDx	Vf()	42		60	V	A
11	**Watchdog**								
11.1	Upper window time	ROS = 100 kΩ ±1%, COS = 1 nF ±5%	WDT	Tu(WDT)	22.2	24.6	27	ms	A
11.2	Lower window time	ROS = 100 kΩ ±1%, COS = 1 nF ±5%	WDT	Tl(WDT)	16.4	18	19.8	ms	A
11.3	Watchdog timeout	ROS = 100 kΩ ±1%, COS = 1 nF ±5%	WDT	Tt(WDT)	59.7	64.6	71	ms	A
12	**Warning Lamp WLN**								
12.1	Saturation voltage low	I(WLN) = 20 mA, WLN = low	WLN	Vs()lo			0.4	V	A
12.2	Short-circuit current low	V(WLN) = 1V to V12, WLN = low	WLN	Isc()lo	20	30	50	mA	A
12.3	Threshold current high		WLN	Ith()hi			12	mA	A
12.4	Threshold current low		WLN	Ith()lo	8			mA	A
12.5	Hysteresis threshold current		WLN	Ithhys	0.25		1.5	mA	A
12.6	Threshold voltage detection		WLN	Vth()	2.25		2.75	V	A
12.7	Leakage current	V(WLN) = 0V to 40V, WLN = high	WLN	Ilk()	–10		+10	µA	A
12.8	Overcurrent filter time	I(WLN) > Isc(WLN)lo, T > $T1_{off}$	WLN	tfi()	100		200	µs	A
12.9	Fall time	V(WLN) from high = 90% -> low = 10% V12	WLN	tf()			10	µs	B
12.10	Free-wheeling voltage	I(WLN) = 10 mA, WLN = high, L = 10 µH	WLN	Vf()	42		60	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13	**Reset**								
13.1	Reset pulse duration		RESN	tl(RESN)	5.2		7.7	ms	A
13.2	Reset pulse duration		RESAN	tl(RESAN)	0.1		1	ms	A
14	**Low-side Driver OUTN**								
14.1	Saturation voltage low	I(OUTN) = 60 mA, OUTN = low, T < T_{off}	OUTN	Vs()lo			1.2	V	A
14.2	Short-circuit current low	V(OUTN) = 2V to V12, OUTN = low	OUTN	Isc()lo	60	90	120	mA	A
14.3	Threshold current high		OUTN	Ith()hi			12	mA	A
14.4	Threshold current low		OUTN	Ith()lo	8			mA	A
14.5	Hysteresis threshold current		OUTN	Ithhys	0.25		1.5	mA	A
14.6	Threshold voltage detection		OUTN	Vth()	2.25		2.75	V	A
14.7	Leakage current	V(OUTN) = 0V to 40V, OUTN = high	OUTN	Ilk()	–10		+10	µA	A
14.8	Overcurrent filter time	I(OUTN) > Isc(OUTN)lo, T > $T1_{off}$	OUTN	tfi()	100		200	µs	A
14.9	Fall time	V(OUTN) from high = 90% -> low = 10% V12	OUTN	tf()			10	µs	B
14.10	Free wheeling voltage	I(OUTN) = 10 mA, OUTN = high, L = 10 µH	OUTN	Vf	42		60	V	A
15	**High-side Driver OUTP**								
15.1	Saturation voltage high	Vs(OUTP) = V12 V(OUTP), I(OUTP) = –10 mA, OUTP = high, T < T_{off}	OUTP	Vs()hi			1	V	A
15.2	Short-circuit current	V(OUTP) = 0V to V12 – 2V, OUTP = high	OUTP	Isc()hi	–25	–15	–10	mA	A
15.3	Threshold current high		OUTP	Ith()hi	–5			mA	A
15.4	Threshold current low		OUTP	Ith()lo			–2	mA	A
15.5	Hysteresis threshold current		OUTP	Ithhys	–1		–0.1	mA	A
15.6	Leakage current	V(OUTP) = 0V to V12, OUTP = low	OUTP	Ilk()	–10		+10	µA	A
15.7	Overcurrent filter time	I(OUTP) > Isc(OUTP)hi, T > $T1_{off}$	OUTP	tfi()	100		200	µs	A
15.8	Rise time	V(OUTP) from low = 10% -> high = 90% V12	OUTP	tr()			10	µs	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16	**Watchdog Oscillator RCOS**								
16.1	Oscillator frequency	ROS = 100 kΩ ±1%, COS = 1 nF ±5%	RCOS	f_{OSC}	9	10	11	kHz	A
16.2	Permissible frequency range	No reset, f – 1/(2 × ROS × COS)	RCOS	f_{OSC}	0.9		55	kHz	A
16.3	Permissible resistor	COS = 1 nF	RCOS	ROS	20		100	kΩ	A
16.4	Permissible capacitor	ROS = 100 kΩ	RCOS	COS	1		10	nF	A
16.5	Short-circuit current low	V(RCOS) = VI	RCOS	Isc()lo	1		4	mA	A
16.6	Leakage current	V(RCOS) = 0% to 63.2% VI	RCOS	Ilk()	–5		+5	µA	A
17	**Main Oscillator**								
17.1	Main oscillator frequency	RREF = 10 kΩ ±2%		f_{mosC}	82.5	100	120	kHz	A
18	**Comparator CxI, x = 1, 2**								
18.1	Threshold voltage detection		CxI	Vth(CxI)	1.1	1.23	1.4	V	A
18.2	Leakage current	V(CxI) = 0V to V5	CxI	Ilk(CxI)	–10		+10	µA	A
18.3	Propagation delay	dv/dt > 1V/µs	CxI	tpd(Cx)			20	µs	B
19	**TCFET**								
19.1	Output voltage	Vo(TCFET) = V(TCFET) – V12, V12 > 6.5V, I(TCFET) = –20 µA to 0 µA	TCFET	Vo()	4.5		10	V	A
19.2	Short-circuit current high	V(BSC) = 0V to V12 – 3V	BSC	Isc(BSC)hi	1		25	mA	A
19.3	Saturation voltage high	Vd() = V(BSC) – V(TCFET), TCFET = high, I(TCFET) = –20 µA	BSC	Vs()hi			1.5	V	A
19.4	Saturation voltage low	TCFET = low, I(TCFET) = 50 µA	TCFET	Vs()lo			200	mV	A
19.5	Short-circuit current high	V(TCFET) = 0V, TCFET = high	TCFET	Isc()hi	–250	–50	–25	µA	A
19.6	Short-circuit current low	V(TCFET) = 2V to V12, TCFET = low	TCFET	Isc()lo	100	150	200	µA	A
19.7	Leakage current	V(BSC) = V12 to 36V, TCFET = low	BSC	Ilk()	–10		+10	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

5. Electrical Characteristics (Continued)

Operating conditions: V12 = 6.5V to 26V, V5 = 5V ±3%, RREF = 10 kΩ ±2%, T_j = –40°C to 150°C, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
20	**V12S Switch**								
20.1	Saturation voltage high	Vs(V12S) = V12 – V(12S), V12S = high, T < $T2_{off}$, I(V12S) = –60 mA	V12S	Vs()hi	0.36		1.2	V	A
20.2	Short-circuit current high	V(V12S) = 0V to V12 – 2V, V12S = high	V12S	Isc()hi	–150	–90	–60	mA	A
20.3	Leakage current	V(V12S) = 0V to V12, V12S = low	V12S	Ilk()	–10		+10	µA	A
21	**UVM Voltage Monitoring**								
21.1	Input voltage range		UVM	Vir(UVR)	0.3 × V5		0.9 × V5		A
21.2	Threshold on V(K30, UVM)	R(K30, UVM) = 511Ω ±2%	UVM	Vt(K30, UVM)	2.9 × UVR	3.0 × UVR	3.1 × UVR		A
21.3	Input resistor		UVM	Ri(UVM)	60	100	150	kΩ	A
21.4	Undervoltage reference hysteresis based on V(K30, UVM)		UVM	Vt(UVR) hys	0.02 × UVR		0.06 × UVR		A
21.5	Leakage current	V(UVR) = 0V to V5	UVR	Ilk(UVR)	–5		+5	µA	A
21.6	Leakage current	V(UVM) = 0V to V12, standby	UVM	Ilk(UVM) stb	–5		+5	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Reduced operation mode means either
- R_{DSON} of drivers could be higher than specified or
- Voltage at pin TCFET could be beyond specified limits

6. Operating Conditions: SPI Interface

V12 = 5.8V to 26V; T_{amb} = –40°C to 105°C

Parameters	Symbol	Min.	Max.	Unit
Cycle time	t_{cycle}	0.5	12.5	µs
Low cycle time	$t_{cycle,lo}$	150		ns
High cycle time	$t_{cycle,hi}$	150		ns
Setup time: DI stable before CLK high to low	t_{setup}	100		ns
Hold time: DI stable after CLK high to low	t_{hold}	100		ns
Access time: DO stable after CLK high to low	t_{access}	100		ns
Valid time: DO stable before CLK high to low	t_{valid}	100		ns

7. Functional Description

7.1 Bandgaps

For voltage monitoring and as references for various voltage regulators, two independent bandgaps are used. The bandgaps for the generation and monitoring of the internal supply (V5 and V5A) are used in cross-over mode.

7.2 Bias

The external resistor at RREF defines a current reference for all blocks and determines main oscillator frequency. The current through the external resistor is monitored and in case of malfunction (pin open or short to ground; current is less than 0.25 times or greater than 8 times nominal value), a bias failure is detected (see Table 7-9 on page 25).

7.3 Temperature Monitoring

To protect the circuit from extensive temperature in error condition, two temperature levels are implemented to switch off various blocks. At the lower temperature level, the outputs WLN, OUTN or OUTP are switched off after a debounce time, if the corresponding driver is in current limitation.

The Warning Lamp is switched on above the upper temperature level. All other drivers and the linear regulators will switch off. If the temperature level falls below the shutdown temperature (hysteresis), all drivers except TCFET and the relay drivers will go to their previous state.

7.4 Enable/Standby

The power consumption of ATA6814 is reduced to a minimum via inputs E5 or EK15 (sleep mode). With the signal TEN via SPI command, the inputs E5 and EK15 can be overwritten and the ATA6814 will stay active (keep-alive function). The status of EK15 can be read via SPI.

Table 7-1. Enable/Standby Table

E5	EK15	TEN (SPI)	ATA6814
High	x	x	Active
x	High	x	Active
Low	Low	High	Active
Low	Low	Low	Standby

7.5 V12 Voltage Monitoring

The system supply is checked for overvoltage and undervoltage at the internal voltage divider. If the voltage exceeds the limits, the drivers are switched off and a reset at RESN and RESAN is generated (see Table 7-9 on page 25).

7.6 5V Linear Regulators

The ATA6814 offers two independent 5V supplies. The main supply (V5) is available only in active mode while the auxiliary 5V supply (V5A) is active all the time. The ATA6814 activates the basis of external bipolar transistors via pins B5 and B5A. The currents of the regulators V5 (150 mA) and V5A (30 mA), defined in the datasheet, can only be achieved if the external transistors fulfil certain requirements in terms of current amplification and transit frequency. Especially for V12 = 5.8V a low saturation voltage of B5 and B5A in combination with the forward diode voltage and a low saturation voltage (Uce,sat) of the external bipolar transistors is required. For fast load changes at V5 a high transit frequency is necessary (typically f_T > 100 MHz).

For voltage monitoring and as references for the voltage regulators two independent bandgaps are used. The voltage monitoring functions of V5 and V5A generate a reset pulse at RESN and RESAN if the limits are exceeded (see Table 7-9 on page 25). For internal voltage supply, an additional linear regulator (VI) is implemented.

7.7 Current Measurement

The ATA6814 contains two differential amplifiers for current measurement. The input signal of each amplifier is a voltage drop over an external current sense resistor. The amplification, defined by the ratio of external resistors, provides a reasonable signal for the following A/D converter. The output is limited to V5.

7.8 Relay Driver

The ATA6814 features four current-limited relay drivers for motor direction control relays. The relays are controlled by an SPI command and the input of the enable relay driver (ERD). Error conditions disable the relays permanently (see Table 7-9 on page 25).

Table 7-2. Relay Status Table

TRD1 (SPI)	TRD2 (SPI)	ERD	RD1	RD2
Low	Low	x	Open drain	Open drain
Low	High	High	Open drain	Low
High	Low	High	Low	Open drain
High	High	High	Open drain	Open drain
x	x	Low	Open drain	Open drain

Table 7-3. Relay Status Table

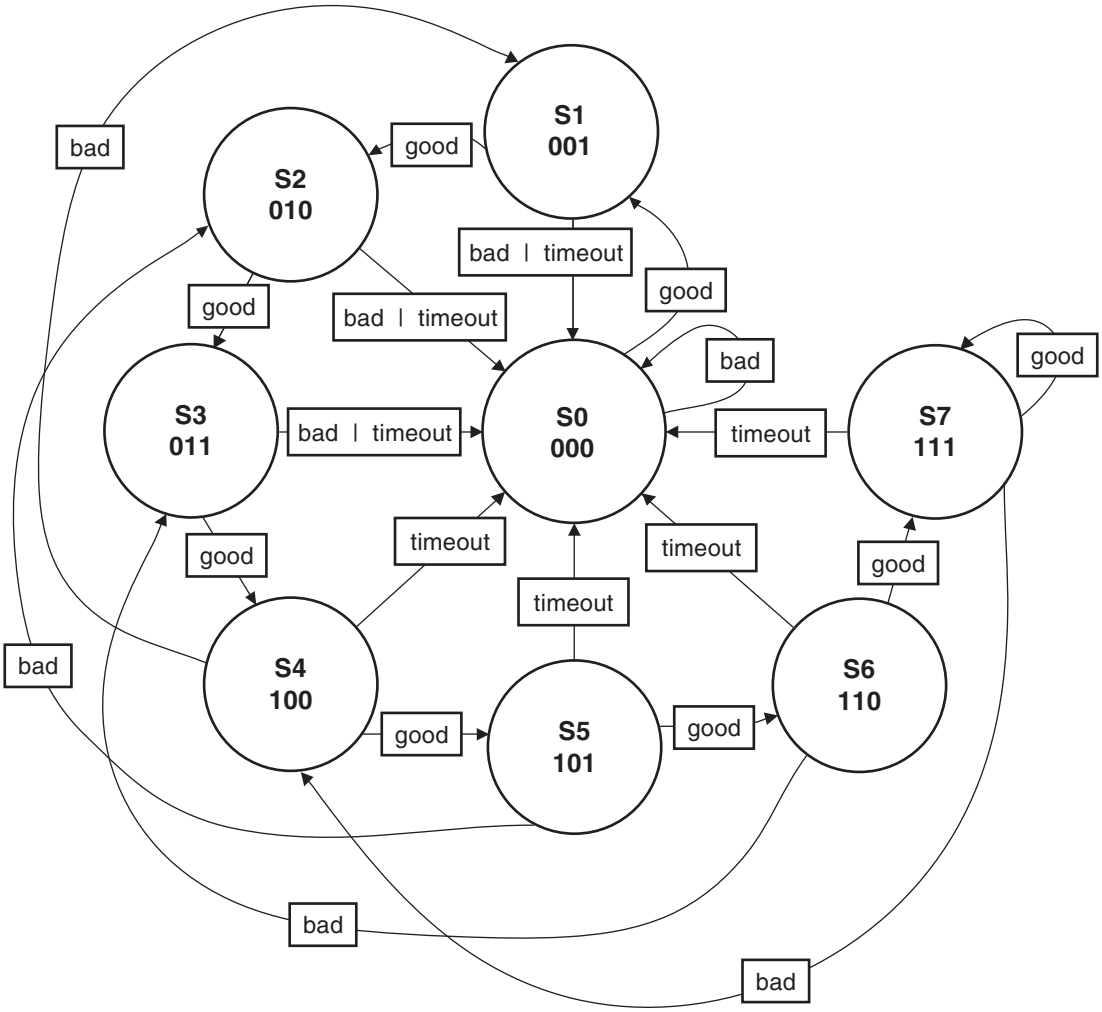
TRD3 (SPI)	TRD4 (SPI)	ERD	RD3	RD4
Low	Low	x	Open drain	Open drain
Low	High	High	Open drain	Low
High	Low	High	Low	Open drain
High	High	High	Open drain	Open drain
x	x	Low	Open drain	Open drain

Note: The simultaneous activation of the relay drivers RD1 and RD4 or RD2 and RD3 is not possible (see Table 7-2 and Table 7-3). This feature ensures that if ATA6814 is used in DC motor application, the motors can only operate in the same direction.

7.9 Watchdog

The open loop watchdog (window comparator) compares each time interval between a falling and a rising edge with a given reference time interval. The lower window time is between $90 \times t_{WD}$ and $91 \times t_{WD}$ and the upper window time is between $122 \times t_{WD}$ and $123 \times t_{WD}$ ($t_{WD} = 2/f_{OSC}$). The watchdog includes an error counter WDC(2:0) which is incremented by one when there are valid trigger events and decremented by three when there are watchdog errors. If the counter reaches a value of zero (state S0: 000), the warning lamp will be switched on. Relay drivers, TCFET-, low- and high-side drivers are disabled. With a counter value greater than or equal to seven (state S7: 111), the watchdog stops affecting the drivers. In the case of a watchdog timeout ($322 \times t_{WD}$ to $323 \times t_{WD}$), the error counter is immediately set to zero. The initial state of the watchdog counter after power-up or if RESN is low is 110 (state S6). The watchdog can be reset by RSTN.

Figure 7-1. State Diagram



7.10 Warning Lamp

The ATA6814 features a watchdog-controlled output, WLN, which can be used to switch a warning lamp. Depending on the warning lamp polarity pin (WLP), the warning lamp output is switched either to low level or to open drain, when a *Warning lamp request* (that is, *On* in Table 7-9 on page 25, column *WLN*) occurs or the corresponding SPI command is transmitted. For the behavior of WLN output refer to Table 7-4. The driver is short-circuit proof and will switch off after a debounce time. An activation of the warning lamp due to *Warning lamp request* is suppressed for $768 \times t_{WD}$ after wake-up to avoid a flickering of the warning lamp during the start-up phase (exception: lower thermal threshold level reached). The driver also has a current sensor and a voltage monitoring which sets SPI flags if the corresponding thresholds are reached.

Warnlamp is open drain during suppression time after wake-up. If the oscillator does not work 4 ms after start up, the internal oscillator watchdog timeout is reached and the warning lamp is switched on.

Table 7-4. Warning Lamp Status Table

Warnlamp Request	TWLN (SPI)	Overcurrent in WLN Occurred	Thermal Threshold #1 Reached	Suppression Time After Wake-up/VI Reset	V12	WLP	WLN
Yes	x	x	No	$t < 768 \times t_{WD}$	> 4.8V	Low	Open drain
Yes	x	x	No	$t > 768 \times t_{WD}$	> 4.8V	Low	Low
Yes	x	No	Yes	$t < 768 \times t_{WD}$	> 4.8V	Low	Open drain
Yes	x	No	Yes	$t > 768 \times t_{WD}$	> 4.8V	Low	Low
No	High	x	No	$t > 768 \times t_{WD}$	> 4.8V	Low	Low
No	Low	x	No	x	> 4.8V	Low	Open drain
Yes	x	Yes	Yes	x	> 4.8V	Low	Open drain
Yes	x	x	No	x	> 4.8V	High	Open drain
Yes	x	No	Yes	x	> 4.8V	High	Open drain
No	High	x	No	$t > 768 \times t_{WD}$	> 4.8V	High	Low
No	Low	x	No	x	> 4.8V	High	Open drain
No	High	Yes	Yes	x	> 4.8V	High	Open drain
No	High	No	Yes	x	> 4.8V	x	Open drain
x	x	x	x	x	< 4.8V	x	Open drain

7.11 Reset

When V12, VI, V5 or V5A are beyond their corresponding normal operating range or the temperature has reached the upper temperature level, a reset is indicated at the outputs RESN ($640 \times t_{mos}$; $t_{mos} = 1/f_{mos}$) and RESAN. Additionally, RESAN can be activated by an SPI command. Via input RSTN, the SPI Interface and the watchdog can be reset by an external signal (see Table 7-9 on page 25).

7.12 SPI Interface

The ATA6814 supports an 8-bit SPI interface to communicate with the microprocessor. The MSB is transmitted first. There are two status registers (address 0xxxxx01 and 0xxxxx10) and two control registers (address 1xxxxx01 and 1xxxxx10).

Table 7-5. Status Register 0xxxxx01 Request by Microprocessor

Bit	Name	Meaning	Function
7	C1O	Comparator 1 output	0: comparator C1I below threshold 1: comparator C1I above threshold
6	EK15S	EK15 status	0: EK15 below threshold 1: EK15 above threshold
5	WLPS	Warnlamp polarity status	0: pin WLP = low 1: pin WLP = high
4	OTS	Overtemperature status	0: normal operation 1: overtemperature present or overtemperature detection switched off
3	WDOK	Watchdog status	0: watchdog OK 1: watchdog failure
2:0	WDC(2:0)	Watchdog counter bit 2:0	Status of watchdog counter

Table 7-6. Status Register 0xxxxx10 Request by Microprocessor

Bit	Name	Meaning	Function
7	WLNOC	Warnlamp overcurrent	0: no overcurrent 1: overcurrent
6	ONOC	OUTN overcurrent	0: no overcurrent 1: overcurrent
5	OPOC	OUTP overcurrent	0: no overcurrent 1: overcurrent
4	WLNCS	Warnlamp current status	0: current below threshold 1: current above threshold
3	ONCS	OUTN current status	0: current below threshold 1: current above threshold
2	OPCS	OUTP current status	0: current below threshold 1: current above threshold
1	WLNVS	Warnlamp voltage status	0: voltage below threshold 1: voltage above threshold
0	ONVS	OUTN voltage status	0: voltage below threshold 1: voltage above threshold

Table 7-7. Control Register 1xxxxx01 Sent by Microprocessor

Bit	Name	Meaning	Function	Comment
7	TWLN	Trigger warning lamp	**0: WLN = off** 1: WLN = on	See Table 7-4 on page 21 and Table 7-9 on page 25
6	TOUTN	Trigger OUTN	**0: OUTN = off** 1: OUTN = on	See Table 7-10 and Table 7-11 on page 26
5	TOUTP	Trigger OUTP	**0: OUTP = off** 1: OUTP = on	See Table 7-10 and Table 7-11 on page 26
4	TEN	Trigger enable (keep alive)	**0: no keep alive** 1: keep alive	See Table 7-1 on page 18
3	TV12S	Trigger V12 switch	**0: V12S = off** 1: V12S = V12	Used in Testmode 3 see Table 7-9 on page 25
2	TUVR	Trigger undervoltage reference	**0: if UVM < 3 × UVR => UVW = low** **0: if UVM > 3 × UVR => UVW = high** 1: UVW = low	
1	–	–	–	No function
0	OTDE	Overtemperature detection enable	0: temperature detection off **1: temperature detection on**	Set OTS = high if overtemperature => OTS = high, else low

Note: **Bold:** default state after reset by RSTN = low

Table 7-8. Control Register 1xxxxx10 Sent by Microprocessor

Bit	Name	Meaning	Function	Comment
7	TTCFET	Trigger test current FET	**0: TCFET = off** 1: TCFET = on	See Table 7-9 on page 25
6	TRESAN	Trigger RESAN	**0: default** 1: RESAN = reset (low)	
5	–	–	–	No function
4	TRD4	Trigger relay driver 4	**0: RD4 = off** 1: RD4 = on if RD3 = off	See Table 7-2 on page 19, Table 7-3 on page 19 and Table 7-9 on page 25
3	TRD3	Trigger relay driver 3	**0: RD3 = off** 1: RD3 = on if RD4 = off	
2	TRD2	Trigger relay driver 2	**0: RD2 = off** 1: RD2 = on if RD1 = off	
1	TRD1	Trigger relay driver 1	**0: RD1 = off** 1: RD1 = on if RD2 = off	
0	–	–	–	No function

Note: **Bold:** default state after reset by RSTN = low

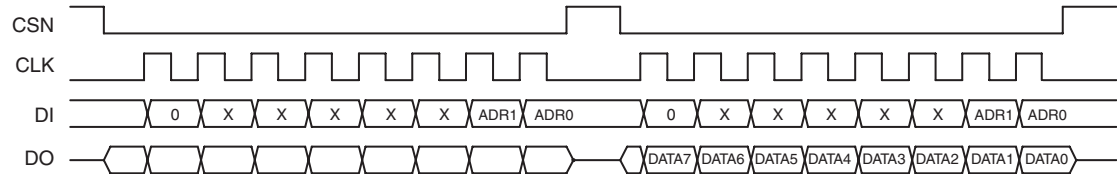
For operation of SPI communication see the following timing diagrams (see Figure 7-2 and Figure 7-3 on page 24).

With a low signal at CSN, the ATA6814 will be selected for communication by the microprocessor. With clock pulses at CLK, the address and data transfer will be synchronized. DI is the input for address and data from the microprocessor to ATA6814. The data must be valid at the falling edge of the CLK pin. DO transfers data from ATA6814 to the microprocessor.

The request command structure (to read a status register of ATA6814) consists of a two-byte transmission. The control command structure (to write a control register of ATA6814) consists of a three-byte transmission with eight clock pulses each and a low/high transition at CSN. The first byte is for identification.

All request command ID bytes shall have a “0” in their most significant bit. The address is transmitted by the last two bits. In the second byte (which can be a dummy byte (0x00) or next command), the status register corresponding to the address of the first byte will be sent by DO. At start-up, the returned value when the first command is sent will be zero (no 'last command' available).

Figure 7-2. Request Command Structure (Read Register)

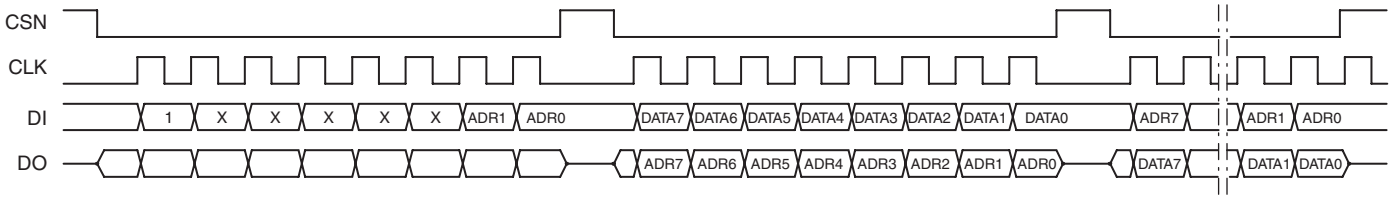


All control command ID bytes shall have a “1” in their most significant bit. The address is transmitted by the last two bits. The second byte is the data byte which contains the control data for the send command.

With the second low to high transition of CSN the data is stored in ATA6814.

The SPI logic monitors for faulty communication. To check which data is received at ATA6814 in the second and third clock cycle, the address and data are sent back to the microprocessor and tested to verify that the transmission was correct. The first data byte at DO is the response byte of the last command while the third DI byte is the address for the next data. If there is no next command, the address can be set to 0x00.

Figure 7-3. Control Command Structure (Write Register)



The 8 CLK pulses must be received when CSN is triggered, otherwise the address and/or data will be ignored and zeros will be returned on DO.

The minimum time for receiving during CSN = low is $t \leq 100$ µs; otherwise, a timeout expires and the receiving is stopped. Any received data is ignored. Therefore, the minimum clock frequency is 80 kHz for SPI transmission.

7.13 External Voltage Regulator VRE

The ATA6814 can control an external voltage regulator with enable input. The VRE output provides the same logic as for the V5 regulator (see Table 7-9). For V5 voltage monitoring, the external generated voltage must be connected to V5.

Table 7-9. Logic Table

Event	VI	V5 VRE	V5A	SPI Info	WLN	RD1 to RD4	RESN	RESAN	V12S	OUTx x = N,P	TCFET
Standby	Off	Off	On	–	Off	Off	–	No reset	Off	Off	Off
V12 undervoltage	On	Off	Off	No	Off	Off	Reset	Reset	Off	Off	Off
VI undervoltage	On	Off	On	No	Off	Off	Reset	No reset	Off	Off	Off
VI overvoltage	On	Off	On	No	On	Off	Reset	No reset	Off	Off	Off
Oscillator/bias failure	On	Off	Off	No	On	Off	Reset	Reset	Off	Off	Off
V12 overvoltage	On	Off	Off	No	On	Off	Reset	Reset	Off	Off	Off
Upper thermal threshold	On	On	On	Yes	On(4)	Off	Reset	Reset	Off(5)	Off	Off
Reset by RSTN	On	On	On	No	On	Off	No reset	No reset	Off	Off	Off
V5 out of range	On	On	On	No	On	Off	Reset	No reset	Off	Off	Off
V5A out of range	On	On	On	No	On	Off	No reset	Reset	Off	Off	Off
Short circuit WLN (overcurrent)	On	On	On	Yes	Off(1)	On/Off	No reset	No reset	On/Off	On/Off	On/Off
Short circuit OUTx (overcurrent)	On	On	On	Yes	Off	On/Off	No reset	No reset	On/Off	On/Off(1)	On/Off
Watchdog error	On	On	On	Yes	On	Off	No reset	No reset	On/Off	Off	Off
Off mode	–	–	–	–	–	Perm(3)	–	–	Temp(2)	Temp	Perm

Note:
1. Corresponding driver is switched off if thermal threshold number 1 is reached
2. Temp = temporary state, recovery when event condition is removed, except VI out of over-/undervoltage, thermal threshold number 2 reached or reset by RSTN
3. Perm = permanent state, no recovery when event condition is removed, must be re-engaged by SPI command
4. If no overcurrent in WLN
5. Not testable

7.14 Low-/High-side Driver

ATA6814 features two multipurpose outputs, a low-side driver OUTN and a high-side driver OUTP. Both drivers are controlled via SPI and are short-circuit proof (they will switch off after a debounce time if a short circuit is detected). During a short-circuit condition the corresponding SPI flag is set. The drivers are disabled by a watchdog error or during the reset phase. Both drivers also have an current sensor and OUTN has a voltage monitor which sets SPI flags if the corresponding thresholds are reached.

Table 7-10. Logic Table for Low-side Driver

TOUTN (SPI)	Overcurrent and Thermal Threshold Number 1 Reached	Watchdog	OUTN
High	No	OK	Low
Low	No	OK	Open drain
x	No	Error	Open drain
x	Yes	x	Open drain

Table 7-11. Logic Table for High-side Driver

TOUTP (SPI)	Overcurrent and Thermal Threshold Number 1 Reached	Watchdog	OUTP
High	No	OK	High
Low	No	OK	Open drain
x	No	Error	Open drain
x	Yes	x	Open drain

7.15 Oscillators

The watchdog oscillator provides an internal frequency of f_{WD} = 5 kHz ±10% given by external components.

R_{OS} = 100 kΩ ±1% and C_{OS} = 1 nF ±5% for the watchdog. For failsafe reasons, the clock frequency is internally monitored by an oscillator with RREF = 10 kΩ running at f_{OSC} = 100 kHz ±20%. This oscillator determines all other time constants. The watchdog oscillator frequency can be adjusted by a factor of five with the components R_{OS} and C_{OS} according to the formula: $f_{WD} = 1/t_{WD}$ where

$$t_{WD} = 2 \times R_{OS} \times C_{OS} \times \left(1 + \frac{0.632 \times VI}{I_{SC} \times R_{OS} - 0.684 \times VI}\right)$$

The first term describes charging the external RC, and the second term describes discharging.

With R_{OS} = 100 kΩ and C_{OS} = 1 nF the period of RCOS will result to typically $t_{osc} = 100 \times (1 + 0.012)$ µs.

f_{WD} is half of the frequency measured externally at the RCOS pin.

An oscillator failure generated by the oscillator watchdog occurs if the period of RCOS is smaller than t_{OSC} or greater than 200 × t_{OSC}, $f_{OSC} = 1/t_{OSC}$.

For oscillator failure, see Table 7-9 on page 25.

7.16 12V Switch

Via an SPI command, the voltage at pin V12 can be switched to pin V12S (see Table 7-9 on page 25). The 12V switch has a current limitation.

7.17 Comparator

The ATA6814 has two comparators. They compare inputs CxI in reference to the bandgap voltage. There are no internal pull-ups or pull-downs. The output is a V5-based push-pull stage. A hysteresis can be implemented by external resistors. Additionally, the output of comparator number 1 can be read out via SPI.

7.18 TCFET Driver

The ATA6814 features a circuit to drive an external N-channel FET. The control voltage is generated by a charge pump with bootstrap circuit for faster power-up behavior. Activation is done by an SPI command (see Table 7-9 on page 25).

7.19 UVM Voltage Monitoring

An undervoltage warning is indicated at output UVW if V12 falls below 3 × UVR. This reference-voltage level can be adjusted by an external resistor divider. The undervoltage warning can be tested with an SPI command.

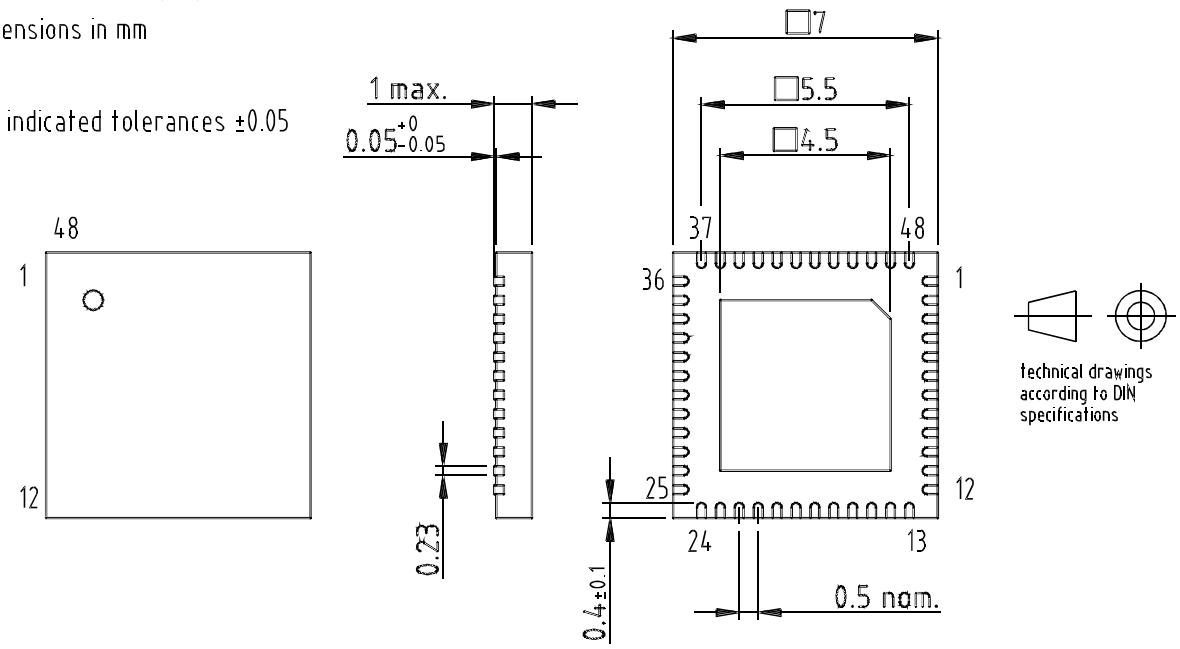
8. Ordering Information

Extended Type Number	Package	Remarks
ATA6814-PLSW	QFN48	Tube, lead-free
ATA6814-PLQW	QFN48	Taped and reeled, lead-free

9. Package Information

Package: QFN 48 - 7x7
Exposed pad 4.5x4.5
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm

Not indicated tolerances ±0.05



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