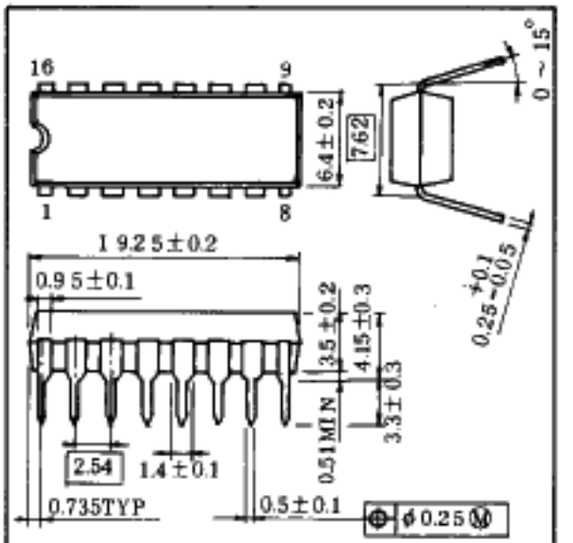
TC9203P/F

PLL MOTOR CONTROL FOR FDD

TC9203P/F are C^2MOS LSI designed for controlling the motor of especially for Disk Spindle Drive (FDD). 8-bit D/A converter system has been employed for each of the speed control system (AFC) and the phase control system (APC) and realize a wide reduction of external parts and free adjustment motor control system.

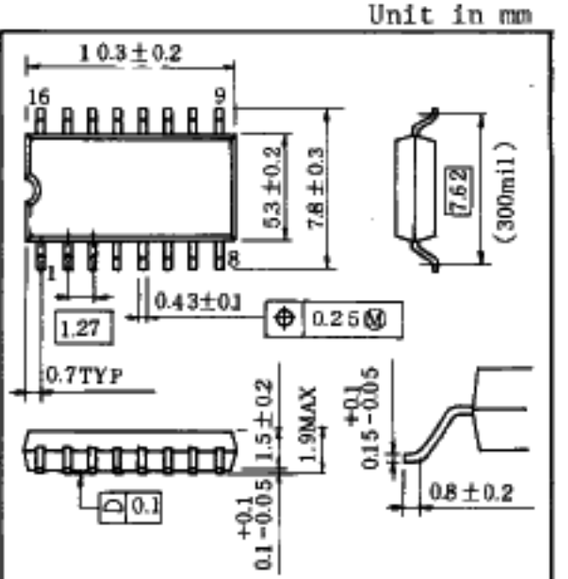
- Crystal can be used up to 8MHz, and crystal reference dividing frequency selected from three position of 1/5, 1/6 and 1/12 correspond to 8,5 and 3.5 inch FDD.
- Lock range can be selected from two position of 1/20 and 1/27.
- External oscillator makes possible fine adjustment of speed.
- Lock detection output and reverse rotation signal output are provided.
- Surface mount is available with TC9203F.



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

JEDEC	–
TOSHIBA	DIP16-P-300A

Unit in mm



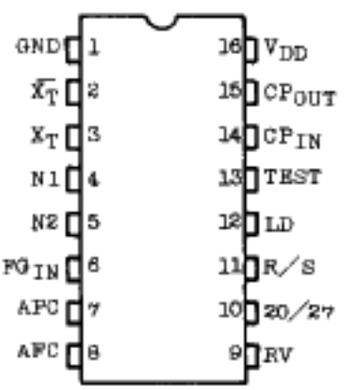
Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

JEDEC	–
TOSHIBA	SOP16-P-300

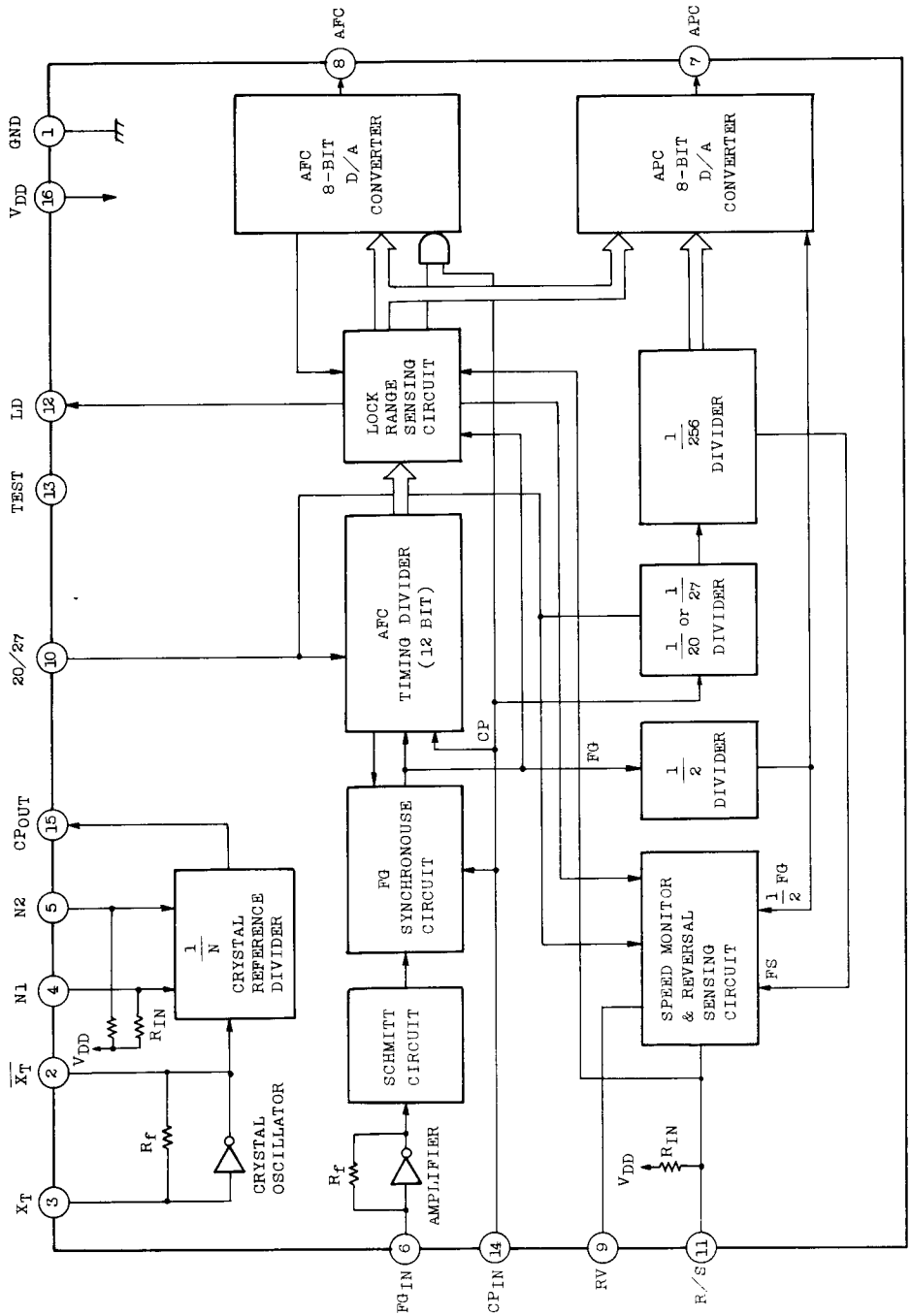
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3~7.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	Topr	-30~75	°C
Storage Temperature	Tstg	-55~125	°C

PIN CONNECTIONS



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD}=5V, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	-		*	4.5	5.0	5.5	V
Operating Supply Current		I_{DD}	1	X'tal=8MHz CP_{IN}=CP_{OUT}	*	-	5.0	12.0	mA
Operating Frequency Range	X_T	f_{XT}	2		*	1.0	~	8.0	MHz
	CP_{IN}	f_{CP}	3	Square wave	*	0.05	~	4.0	
	FG_{IN}	f_{FG}	-	V_{IN}=0.5Vp-p Sin wave	*	-	~	10	kHz
Input Operating Voltage	FG_{IN}	$V_{IN\ FG}$	4	f_{FG}=10kHz Sine wave	*	0.5	~	V_{DD}-0.5	Vp-p
AFC, APC D/A Converter	Ladder Resistor	R_L	6			30	50	75	kΩ
	Max. Deviation		-	V_{DD}=4.5~5.5V		-	±2.5	±6.5	LSB
	Resolution					-	V_{DD}/256	-	V
	Temperature Drift					-	±1	-	LSB
Pullup Resistor		R_{IN}	-	N1,N2,20/27,R/S	*	10	30	50	kΩ
Input Voltage	"H" Level	V_{IH}	-	N1,N2,20/27,R/S CP_{IN}	*	V_{DD}×0.8	~	V_{DD}	V
	"L" Level	V_{IL}				0	~	V_{DD}×0.2	
Input Leak Current		I_{IH}/I_{IL}	-	CP_{IN}	*	-	-	±1.0	μA
Output Current	"H" Level	I_{OH}	-	RV, LD CP_{OUT}	V_{OH}=4V	-0.5	-1.0	-	mA
	"L" Level	I_{OL}			V_{OL}=1V	0.5	1.0	-	
Amplifier Feedback Resistor	X_T	R_f	5			100	200	500	kΩ
	FG_{IN}					300	500	800	

* : Guaranted within the range of V_{DD}=4.5V~5.5V, Ta=-40~85°C.

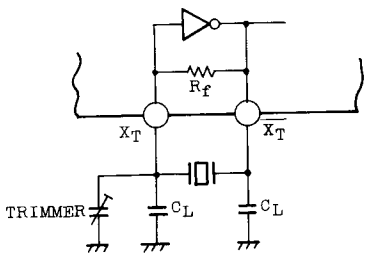
FUNCTIONAL EXPLANTION OF EACH TERMINAL

PIN No.	SYMBOL	TERMINAL NAME	FUNCTIONAL & OPERATION EXPLANATION	REMARKS
16	V_{DD}		Power supply voltage terminal and grunding terminal.	
1	GND			
2	$\overline{X_T}$	Crystal Oscillation Terminal	Crystal oscillator is connected.	with a built-in feedback resistor.
3	X_T			
4	N1	Reference Divided Frequency Switching Terminal	Switching of divided frequency from the crystal reference frequency divider into 1/5,1/6 and 1/12 is possible.	with a built-in pull-up resistor.
5	N2			
6	FG_{IN}	FG Pulse Input Terminal	Frequency generator input.	with a built-in amplifier.
7	APC	APC Output Terminal	8 bit DAC output terminal for phase-voltage conversion.	
8	AFC	AFC Output Terminal	8 bit DAC output terminal for frequency-voltage conversion.	
9	RV	Reverse Signal Output Terminal	Terminal for motor reverse signal Output.	
10	20/27	Lock Range Switching Terminal	Terminal for switching lock range. H or NC=1/20, L=1/27.	with a built-in pull-up resistor
11	R/S	RUN/STOP Input Terminal	Motor RUN/STOP signal input terminal. H or NC=STOP, L=RUN.	with a built-in pull-up resistor
12	LD	Lock Detecting Terminal	This terminal becomes H when the motor speed is within the lock range and otherwise L.	
14	CP_{IN}	Reference Frequency Input Terminal	Normally connected to CP_{OUT}. For external fine adjustment input from an external oscillator.	
15	CP_{OUT}	Reference Frequency Output Terminal	Terminal for divided output from the crystal reference frequency divider. Normally connected CP_{IN}.	
13	TEST	Test Terminal	Input terminal of internal test. Generally ground.	

OPERATION

1. Crystal oscillation terminals (X_T, $\overline{X_T}$)

. The crystal oscillator is used by connecting as shown below.



. C_L of 10~30pF is appropriate.

Crystal oscillation frequency is calculated by the following equation according to number of FG pulses of a motor to be used.

$$f_X = \frac{R}{60} \times FG' \times 128 \times (20 \text{ or } 27) \times N \quad (Hz)$$

(Note) (20 or 27) : 20 at 20/27="H" or Open.
27 at 20/27="L".

f_X: Crystal oscillation frequency, FG': number of FG pulse generated per revolution of motor, R: revolution of motor per minute,
N : Ratio of frequency division of the crystal reference frequency divider. (Refer to Item 9.)

. Maximum operating frequency is above 8MHz and crystals up to 8MHz can be used.

2. Reference frequency input/output terminals (CP_{IN}, CP_{OUT})

. Divided output $\frac{f_X}{N}$ from the crystal reference frequency divider is available at CP_{OUT}, which is normally connected CP_{IN}.

. When an external oscillator (CR oscillator, etc.) is connected to CP_{IN}, motor speed can be finally adjusted.

3. FG pulse input terminal (FG_{IN})

. This is the input terminal of FG pulse that shows the motor speed. This FG pulse becomes comparision frequency.

. This terminal has built-in Amplifier and Schmitt circuit. FG pulses are applied through capacitor coupling and small amplitude is enough for proper operation.

4. Lock range switching terminal (20/27)

. This terminal is for switching rock range of motor, with a pull-up resistor and chattering preventive circuit.

(TRUTH TABLE)

20/27	DIVIDED FREQUENCY	LOCK RANGE
L	1/27	+3.4~-3.9% of reference cycle
H or NC	1/20	+4.6~-5.3% of reference cycle

5. APC, AFC output terminal (APC, AFC)

. AFC (speed control output) is a F-V converter for FG frequency, and is consisting of a 8 bit D/A converter.

. APC (phase control output) is a phase comparator (ϕ-V converter) that compares phase difference ϕ between 1/2 FG and reference frequency FS', and is also consisting of a 8 bit D/A converter.

. Both APC and AFC perform the following 3 operations according to FG_{IN} frequency.

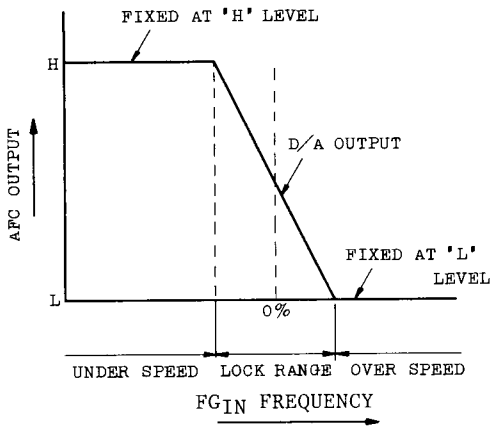
a. When FG_{IN} frequency is within the lock range:
Both APC and AFC perform the normal operation for FG_{IN}.

b. When FG_{IN} frequency is below the lock range (under speed):
APC and AFC outputs are both fixed at "H" level.

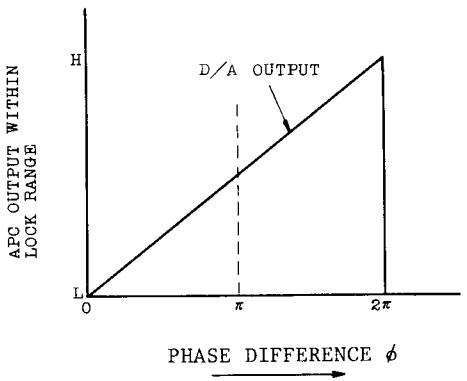
c. When FG_{IN} frequency is above the lock range (over speed):
APC and AFC outputs are both fixed at "L" level.

. When a motor is in STOP state (P/S=H or NC), both AFC and APC are fixed "L" level.

AFC Output change status for FG_{IN} frequency

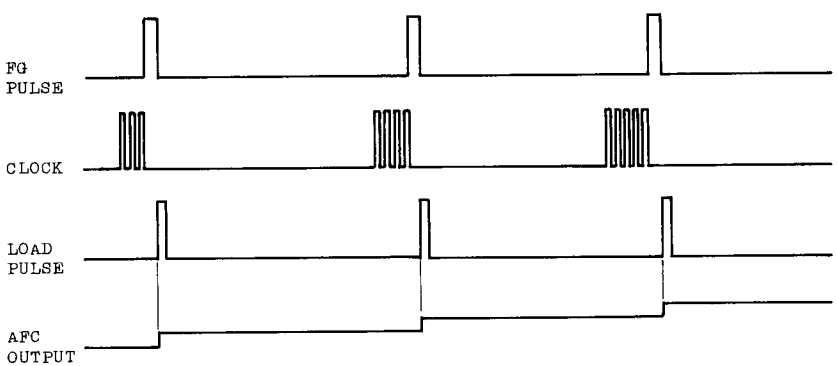


APC Output change status for phase difference ϕ.

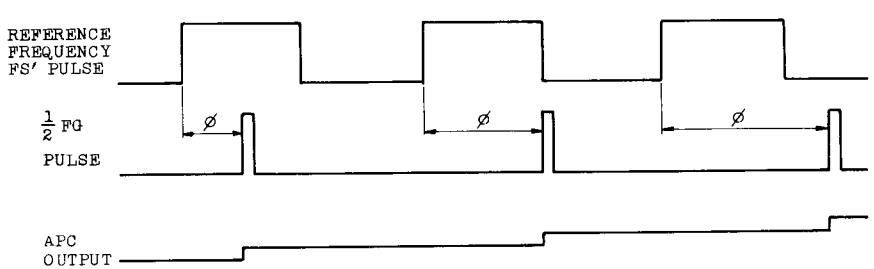


. AFC and APC timing chart within lock range.

a. AFC (SPEED CONTROL SYSTEM)



b. APC (PHASE CONTROL SYSTEM)



6. Lock detecting terminal (LD)

. This terminal is the lock detecting output and is placed at "H" level when FG_{IN} frequency is within the lock range and otherwise, placed at "L" level.

7. RUN/STOP input terminal (R/S)

. RUN/STOP signals of the motor are input to this terminal.

. This terminal has a pull-up resistor and a chattering proventive circuit.

. During RUN (R/S=L), AFC, APC and LD perform the above-mentioned operations for FG_{IN} frequency, and during STOP (R/S=H or NC), AFC, APC and LD are all fixed at "L" level.

8. Reverse signal output terminal (RV)

. At the switching of lock range from 1/20 to 1/27 or the operating from RUN to STOP, reverse signal for braking the motor is output through this terminal.

. Change of RV output status

PREVIOUS STATUS ⇨	RV OUTPUT CHANGE TO "H" LEVEL ↓	⇨ RV OUTPUT CHANGE TO "L" LEVEL ↓
During normal rotation (during lock) at 1/20.	When the lock range is switched from 1/20 to 1/27.	When the motor speed is locked at 1/27, or when FG_{IN} 1/8FS, or when the lock range is switched from 1/27 to 1/20.
During normal rotation (during lock) at 1/20 or 1/27.	When the operation is switched from RUN to STOP.	When FG_{IN} 1/8FS or when the operation is switched from STOP to RUN.

. In other cases than above, RV output is not changed and fixed at "L" level.

. Further, if FG frequency rises up to 1.5 times of normal rotation at 1/20 (2 times of normal rotation at 1/27), RV output is reset

9. Reference divided frequency switching terminal (N1, N2)

. Divided frequency 1/N of the crystal reference frequency divider can be switched to 1/5, 1/6 or 1/12 by number of FG pulses or a crystal used.

. This terminal has a built-in pull-up resistor.

(TRUTH TABLE)

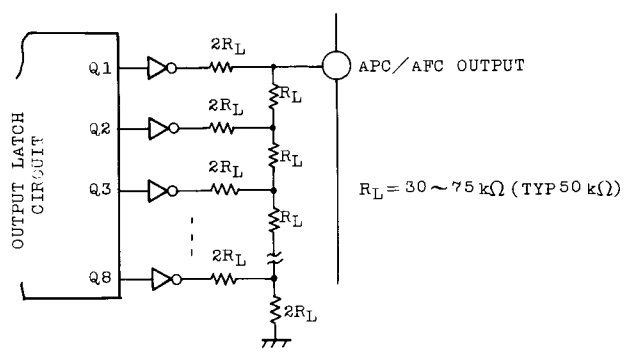
N1	N2	1/N
H	H	1/5
L	H	1/6
H	L	1/12

1/N: CRISTAL REFERENCE DIVIDED FREQUENCY

(Note) Don't use mode, N1=N2="L", because this mode is test mode.

CAUTION IN APPLICATION

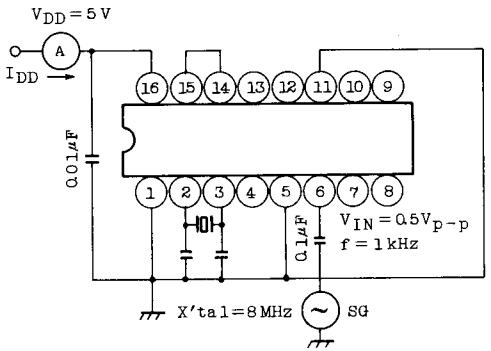
. APC and AFC terminals are for the 8-bit D/A converter outputs, which are directly output from the R-2R ladder type resistor network as shown in the following diagram. Impedance of these outputs becomes equal to the ladder resistor value R_L. Terefore, input impedance at the receiving side of these terminals shall be designed accordingly.



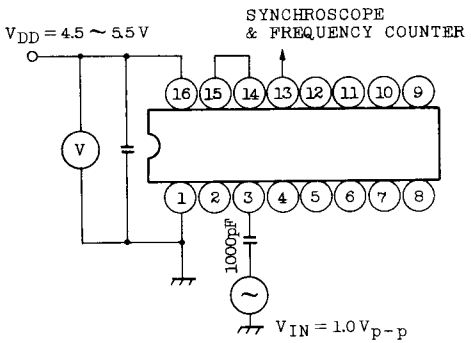
. A filter for an externally mounted differential amplifier on an application circuit shall be selected to meet the response characteristic of a motor to be used.

CHARACTERISTIC TEST CIRCUIT

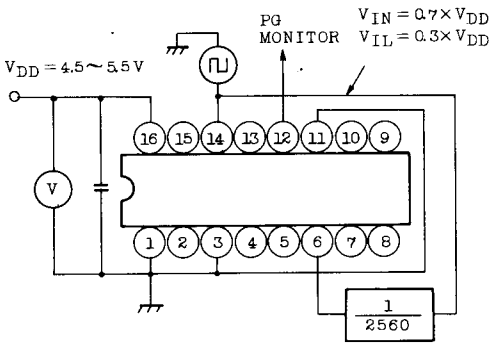
(1) Operating supply current I_{DD}



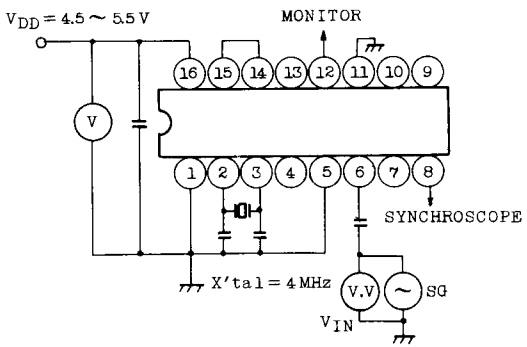
(2) X_T Operating frequency range $f_{MAX}(f_{XT})$



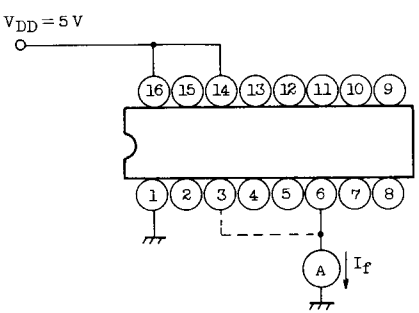
(3) CP_{IN} Operating frequency range $f_{MAX}(f_{CP})$



(4) FG_{IN} Input sensitivity V_{INFG}

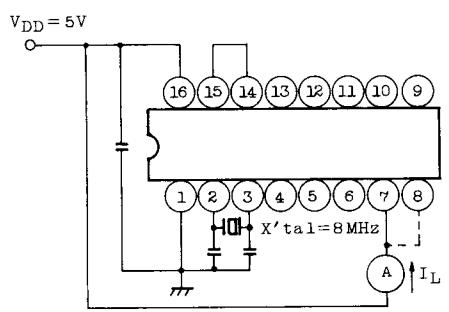


(5) Amplifier feedback resistor



$$R_f = \frac{5}{I_f} (\Omega)$$

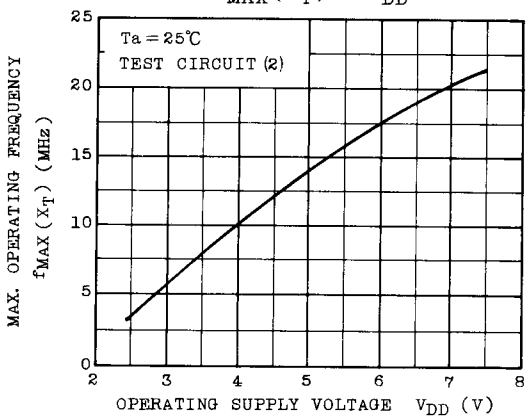
(6) D/A Converter ladder resistor $\overline{R_L}$



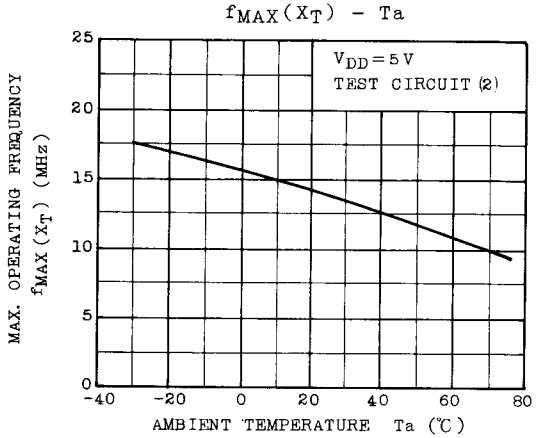
$$\overline{R_L} = \frac{5}{I_L} (\Omega)$$

CHARACTERISTIC DATA

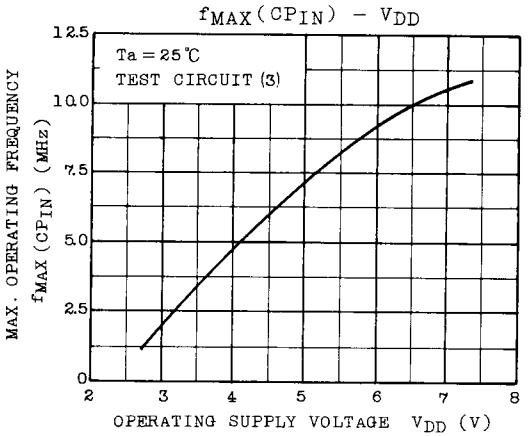
$f_{MAX}(X_T)$ – V_{DD}



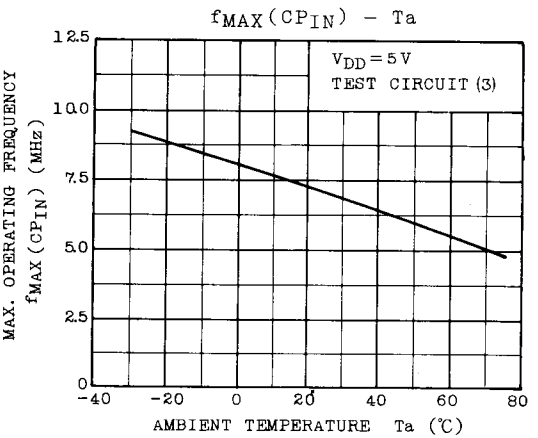
$f_{MAX}(X_T)$ – Ta



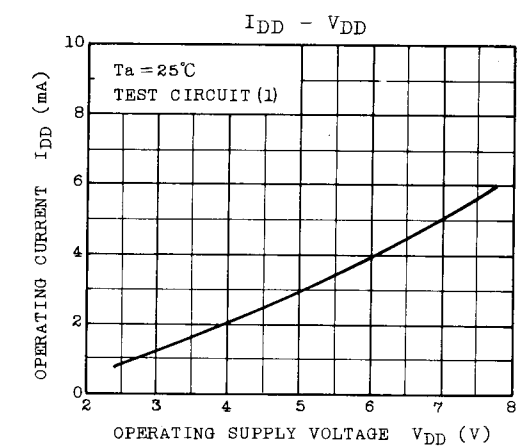
$f_{MAX}(CP_{IN})$ – V_{DD}



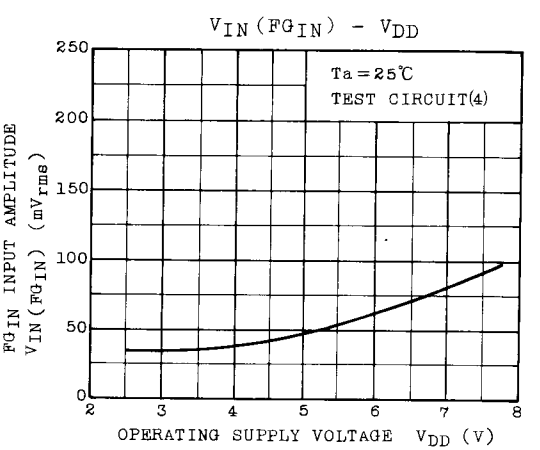
$f_{MAX}(CP_{IN})$ – Ta



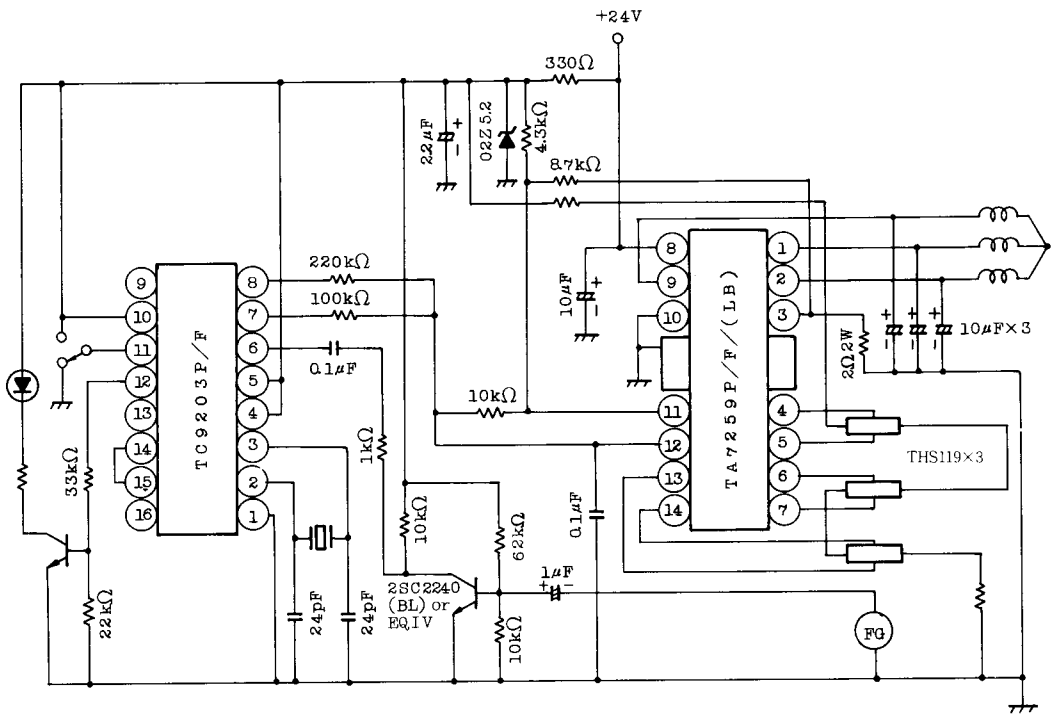
I_{DD} – V_{DD}



$V_{IN}(FG_{IN})$ – V_{DD}



EXAMPLE APPLICATION CIRCUIT



Example of crystal oscillation frequency calculation.

When FG' (number of FG pulse) = 180 pulses and R (revolution of motor) = 200r.p.m., if the dividing frequency of reference divider and lock range is set at N=5 dividing frequency and 20/27=20, the crystal oscillation frequency f_X is as follows:

$$f_X = \frac{R}{60} \times FG' \times 128 \times 20 \times N = \frac{200}{60} \times 180 \times 128 \times 20 \times 5 = 7.680\text{MHz}$$