

SANYO

No. 3032

LA2231, 2231MMonolithic Linear IC
RDS Signal Demodulator**Overview**

The LA2231 incorporates functions necessary for demodulating RDS* and ARI signals.

*The RDS (Radio Data System) transmits various multiplexed data for FM broadcasting. The RDS is a system standardized by EBU (European Broadcasting Union) and common to all European nations. Multiplex data includes a list of frequencies of all the radio stations which put the same program on the air. This enables listeners traveling a long distance by car to always tune in to the best radio station by automatic follow-up reception. In addition to this, the RDS transmits data consisting of 8 alphanumeric characters to represent the name of each radio station and coded data representing the types of programs (news, sports, classical music, etc.). This makes it possible to realize new functions in FM radio reception.

Features

Incorporating ARI-SK and DK decoders, the demodulator can be applied to the ARI system with the RDS.

Functions

- DSB demodulation
- Subcarrier regeneration
- Bit rate clock regeneration
- DPSK decoding
- ARI-SK identification
- ARI-DK identification
- RDS indicator drive
- ARI indicators drive
- Data error indication output

Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V _{CC} max	Pins 13, 14, 15, 23	12	V
Inflow Current	I _{LED}	Pins 13, 14, 15	20	mA
Allowable Power Dissipation	P _d max*		450	mW
Operating Temperature	T _{op}		-30 to +80	°C
Storage Temperature	T _{stg}		-40 to +125	°C

*LA2231M: Ta≤47°C

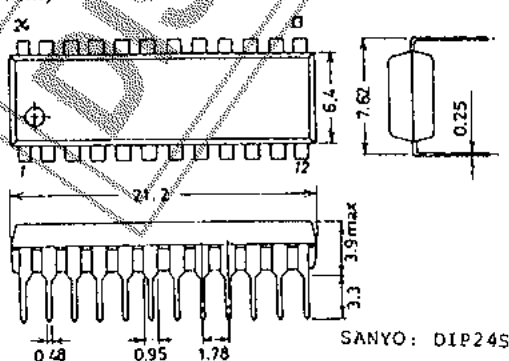
Operating Conditions at Ta=25°C

				unit
Recommended Supply Voltage	V _{CC}	Pin 23	5.0	V
Operating Voltage Range	V _{CC} op	Pin 23	4.5 to 5.5	V

Case Outline 3057-D24SIC

(unit: mm)

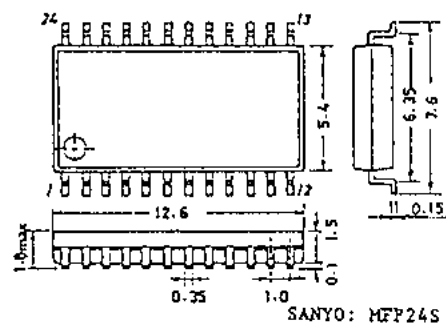
[LA2231]



Case Outline 3112-M24SIC

(unit: mm)

[LA2231M]



Specifications and information herein are subject to change without notice.

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LA2231, 2231M

Operating Characteristics at $T_a=25^\circ\text{C}$, $V_{cc}=5.0\text{V}$

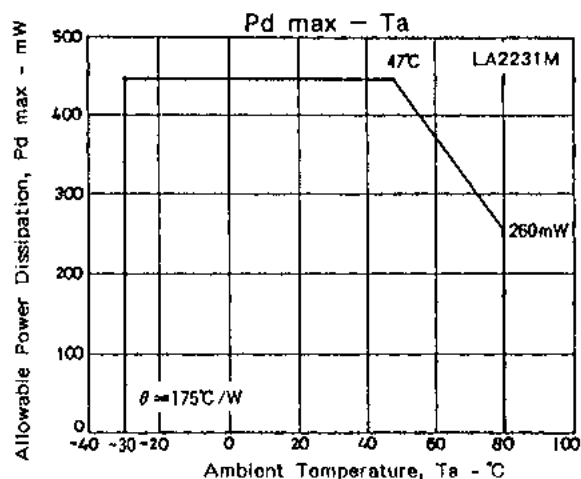
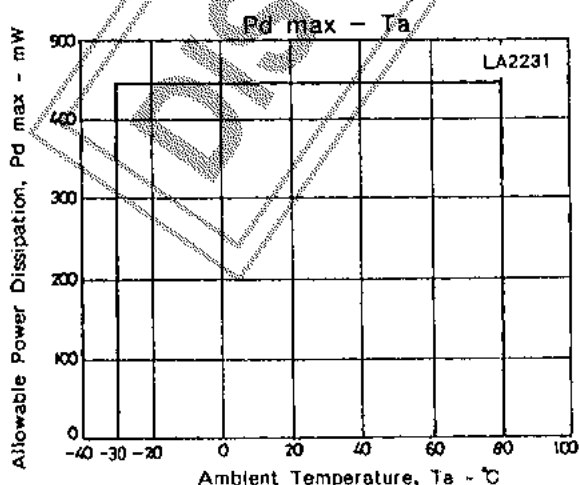
	min	typ	max	unit
Quiescent Current	14	20	26	mA
PLL Capture Range (10mVrms CW input)		-0.9		%
		+1.5		%
RDS Detection Sensitivity (pin 5 input which sets pin 15 to "L")		1.5	3.5	mVrms
ARI Detection Sensitivity (pin 5 input which sets pin 14 to "L")		3.5	7.5	mVrms
DK Detection Sensitivity (pin 5 input which sets pin 13 to "L")		3.7	8.0	mVrms
Input Dynamic Range (RDS)	55	85		mVrms
(Maximum pin 5 input which sets pin 15 to "L" and pin 14 to "H")				
Input Dynamic Range (ARI)	100	190		mVrms
(Maximum pin 5 input which sets pin 14 to "L" and pin 13 to "H")				
Data Demodulation Sensitivity		5		dB
(C/N input which sets the error rate= 10^{-3})				
Bit Rate Clock Jitter	8	9	10	usec
ARI Lock-up Time (Time that pin 14 turns to "L" after ARI=27mVrms inputs)		60	*1	msec
RDS Lock-up Time (Time that pin 15 turns to "L" after RDS=10mVrms inputs)		40	*2	msec
ARI + RDS Lock-up Time		130	*3	msec
(Time that pin 15 turns to "L" after ARI+RDS=28mVrms inputs)				
DK Lock-up Time		0.6	*4	sec
(Time that pin 13 turns to "L" after ARI+BK+DK=27mVrms inputs)				
DK Off Time		0.9	2.0	sec
(Time that pin 13 turns to "H" after ARI=27mVrms inputs and DK only off)				
Data Output ("H" level)	4.7	4.9	5.0	V
("L" level)	0	0.1	0.3	V
Bit Rate Clock Output ("H" level)	4.7	4.9	5.0	V
("L" level)	0	0.1	0.3	V
Error Flag Output ("H" level)	4.7	4.9	5.0	V
("L" level)	0	0.1	0.3	V
Free-run Frequency	453	456	459	kHz

Values *1 to *4 may become high though the probability is extremely low, so the maximum value is not specified (the maximum value exceeds 2 sec once per 1000 measurements).

For reference, the table below lists the upper limit (approximately 3σ) values of periods in which lock-up occurs with a probability of about 99%.

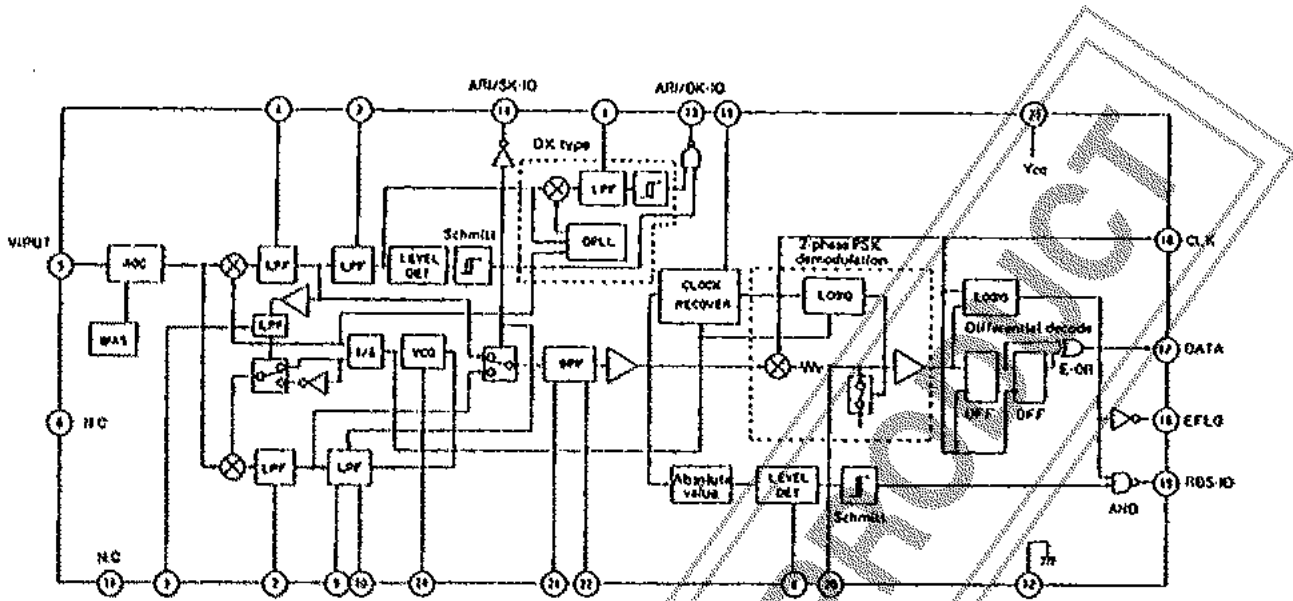
Reference table (periods in which lock-up occurs with a probability of about 99%)

Item	*1	*2	*3	*4
Upper limit(3σ)	170	150	200	1.7
unit	msec	msec	msec	sec

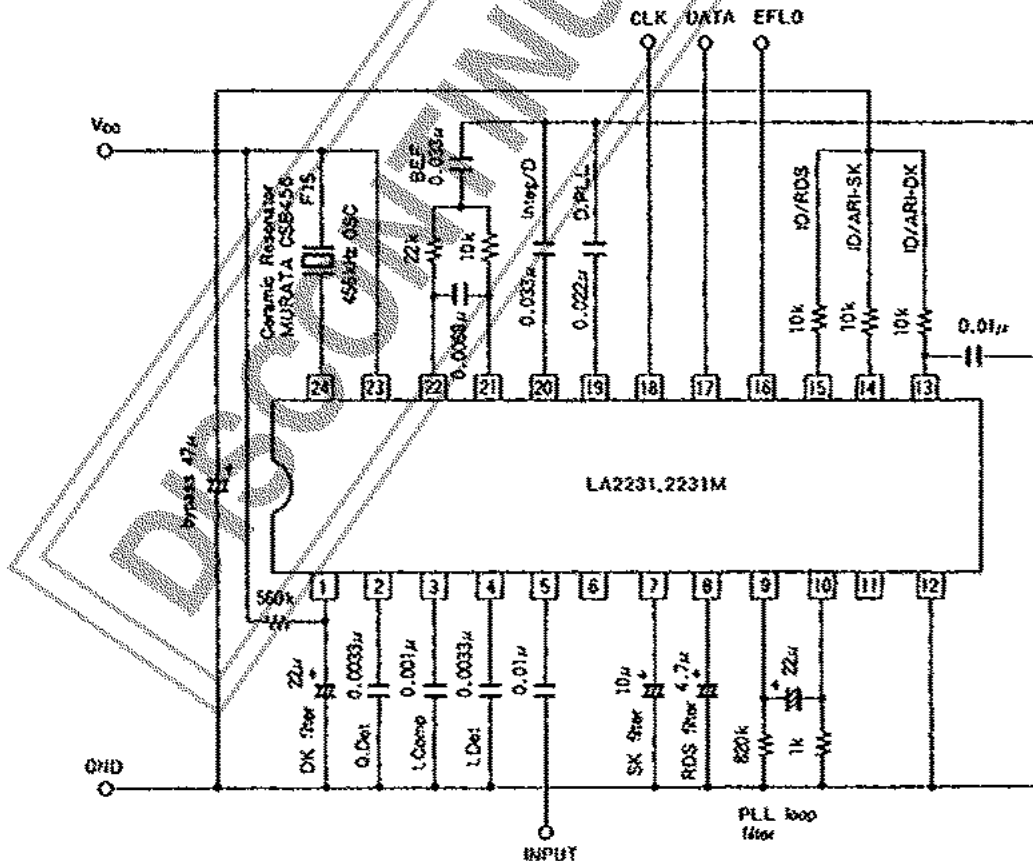


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LA2231/LA2231M Block Diagram

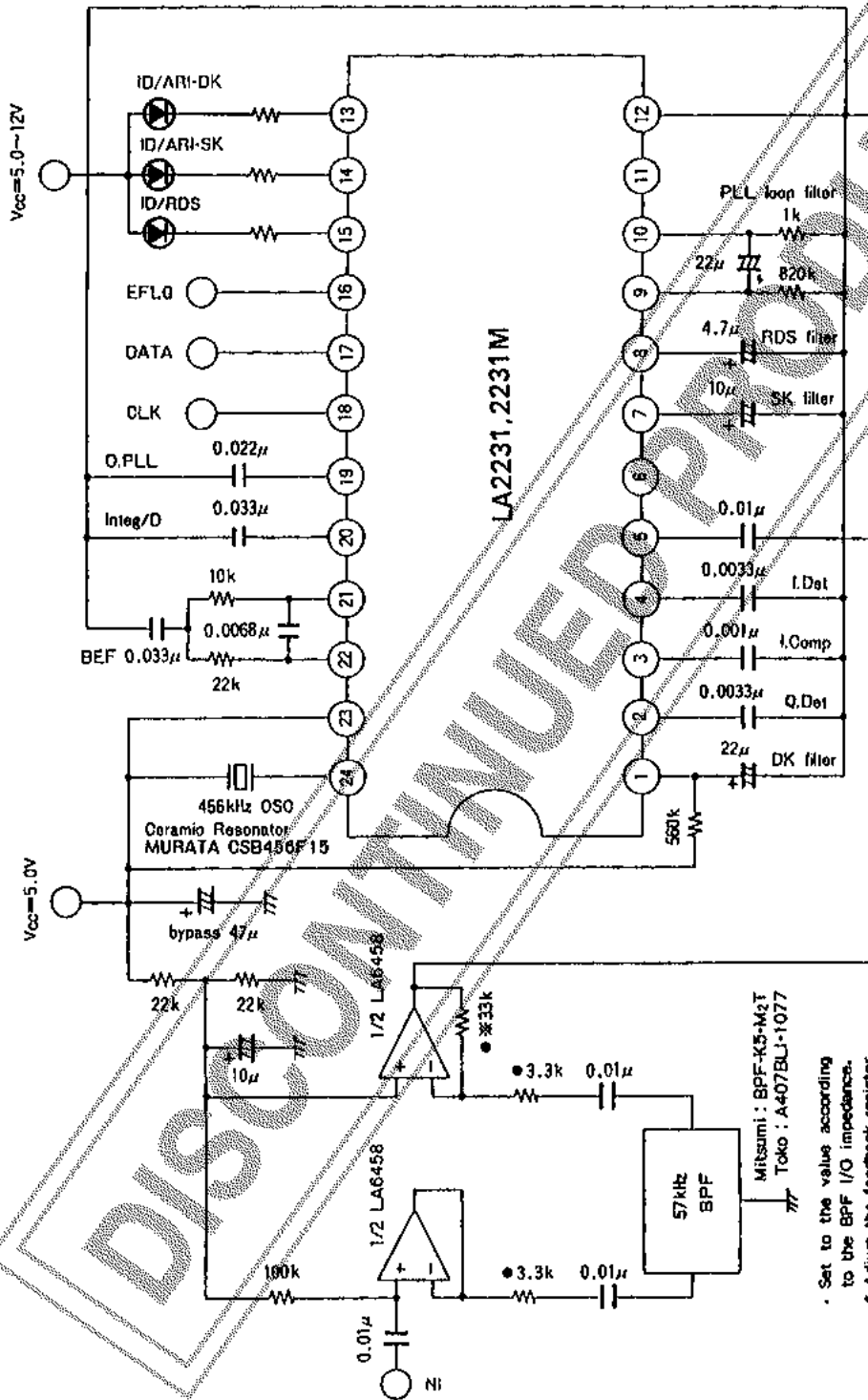


LA2231/LA2231M Test Circuit



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LA2231/2231M Sample Application Circuit

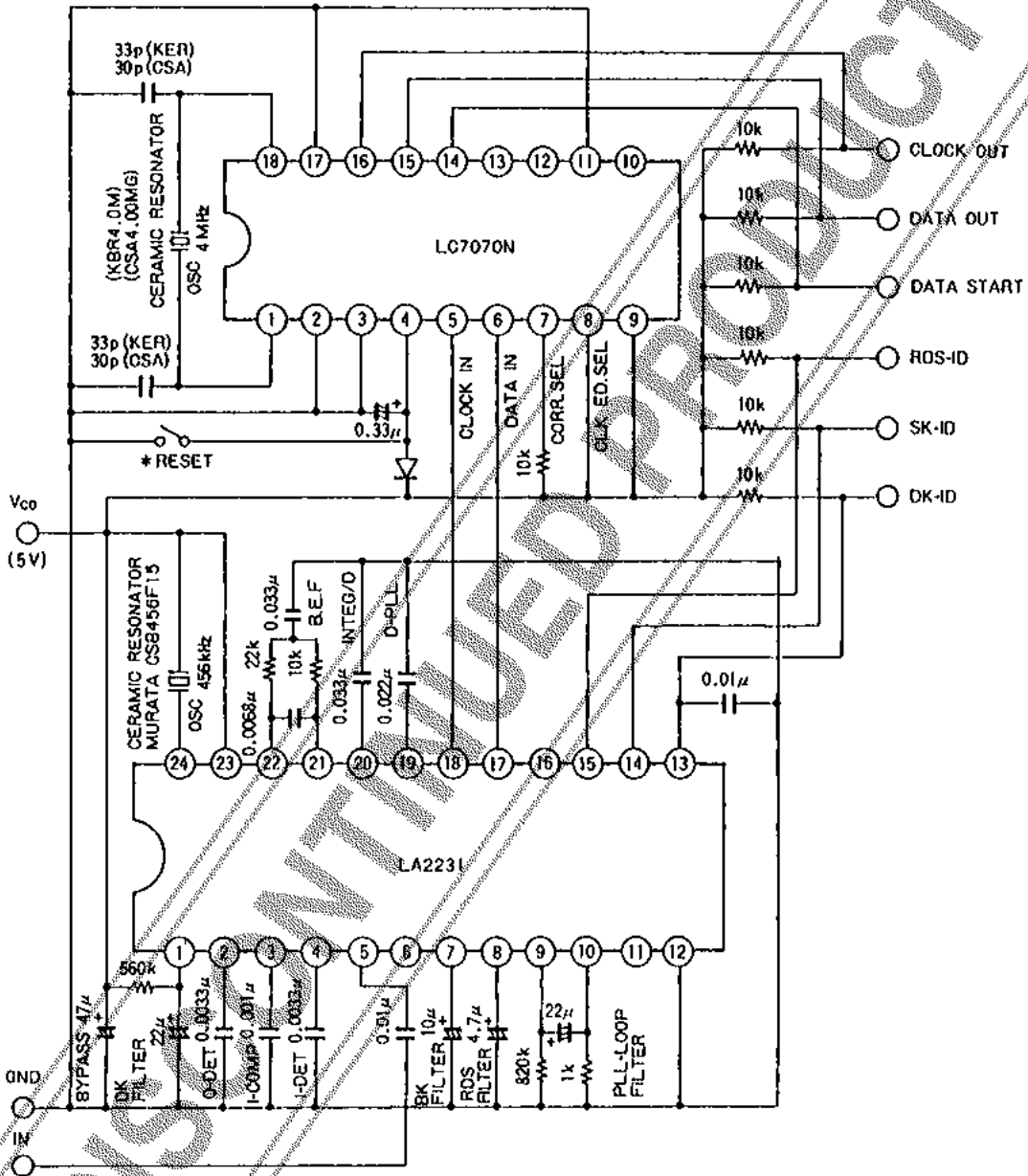


- Capacitors at pins ⑦, ⑧ and ⑨ determine the time for the ID lamp (pins 13 to 15) to be lit when Vcc turns on. (The smaller the capacitance is, the shorter the time becomes.)
- Capacitance of the capacitors at pins ⑦, ⑧ and ⑨ should have more than half the values shown in the diagram (this prevents erroneous lighting of the ID lamp).

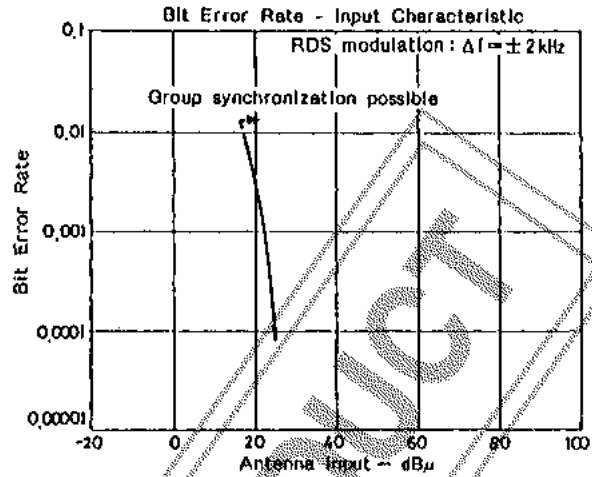
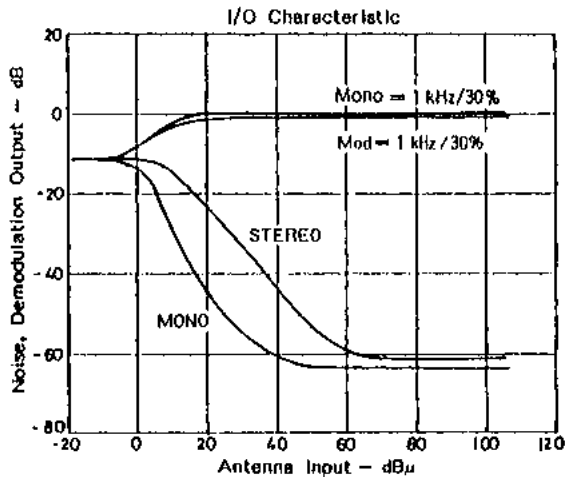
- Set to the value according to the BPF I/O impedance.
- Adjust the feedback resistor 33kΩ according to the FM demodulation output. Set the resistor so that the RDS signal input is 10mVrms (typ) at pin ⑤ of the LA2231 (RDS modulation Δf = ±2.0kHz).

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LA2231 + LA7070N Sample Application Circuit



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Description of the LA2231 and 2231M

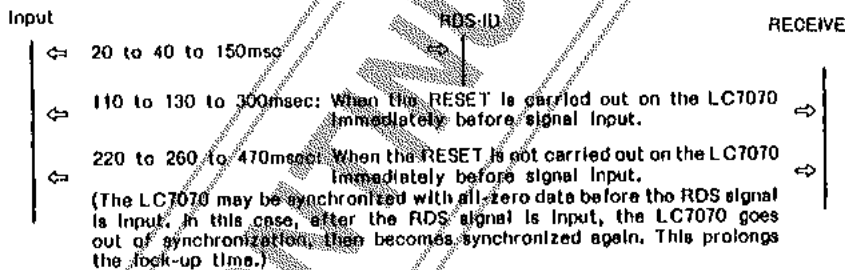
1. LA2231+LC7070N lock-up time

The figure below shows the operation timing of the RDS-ID and SK-ID output of the LA2231 and data synchronization output (RECEIVE) of the LC7070N.

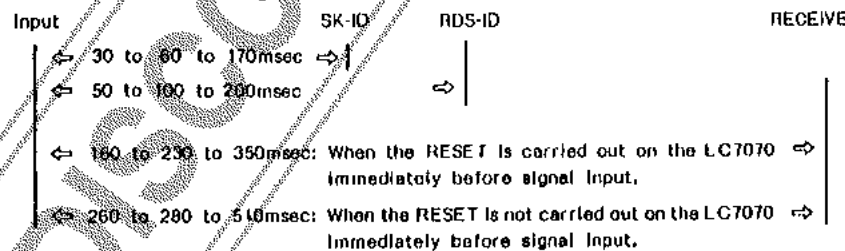
Variations in the detection time are not always in this range; these values are given for reference.



RDS only (LA2231, pin 5) = 10mVrms



RDS+SK+BK+DK (LA2231, pin 5) = 28mVrms



2. CLK/DATA output timing of the LA2231



Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.