# STPC PICTOR

## X86 CORE PC COMPATIBLE SOC with GRAPHICS and VIDEO

**PRODUCT PREVIEW**

- ■ PENTIUM® II CLASS CORE RUNNING IN X1 MODE UP TO 133MHZ OR X2 MODE UP TO 200MHZ
- ■ 64 BIT SDRAM CONTROLLER RUNNING AT UP TO 100 MHZ
- ■ VGA & SVGA CRT CONTROLLER
- ■ 135MHz RAMDAC
- ■ 2D GRAPHICS ENGINE
- ■ VIDEO INPUT PORT
- ■ VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- ■ TV OUTPUT
  - 3-LINE FLICKER FILTER
  - CCIR 601/656 SCAN CONVERTER
  - NTSC / PAL COMPOSITE, RGB, S-VIDEO
- ■ PCI 2.2 COMPLIANT MASTER/SLAVE CONTROLLER
- ■ INTEGRATED PERIPHERAL CONTROLLER WITH SUPPPORT FOR EXTERNAL RTC
- ■ ULTRA IDE-33 IDE CONTROLLER
- ■ POWER MANAGEMENT UNIT
- ■ 16-BIT LOCAL BUS WITH 2 DMA CHANNELS
- ■ 1 I2C BUS CONTROLLER
- ■ IEEE 1149.1 JTAG INTERFACE
- ■ PROGRAMMABLE CLOCKS
- ■ 0.18 MICRON TECHNOLOGY.
- ■ 1.8V CORE & 3.3V I/O'S
- ■ MAXIMUM POWER DISSIPATION; 3.1W @ 250MHZ

### DESCRIPTION

The STPC PICTOR integrates a fully static Pentium® MMX® Class processor, fully compatible with Industry Standard, and combines it with powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).



PBGA388
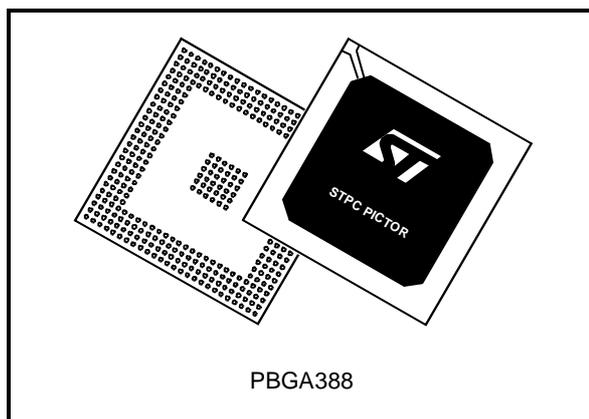
**Logic Diagram**
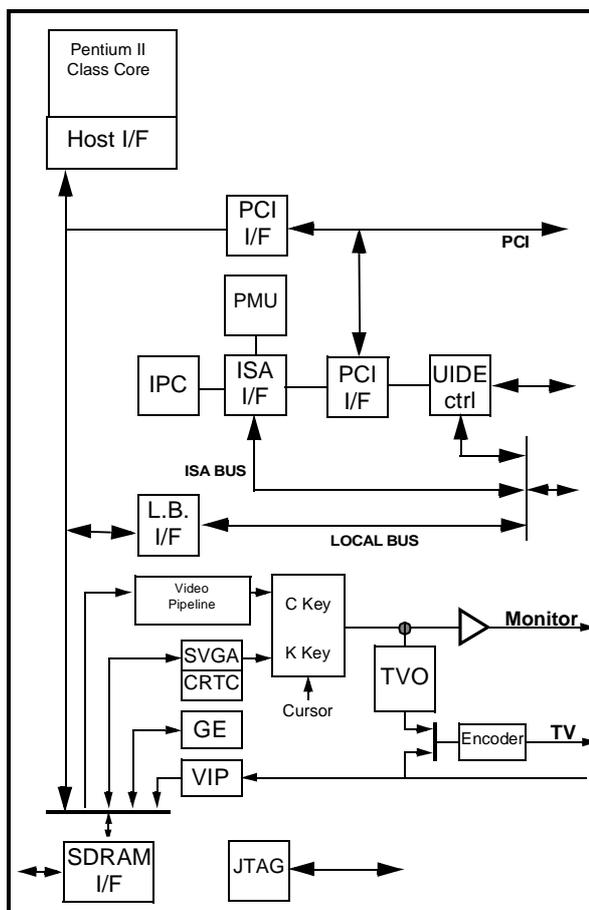
■ **X86 Processor**
■ x86 Pentium® II class compatible processor
   -3 Issue integer 6 stage pipeline/clock
   -3 issue MMX®/clock
   -Pipelined FPU
■ Bus clock with skew correction
■ Internal core clocks generated as multiples of bus clock with multiplication factors of X1, X2, X2.5, X3, X3.5

■ **SDRAM Interface**
■ 64 bit data bus
■ 100 MHz maximum SDRAM clock
■ 8 MByte to 128 MByte memory size
■ Supports 16 Mbit, 64 Mbit and 128Mbit memories
■ Support of -8, -10, -12, -13, -15 memory parts
■ Supports Buffered, non-buffered & registered DIMMs
■ Programmable latency
■ 32bit accesses not supported
■ Autoprecharge not supported
■ Power-down not supported

■ **2D Graphics Controller**
■ 64-bit windows accelerator.
■ Backward compatibility to SVGA standards.
■ Hardware acceleration for text, bitblts, transparent blts and fills.
■ Up to 64 x 64 bit graphics hardware cursor.
■ Up to 4MB long linear frame buffer.
■ 8-, 16-, 24- and 32-bit pixels.
■ Drivers availables for various OSes.

■ **CRT Controller**
■ Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
■ 8-, 16-, 24-, 32-bit pixels.
■ Up to 64 x 64 bit graphics hardware cursor. MS Windows compatible.
■ Interlaced or non-interlaced output.
■ Requires no external frequency synthetizer.
■ Requires only external reference source.

■ **Video Input port**
■ Accepts video inputs in CCIR 601 mode.
■ Support of CCIR656 during active video section (without VBI)
■ Optional 2:1 decimator
■ Stores captured video in off setting area of the onboard frame buffer.
■ Video pass through to the TV output for full screen video images.
■ HSYNC and B/T generation or lock onto external video timing source.

■ **Video Pipeline**
■ Two-tap interpolative horizontal filter.
■ Two-tap interpolative vertical filter.
■ Color space conversion (RGB to YUV and YUV to RGB).
■ Color hit information to control external OSD devices
■ (Arbitrary) Programmable window size.
■ Chroma and color keying for integrated video overlay.

■ **Video Output**
■ NTSC-M; PAL-B, D, G, H, I, M, N encoding.
■ 4 analog outputs in two configurations:
   - R,G,B + CVBS
   - C,YS,CVBS1 + CVBS2
■ Flicker-free interlaced output.
■ Programmable two tap filter with gamma correction or three tap flicker filter.
■ Interlaced or non-interlaced operation mode.
■ Progressive to interlaced scan converter.
■ Cross color reduction by specific trap filtering on luma within CVBS flow.
■ Power down mode available on each DAC.

- **PCI Controller**
- Fully compliant with PCI 2.2 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 cpu bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 25-bit address bus.
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 2 Programmable Flash Chip Select.
- 4 Programmable I/O Chip Select.
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 16MB flash devices with boot block shadowed to 0x000F0000.

- **U-IDE Interface**
- Supports PIO
- Supports U-IDE hard drives larger than 528MBytes
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
- Support for PIO mode 3 & 4 and DMA Mode 1 & 2.
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Support for CD-ROM and tape peripherals
- Supports CRC-16 error checking protocol (no correction supported)
- Backward compatibility with IDE (ATA-1).
- Drivers for Windows and other Operating Systems

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and SMI.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.
-