

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

DESCRIPTION

The μ PD16750 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ -corrected by an internal D/A converter and 8-by-2 external power modules. Because the output dynamic range is as large as $V_{DD2} - 0.2$ V to $V_{SS2} + 0.2$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 40 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels. This driver is applicable to SXGA TFT-LCD panels by input display signal 2 systems (Clock divide).

FEATURES

- CMOS level input
- 384 outputs
- Input of 8 bits (gradation data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- Output dynamic range: $V_{DD2} - 0.2$ V to $V_{SS2} + 0.2$ V
- High-speed data transfer: $f_{CLK} = 40$ MHz (internal data transfer speed when operating at 3.0 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (POL21/22)
- Logic power supply voltage (V_{DD1}) : 3.3 V \pm 0.3 V
- Driver power supply voltage (V_{DD2}) : 9.0 V \pm 0.5 V
- Low power control function (LPC)

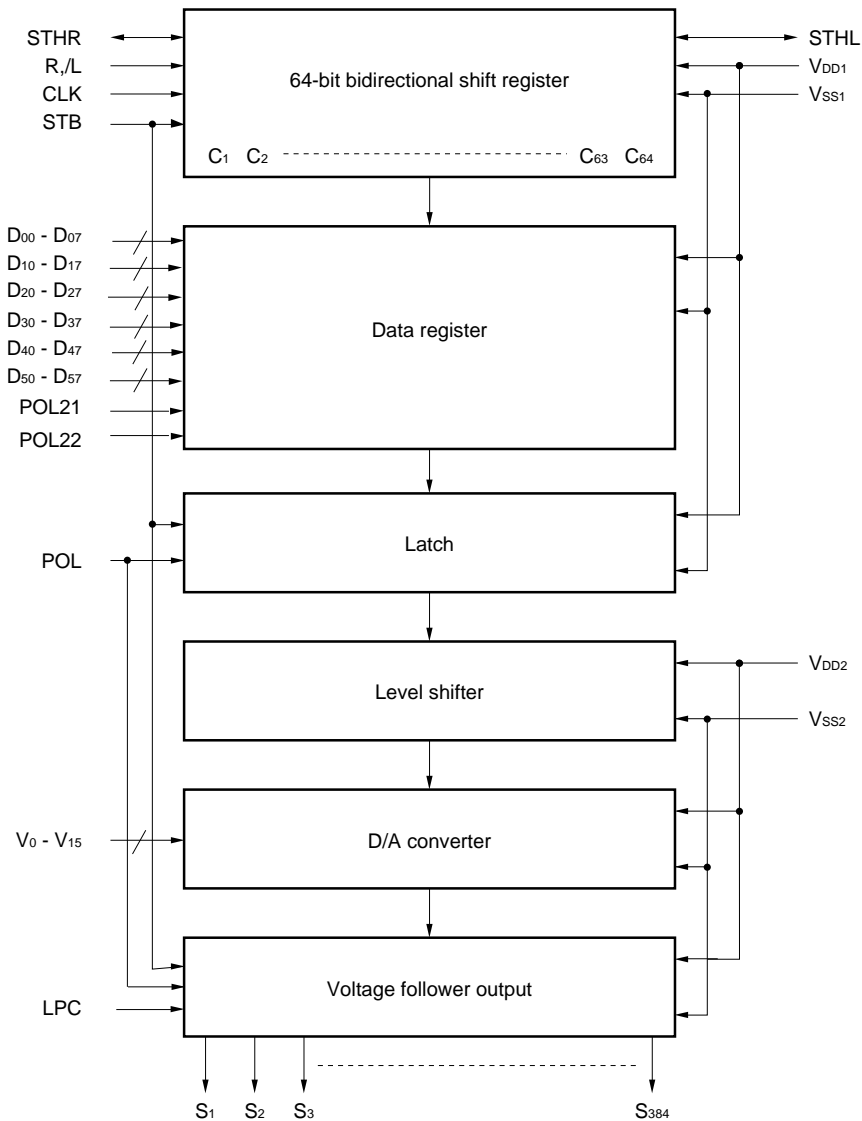
ORDERING INFORMATION

Part Number	Package
μ PD16750N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

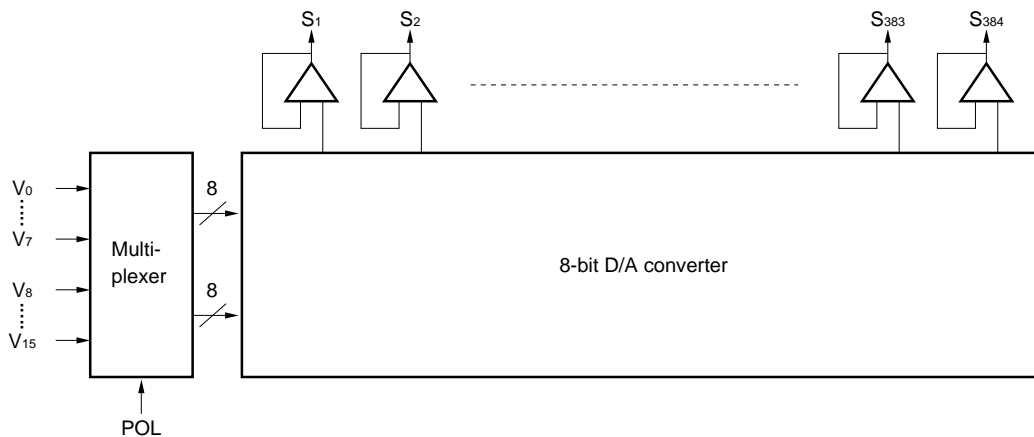
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM

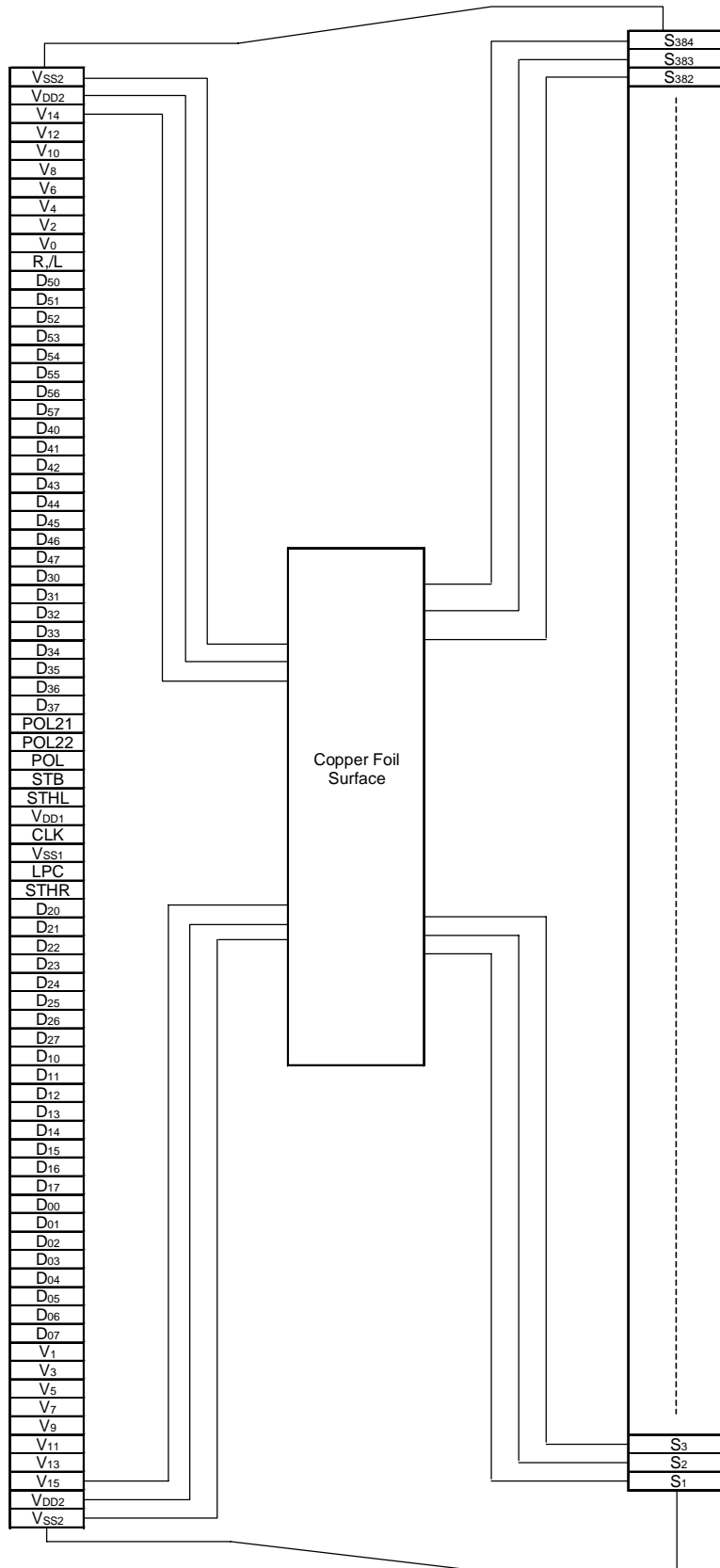


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16750N-xxx)



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Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S ₁ to S ₃₈₄	Driver output	The D/A converted 256-gray-scale analog voltage is output.
D ₀₀ to D ₀₇	Display data input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D _{x0} : LSB, D _{x7} : MSB
D ₁₀ to D ₁₇		
D ₂₀ to D ₂₇		
D ₃₀ to D ₃₇		
D ₄₀ to D ₄₇		
D ₅₀ to D ₅₇		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, S ₁ → S ₃₈₄ , STHL output R,/L = L : STHL input, S ₃₈₄ → S ₁ , STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L : The S _{2n-1} output uses V ₀ to V ₇ as the reference supply. The S _{2n} output uses V ₈ to V ₁₅ as the reference supply. POL = H : The S _{2n-1} output uses V ₈ to V ₁₅ as the reference supply. The S _{2n} output uses V ₀ to V ₇ as the reference supply. S _{2n-1} indicates the odd output: and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time(t _{POL-STB}) with respect to STB's rising edge.
POL21 POL22	Data inversion	Data inversion can invert when display data is loaded. POL21/22 = H : Data inversion loads display data after inverting it. POL21/22 = L : Data inversion does not invert input data. POL21: D ₀₀ to D ₀₇ , D ₁₀ to D ₁₇ , D ₂₀ to D ₂₇ POL22: D ₃₀ to D ₃₇ , D ₄₀ to D ₄₇ , D ₅₀ to D ₅₇
LPC	Low power control input	The output buffer constant current source is blocked, reducing current consumption. In lower power mode (LPC = L: DC-level input possible), the ordinary static current consumption can be reduced by approx. 33 %.
V ₀ to V ₁₅	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. V _{DD2} - 0.2 V > V ₀ > V ₁ > V ₂ > V ₃ > V ₄ > V ₅ > V ₆ > V ₇ > 0.5 V _{DD2} 0.5 V _{DD2} - 0.3 V > V ₈ > V ₉ > V ₁₀ > V ₁₁ > V ₁₂ > V ₁₃ > V ₁₄ > V ₁₅ > V _{SS2} + 0.2 V
V _{DD1}	Logic power supply	3.3 V ± 0.3 V
V _{DD2}	Driver power supply	9.0 V ± 0.5 V
V _{SS1}	Logic ground	Grounding
V _{SS2}	Driver ground	Grounding

- Cautions**
1. The power start sequence must be V_{DD1} , logic input, and V_{DD2} & V_0 to V_{15} in that order. Reverse this sequence to shut down (Simultaneous power application to V_{DD2} and V_0 to V_{15} is possible.).
 2. To stabilize the supply voltage, please be sure to insert a 0.1- μ F bypass capacitor between V_{DD1} - V_{SS1} and V_{DD2} - V_{SS2} . Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μ F is also advised between the γ -corrected power supply terminals ($V_0, V_1, V_2, \dots, V_{15}$) and V_{SS2} .

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2} , common electrode potential V_{COM} , and γ -corrected voltages V_0 to V_{15} and the input data. Be sure to maintain the voltage relationships of

$$V_{DD2} - 0.2\text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2},$$

$$0.5 V_{DD2} - 0.3\text{ V} > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.2\text{ V}$$

Figures 5-2 and 5-3 show the relationship between the input data and the output voltage. This driver IC is designed for only single-sided mounting. Therefore, please do not use it for γ -corrected power supply level inversion in double-sided mounting.

Figure 5-1. Relationship between Input Data and γ -corrected Power Supplies

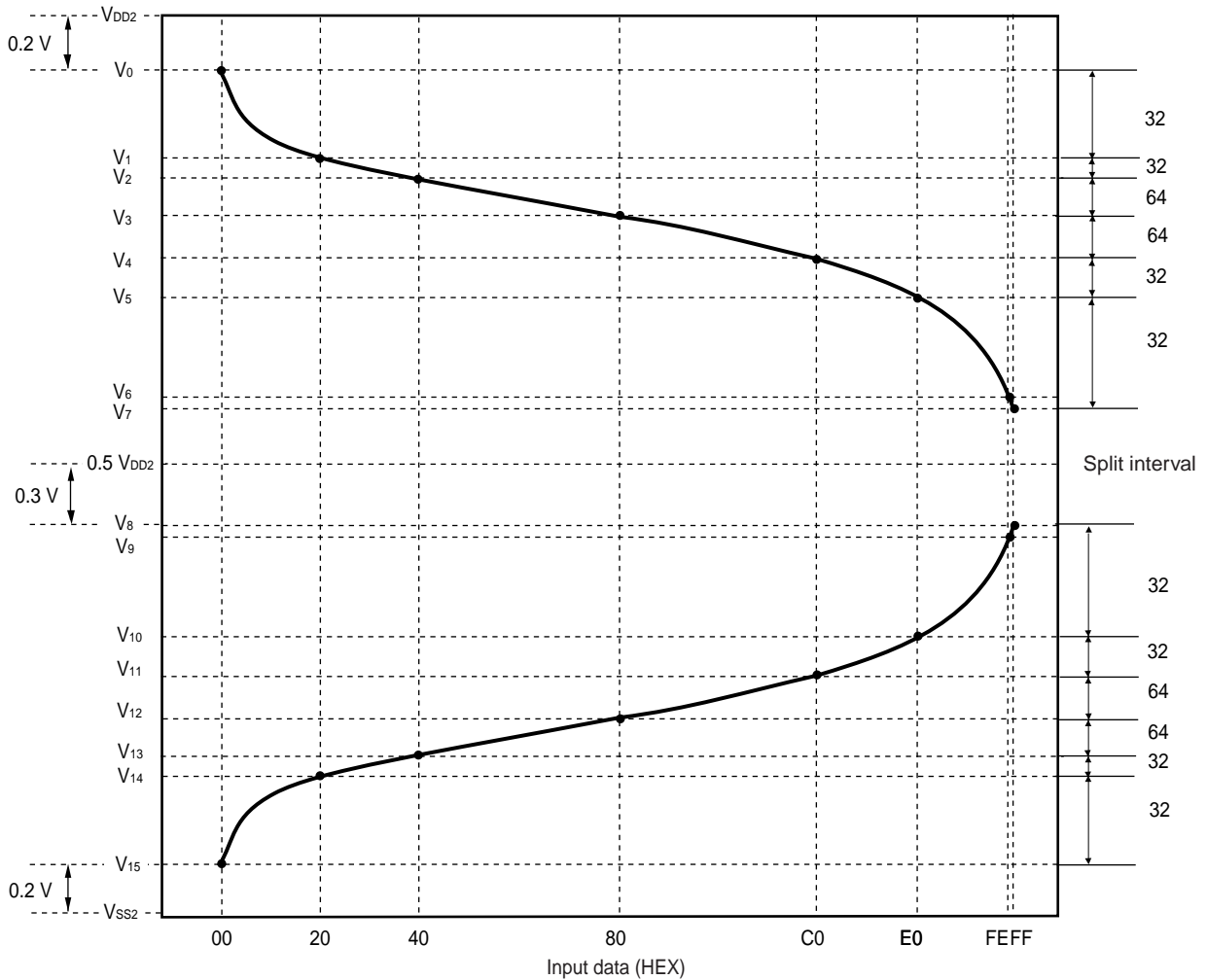
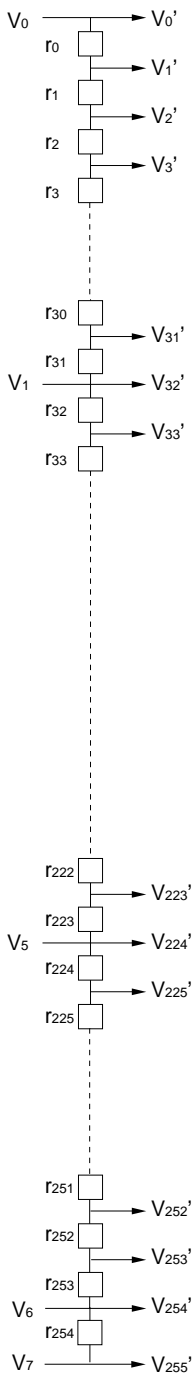


Figure 5-2. Relationship between Input Data and Output Voltage (1/4)

$V_{DD2} - 0.2\text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2}$, POL21/22 = L



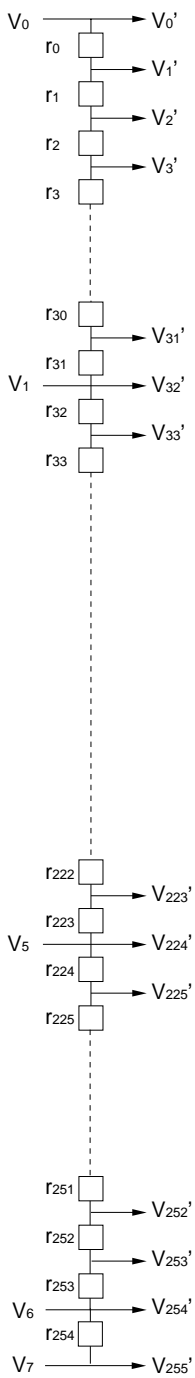
Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage	
00H	0	0	0	0	0	0	0	0	V _{0'}	V ₀
01H	0	0	0	0	0	0	0	1	V _{1'}	V ₁ +(V ₀ -V ₁) X
02H	0	0	0	0	0	0	1	0	V _{2'}	V ₁ +(V ₀ -V ₁) X
03H	0	0	0	0	0	0	1	1	V _{3'}	V ₁ +(V ₀ -V ₁) X
04H	0	0	0	0	0	1	0	0	V _{4'}	V ₁ +(V ₀ -V ₁) X
05H	0	0	0	0	0	1	0	1	V _{5'}	V ₁ +(V ₀ -V ₁) X
06H	0	0	0	0	0	1	1	0	V _{6'}	V ₁ +(V ₀ -V ₁) X
07H	0	0	0	0	0	1	1	1	V _{7'}	V ₁ +(V ₀ -V ₁) X
08H	0	0	0	0	1	0	0	0	V _{8'}	V ₁ +(V ₀ -V ₁) X
09H	0	0	0	0	1	0	0	1	V _{9'}	V ₁ +(V ₀ -V ₁) X
0AH	0	0	0	0	1	0	1	0	V _{10'}	V ₁ +(V ₀ -V ₁) X
0BH	0	0	0	0	1	0	1	1	V _{11'}	V ₁ +(V ₀ -V ₁) X
0CH	0	0	0	0	1	1	0	0	V _{12'}	V ₁ +(V ₀ -V ₁) X
0DH	0	0	0	0	1	1	0	1	V _{13'}	V ₁ +(V ₀ -V ₁) X
0EH	0	0	0	0	1	1	1	0	V _{14'}	V ₁ +(V ₀ -V ₁) X
0FH	0	0	0	0	1	1	1	1	V _{15'}	V ₁ +(V ₀ -V ₁) X
10H	0	0	0	1	0	0	0	0	V _{16'}	V ₁ +(V ₀ -V ₁) X
11H	0	0	0	1	0	0	0	1	V _{17'}	V ₁ +(V ₀ -V ₁) X
12H	0	0	0	1	0	0	1	0	V _{18'}	V ₁ +(V ₀ -V ₁) X
13H	0	0	0	1	0	0	1	1	V _{19'}	V ₁ +(V ₀ -V ₁) X
14H	0	0	0	1	0	1	0	0	V _{20'}	V ₁ +(V ₀ -V ₁) X
15H	0	0	0	1	0	1	0	1	V _{21'}	V ₁ +(V ₀ -V ₁) X
16H	0	0	0	1	0	1	1	0	V _{22'}	V ₁ +(V ₀ -V ₁) X
17H	0	0	0	1	0	1	1	1	V _{23'}	V ₁ +(V ₀ -V ₁) X
18H	0	0	0	1	1	0	0	0	V _{24'}	V ₁ +(V ₀ -V ₁) X
19H	0	0	0	1	1	0	0	1	V _{25'}	V ₁ +(V ₀ -V ₁) X
1AH	0	0	0	1	1	0	1	0	V _{26'}	V ₁ +(V ₀ -V ₁) X
1BH	0	0	0	1	1	0	1	1	V _{27'}	V ₁ +(V ₀ -V ₁) X
1CH	0	0	0	1	1	1	0	0	V _{28'}	V ₁ +(V ₀ -V ₁) X
1DH	0	0	0	1	1	1	0	1	V _{29'}	V ₁ +(V ₀ -V ₁) X
1EH	0	0	0	1	1	1	1	0	V _{30'}	V ₁ +(V ₀ -V ₁) X
1FH	0	0	0	1	1	1	1	1	V _{31'}	V ₁ +(V ₀ -V ₁) X
20H	0	0	1	0	0	0	0	0	V _{32'}	V ₁
21H	0	0	1	0	0	0	0	1	V _{33'}	V ₂ +(V ₁ -V ₂) X
22H	0	0	1	0	0	0	1	0	V _{34'}	V ₂ +(V ₁ -V ₂) X
23H	0	0	1	0	0	0	1	1	V _{35'}	V ₂ +(V ₁ -V ₂) X
24H	0	0	1	0	0	1	0	0	V _{36'}	V ₂ +(V ₁ -V ₂) X
25H	0	0	1	0	0	1	0	1	V _{37'}	V ₂ +(V ₁ -V ₂) X
26H	0	0	1	0	0	1	1	0	V _{38'}	V ₂ +(V ₁ -V ₂) X
27H	0	0	1	0	0	1	1	1	V _{39'}	V ₂ +(V ₁ -V ₂) X
28H	0	0	1	0	1	0	0	0	V _{40'}	V ₂ +(V ₁ -V ₂) X
29H	0	0	1	0	1	0	0	1	V _{41'}	V ₂ +(V ₁ -V ₂) X
2AH	0	0	1	0	1	0	1	0	V _{42'}	V ₂ +(V ₁ -V ₂) X
2BH	0	0	1	0	1	0	1	1	V _{43'}	V ₂ +(V ₁ -V ₂) X
2CH	0	0	1	0	1	1	0	0	V _{44'}	V ₂ +(V ₁ -V ₂) X
2DH	0	0	1	0	1	1	0	1	V _{45'}	V ₂ +(V ₁ -V ₂) X
2EH	0	0	1	0	1	1	1	0	V _{46'}	V ₂ +(V ₁ -V ₂) X
2FH	0	0	1	0	1	1	1	1	V _{47'}	V ₂ +(V ₁ -V ₂) X
30H	0	0	1	1	0	0	0	0	V _{48'}	V ₂ +(V ₁ -V ₂) X
31H	0	0	1	1	0	0	0	1	V _{49'}	V ₂ +(V ₁ -V ₂) X
32H	0	0	1	1	0	0	1	0	V _{50'}	V ₂ +(V ₁ -V ₂) X
33H	0	0	1	1	0	0	1	1	V _{51'}	V ₂ +(V ₁ -V ₂) X
34H	0	0	1	1	0	1	0	0	V _{52'}	V ₂ +(V ₁ -V ₂) X
35H	0	0	1	1	0	1	0	1	V _{53'}	V ₂ +(V ₁ -V ₂) X
36H	0	0	1	1	0	1	1	0	V _{54'}	V ₂ +(V ₁ -V ₂) X
37H	0	0	1	1	0	1	1	1	V _{55'}	V ₂ +(V ₁ -V ₂) X
38H	0	0	1	1	1	0	0	0	V _{56'}	V ₂ +(V ₁ -V ₂) X
39H	0	0	1	1	1	0	0	1	V _{57'}	V ₂ +(V ₁ -V ₂) X
3AH	0	0	1	1	1	0	1	0	V _{58'}	V ₂ +(V ₁ -V ₂) X
3BH	0	0	1	1	1	0	1	1	V _{59'}	V ₂ +(V ₁ -V ₂) X
3CH	0	0	1	1	1	1	0	0	V _{60'}	V ₂ +(V ₁ -V ₂) X
3DH	0	0	1	1	1	1	0	1	V _{61'}	V ₂ +(V ₁ -V ₂) X
3EH	0	0	1	1	1	1	1	0	V _{62'}	V ₂ +(V ₁ -V ₂) X
3FH	0	0	1	1	1	1	1	1	V _{63'}	V ₂ +(V ₁ -V ₂) X

rn	(Ω)
r0	400.0
r1	362.5
r2	325.0
r3	287.5
r4	250.0
r5	222.5
r6	195.0
r7	170.0
r8	145.0
r9	120.0
r10	120.0
r11	120.0
r12	95.0
r13	95.0
r14	95.0
r15	75.0
r16	75.0
r17	75.0
r18	62.5
r19	62.5
r20	62.5
r21	50.0
r22	50.0
r23	50.0
r24	37.5
r25	37.5
r26	37.5
r27	37.5
r28	37.5
r29	37.5
r30	37.5
r31	37.5
r32	35.0
r33	35.0
r34	35.0
r35	35.0
r36	35.0
r37	35.0
r38	35.0
r39	35.0
r40	32.5
r41	32.5
r42	32.5
r43	32.5
r44	32.5
r45	32.5
r46	32.5
r47	32.5
r48	30.0
r49	30.0
r50	30.0
r51	30.0
r52	30.0
r53	30.0
r54	30.0
r55	30.0
r56	27.5
r57	27.5
r58	27.5
r59	27.5
r60	27.5
r61	27.5
r62	27.5
r63	27.5

Caution There is no connection between V7 and V8 in the chip.

Figure 5-2. Relationship between Input Data and Output Voltage (2/4)

V_{DD2} - 0.2 V > V₀ > V₁ > V₂ > V₃ > V₄ > V₅ > V₆ > V₇ > 0.5 V_{DD2}, POL21/22 = L



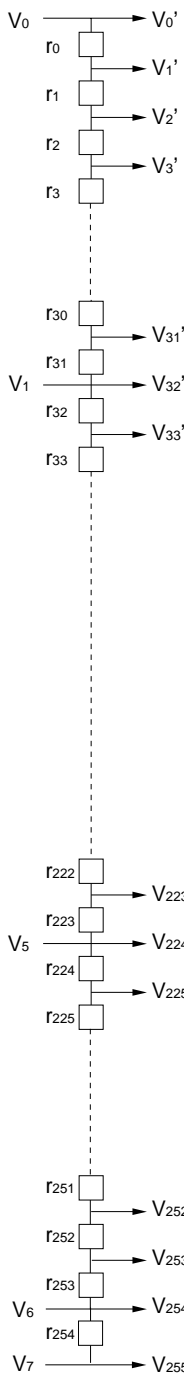
Data	D _{x7}	D _{x6}	D _{x5}	D _{x4}	D _{x3}	D _{x2}	D _{x1}	D _{x0}	Output voltage	
40H	0	1	0	0	0	0	0	0	V ₆₄ '	V ₂
41H	0	1	0	0	0	0	0	1	V ₆₅ '	V ₃ +(V ₂ -V ₃) X
42H	0	1	0	0	0	0	1	0	V ₆₆ '	V ₃ +(V ₂ -V ₃) X
43H	0	1	0	0	0	0	1	1	V ₆₇ '	V ₃ +(V ₂ -V ₃) X
44H	0	1	0	0	0	1	0	0	V ₆₈ '	V ₃ +(V ₂ -V ₃) X
45H	0	1	0	0	0	1	0	1	V ₆₉ '	V ₃ +(V ₂ -V ₃) X
46H	0	1	0	0	0	1	1	0	V ₇₀ '	V ₃ +(V ₂ -V ₃) X
47H	0	1	0	0	0	1	1	1	V ₇₁ '	V ₃ +(V ₂ -V ₃) X
48H	0	1	0	0	1	0	0	0	V ₇₂ '	V ₃ +(V ₂ -V ₃) X
49H	0	1	0	0	1	0	0	1	V ₇₃ '	V ₃ +(V ₂ -V ₃) X
4AH	0	1	0	0	1	0	1	0	V ₇₄ '	V ₃ +(V ₂ -V ₃) X
4BH	0	1	0	0	1	0	1	1	V ₇₅ '	V ₃ +(V ₂ -V ₃) X
4CH	0	1	0	0	1	1	0	0	V ₇₆ '	V ₃ +(V ₂ -V ₃) X
4DH	0	1	0	0	1	1	0	1	V ₇₇ '	V ₃ +(V ₂ -V ₃) X
4EH	0	1	0	0	1	1	1	0	V ₇₈ '	V ₃ +(V ₂ -V ₃) X
4FH	0	1	0	0	1	1	1	1	V ₇₉ '	V ₃ +(V ₂ -V ₃) X
50H	0	1	0	1	0	0	0	0	V ₈₀ '	V ₃ +(V ₂ -V ₃) X
51H	0	1	0	1	0	0	0	1	V ₈₁ '	V ₃ +(V ₂ -V ₃) X
52H	0	1	0	1	0	0	1	0	V ₈₂ '	V ₃ +(V ₂ -V ₃) X
53H	0	1	0	1	0	0	1	1	V ₈₃ '	V ₃ +(V ₂ -V ₃) X
54H	0	1	0	1	0	1	0	0	V ₈₄ '	V ₃ +(V ₂ -V ₃) X
55H	0	1	0	1	0	1	0	1	V ₈₅ '	V ₃ +(V ₂ -V ₃) X
56H	0	1	0	1	0	1	1	0	V ₈₆ '	V ₃ +(V ₂ -V ₃) X
57H	0	1	0	1	0	1	1	1	V ₈₇ '	V ₃ +(V ₂ -V ₃) X
58H	0	1	0	1	1	0	0	0	V ₈₈ '	V ₃ +(V ₂ -V ₃) X
59H	0	1	0	1	1	0	0	1	V ₈₉ '	V ₃ +(V ₂ -V ₃) X
5AH	0	1	0	1	1	0	1	0	V ₉₀ '	V ₃ +(V ₂ -V ₃) X
5BH	0	1	0	1	1	0	1	1	V ₉₁ '	V ₃ +(V ₂ -V ₃) X
5CH	0	1	0	1	1	1	0	0	V ₉₂ '	V ₃ +(V ₂ -V ₃) X
5DH	0	1	0	1	1	1	0	1	V ₉₃ '	V ₃ +(V ₂ -V ₃) X
5EH	0	1	0	1	1	1	1	0	V ₉₄ '	V ₃ +(V ₂ -V ₃) X
5FH	0	1	0	1	1	1	1	1	V ₉₅ '	V ₃ +(V ₂ -V ₃) X
60H	0	1	1	0	0	0	0	0	V ₉₆ '	V ₃ +(V ₂ -V ₃) X
61H	0	1	1	0	0	0	0	1	V ₉₇ '	V ₃ +(V ₂ -V ₃) X
62H	0	1	1	0	0	0	1	0	V ₉₈ '	V ₃ +(V ₂ -V ₃) X
63H	0	1	1	0	0	0	1	1	V ₉₉ '	V ₃ +(V ₂ -V ₃) X
64H	0	1	1	0	0	1	0	0	V ₁₀₀ '	V ₃ +(V ₂ -V ₃) X
65H	0	1	1	0	0	1	0	1	V ₁₀₁ '	V ₃ +(V ₂ -V ₃) X
66H	0	1	1	0	0	1	1	0	V ₁₀₂ '	V ₃ +(V ₂ -V ₃) X
67H	0	1	1	0	0	1	1	1	V ₁₀₃ '	V ₃ +(V ₂ -V ₃) X
68H	0	1	1	0	1	0	0	0	V ₁₀₄ '	V ₃ +(V ₂ -V ₃) X
69H	0	1	1	0	1	0	0	1	V ₁₀₅ '	V ₃ +(V ₂ -V ₃) X
6AH	0	1	1	0	1	0	1	0	V ₁₀₆ '	V ₃ +(V ₂ -V ₃) X
6BH	0	1	1	0	1	0	1	1	V ₁₀₇ '	V ₃ +(V ₂ -V ₃) X
6CH	0	1	1	0	1	1	0	0	V ₁₀₈ '	V ₃ +(V ₂ -V ₃) X
6DH	0	1	1	0	1	1	0	1	V ₁₀₉ '	V ₃ +(V ₂ -V ₃) X
6EH	0	1	1	0	1	1	1	0	V ₁₁₀ '	V ₃ +(V ₂ -V ₃) X
6FH	0	1	1	0	1	1	1	1	V ₁₁₁ '	V ₃ +(V ₂ -V ₃) X
70H	0	1	1	1	0	0	0	0	V ₁₁₂ '	V ₃ +(V ₂ -V ₃) X
71H	0	1	1	1	0	0	0	1	V ₁₁₃ '	V ₃ +(V ₂ -V ₃) X
72H	0	1	1	1	0	0	1	0	V ₁₁₄ '	V ₃ +(V ₂ -V ₃) X
73H	0	1	1	1	0	0	1	1	V ₁₁₅ '	V ₃ +(V ₂ -V ₃) X
74H	0	1	1	1	0	1	0	0	V ₁₁₆ '	V ₃ +(V ₂ -V ₃) X
75H	0	1	1	1	0	1	0	1	V ₁₁₇ '	V ₃ +(V ₂ -V ₃) X
76H	0	1	1	1	0	1	1	0	V ₁₁₈ '	V ₃ +(V ₂ -V ₃) X
77H	0	1	1	1	0	1	1	1	V ₁₁₉ '	V ₃ +(V ₂ -V ₃) X
78H	0	1	1	1	1	0	0	0	V ₁₂₀ '	V ₃ +(V ₂ -V ₃) X
79H	0	1	1	1	1	0	0	1	V ₁₂₁ '	V ₃ +(V ₂ -V ₃) X
7AH	0	1	1	1	1	0	1	0	V ₁₂₂ '	V ₃ +(V ₂ -V ₃) X
7BH	0	1	1	1	1	0	1	1	V ₁₂₃ '	V ₃ +(V ₂ -V ₃) X
7CH	0	1	1	1	1	1	0	0	V ₁₂₄ '	V ₃ +(V ₂ -V ₃) X
7DH	0	1	1	1	1	1	0	1	V ₁₂₅ '	V ₃ +(V ₂ -V ₃) X
7EH	0	1	1	1	1	1	1	0	V ₁₂₆ '	V ₃ +(V ₂ -V ₃) X
7FH	0	1	1	1	1	1	1	1	V ₁₂₇ '	V ₃ +(V ₂ -V ₃) X

rn	(Ω)
r64	25.0
r65	25.0
r66	25.0
r67	25.0
r68	25.0
r69	25.0
r70	25.0
r71	25.0
r72	25.0
r73	25.0
r74	25.0
r75	25.0
r76	25.0
r77	25.0
r78	25.0
r79	25.0
r80	25.0
r81	25.0
r82	25.0
r83	25.0
r84	25.0
r85	25.0
r86	25.0
r87	25.0
r88	25.0
r89	25.0
r90	25.0
r91	25.0
r92	25.0
r93	25.0
r94	25.0
r95	25.0
r96	25.0
r97	25.0
r98	25.0
r99	25.0
r100	25.0
r101	25.0
r102	25.0
r103	25.0
r104	25.0
r105	25.0
r106	25.0
r107	25.0
r108	25.0
r109	25.0
r110	25.0
r111	25.0
r112	25.0
r113	25.0
r114	25.0
r115	25.0
r116	25.0
r117	25.0
r118	25.0
r119	25.0
r120	25.0
r121	25.0
r122	25.0
r123	25.0
r124	25.0
r125	25.0
r126	25.0
r127	25.0

Caution There is no connection between V₇ and V₈ in the chip.

Figure 5-2. Relationship between Input Data and Output Voltage (3/4)

V_{DD2} - 0.2 V > V₀ > V₁ > V₂ > V₃ > V₄ > V₅ > V₆ > V₇ > 0.5 V_{DD2}, POL21/22 = L



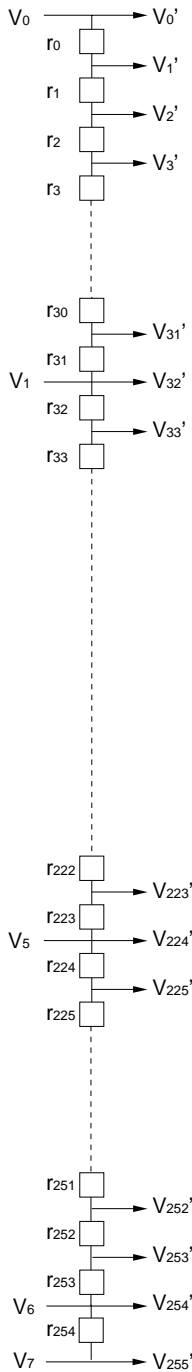
Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage			
80H	1	0	0	0	0	0	0	0	V _{128'}	V ₃		
81H	1	0	0	0	0	0	0	1	V _{129'}	V _{4+(V3-V4)}	X	1875.0 / 1900.0
82H	1	0	0	0	0	0	1	0	V _{130'}	V _{4+(V3-V4)}	X	1850.0 / 1900.0
83H	1	0	0	0	0	0	1	1	V _{131'}	V _{4+(V3-V4)}	X	1825.0 / 1900.0
84H	1	0	0	0	0	1	0	0	V _{132'}	V _{4+(V3-V4)}	X	1800.0 / 1900.0
85H	1	0	0	0	0	1	0	1	V _{133'}	V _{4+(V3-V4)}	X	1775.0 / 1900.0
86H	1	0	0	0	0	1	1	0	V _{134'}	V _{4+(V3-V4)}	X	1750.0 / 1900.0
87H	1	0	0	0	0	1	1	1	V _{135'}	V _{4+(V3-V4)}	X	1725.0 / 1900.0
88H	1	0	0	0	1	0	0	0	V _{136'}	V _{4+(V3-V4)}	X	1700.0 / 1900.0
89H	1	0	0	0	1	0	0	1	V _{137'}	V _{4+(V3-V4)}	X	1675.0 / 1900.0
8AH	1	0	0	0	1	0	1	0	V _{138'}	V _{4+(V3-V4)}	X	1650.0 / 1900.0
8BH	1	0	0	0	1	0	1	1	V _{139'}	V _{4+(V3-V4)}	X	1625.0 / 1900.0
8CH	1	0	0	0	1	1	0	0	V _{140'}	V _{4+(V3-V4)}	X	1600.0 / 1900.0
8DH	1	0	0	0	1	1	0	1	V _{141'}	V _{4+(V3-V4)}	X	1575.0 / 1900.0
8EH	1	0	0	0	1	1	1	0	V _{142'}	V _{4+(V3-V4)}	X	1550.0 / 1900.0
8FH	1	0	0	0	1	1	1	1	V _{143'}	V _{4+(V3-V4)}	X	1525.0 / 1900.0
90H	1	0	0	1	0	0	0	0	V _{144'}	V _{4+(V3-V4)}	X	1500.0 / 1900.0
91H	1	0	0	1	0	0	0	1	V _{145'}	V _{4+(V3-V4)}	X	1475.0 / 1900.0
92H	1	0	0	1	0	0	1	0	V _{146'}	V _{4+(V3-V4)}	X	1450.0 / 1900.0
93H	1	0	0	1	0	0	1	1	V _{147'}	V _{4+(V3-V4)}	X	1425.0 / 1900.0
94H	1	0	0	1	0	1	0	0	V _{148'}	V _{4+(V3-V4)}	X	1400.0 / 1900.0
95H	1	0	0	1	0	1	0	1	V _{149'}	V _{4+(V3-V4)}	X	1375.0 / 1900.0
96H	1	0	0	1	0	1	1	0	V _{150'}	V _{4+(V3-V4)}	X	1350.0 / 1900.0
97H	1	0	0	1	0	1	1	1	V _{151'}	V _{4+(V3-V4)}	X	1325.0 / 1900.0
98H	1	0	0	1	1	0	0	0	V _{152'}	V _{4+(V3-V4)}	X	1300.0 / 1900.0
99H	1	0	0	1	1	0	0	1	V _{153'}	V _{4+(V3-V4)}	X	1272.5 / 1900.0
9AH	1	0	0	1	1	0	1	0	V _{154'}	V _{4+(V3-V4)}	X	1245.0 / 1900.0
9BH	1	0	0	1	1	0	1	1	V _{155'}	V _{4+(V3-V4)}	X	1217.5 / 1900.0
9CH	1	0	0	1	1	1	0	0	V _{156'}	V _{4+(V3-V4)}	X	1190.0 / 1900.0
9DH	1	0	0	1	1	1	0	1	V _{157'}	V _{4+(V3-V4)}	X	1162.5 / 1900.0
9EH	1	0	0	1	1	1	1	0	V _{158'}	V _{4+(V3-V4)}	X	1135.0 / 1900.0
9FH	1	0	0	1	1	1	1	1	V _{159'}	V _{4+(V3-V4)}	X	1107.5 / 1900.0
A0H	1	0	1	0	0	0	0	0	V _{160'}	V _{4+(V3-V4)}	X	1080.0 / 1900.0
A1H	1	0	1	0	0	0	0	1	V _{161'}	V _{4+(V3-V4)}	X	1050.0 / 1900.0
A2H	1	0	1	0	0	0	1	0	V _{162'}	V _{4+(V3-V4)}	X	1020.0 / 1900.0
A3H	1	0	1	0	0	0	1	1	V _{163'}	V _{4+(V3-V4)}	X	990.0 / 1900.0
A4H	1	0	1	0	0	1	0	0	V _{164'}	V _{4+(V3-V4)}	X	960.0 / 1900.0
A5H	1	0	1	0	0	1	0	1	V _{165'}	V _{4+(V3-V4)}	X	930.0 / 1900.0
A6H	1	0	1	0	0	1	1	0	V _{166'}	V _{4+(V3-V4)}	X	900.0 / 1900.0
A7H	1	0	1	0	0	1	1	1	V _{167'}	V _{4+(V3-V4)}	X	870.0 / 1900.0
A8H	1	0	1	0	1	0	0	0	V _{168'}	V _{4+(V3-V4)}	X	840.0 / 1900.0
A9H	1	0	1	0	1	0	0	1	V _{169'}	V _{4+(V3-V4)}	X	807.5 / 1900.0
AAH	1	0	1	0	1	0	1	0	V _{170'}	V _{4+(V3-V4)}	X	775.0 / 1900.0
ABH	1	0	1	0	1	0	1	1	V _{171'}	V _{4+(V3-V4)}	X	742.5 / 1900.0
ACH	1	0	1	0	1	1	0	0	V _{172'}	V _{4+(V3-V4)}	X	710.0 / 1900.0
ADH	1	0	1	0	1	1	0	1	V _{173'}	V _{4+(V3-V4)}	X	677.5 / 1900.0
AEH	1	0	1	0	1	1	1	0	V _{174'}	V _{4+(V3-V4)}	X	645.0 / 1900.0
AFH	1	0	1	0	1	1	1	1	V _{175'}	V _{4+(V3-V4)}	X	612.5 / 1900.0
B0H	1	0	1	1	0	0	0	0	V _{176'}	V _{4+(V3-V4)}	X	580.0 / 1900.0
B1H	1	0	1	1	0	0	0	1	V _{177'}	V _{4+(V3-V4)}	X	545.0 / 1900.0
B2H	1	0	1	1	0	0	1	0	V _{178'}	V _{4+(V3-V4)}	X	510.0 / 1900.0
B3H	1	0	1	1	0	0	1	1	V _{179'}	V _{4+(V3-V4)}	X	475.0 / 1900.0
B4H	1	0	1	1	0	1	0	0	V _{180'}	V _{4+(V3-V4)}	X	440.0 / 1900.0
B5H	1	0	1	1	0	1	0	1	V _{181'}	V _{4+(V3-V4)}	X	405.0 / 1900.0
B6H	1	0	1	1	0	1	1	0	V _{182'}	V _{4+(V3-V4)}	X	370.0 / 1900.0
B7H	1	0	1	1	0	1	1	1	V _{183'}	V _{4+(V3-V4)}	X	335.0 / 1900.0
B8H	1	0	1	1	1	0	0	0	V _{184'}	V _{4+(V3-V4)}	X	300.0 / 1900.0
B9H	1	0	1	1	1	0	0	1	V _{185'}	V _{4+(V3-V4)}	X	262.5 / 1900.0
BAH	1	0	1	1	1	0	1	0	V _{186'}	V _{4+(V3-V4)}	X	225.0 / 1900.0
BBH	1	0	1	1	1	0	1	1	V _{187'}	V _{4+(V3-V4)}	X	187.5 / 1900.0
BCH	1	0	1	1	1	1	0	0	V _{188'}	V _{4+(V3-V4)}	X	150.0 / 1900.0
BDH	1	0	1	1	1	1	0	1	V _{189'}	V _{4+(V3-V4)}	X	112.5 / 1900.0
BEH	1	0	1	1	1	1	1	0	V _{190'}	V _{4+(V3-V4)}	X	75.0 / 1900.0
BFH	1	0	1	1	1	1	1	1	V _{191'}	V _{4+(V3-V4)}	X	37.5 / 1900.0

rn	(Ω)
r128	25.0
r129	25.0
r130	25.0
r131	25.0
r132	25.0
r133	25.0
r134	25.0
r135	25.0
r136	25.0
r137	25.0
r138	25.0
r139	25.0
r140	25.0
r141	25.0
r142	25.0
r143	25.0
r144	25.0
r145	25.0
r146	25.0
r147	25.0
r148	25.0
r149	25.0
r150	25.0
r151	25.0
r152	27.5
r153	27.5
r154	27.5
r155	27.5
r156	27.5
r157	27.5
r158	27.5
r159	27.5
r160	30.0
r161	30.0
r162	30.0
r163	30.0
r164	30.0
r165	30.0
r166	30.0
r167	30.0
r168	32.5
r169	32.5
r170	32.5
r171	32.5
r172	32.5
r173	32.5
r174	32.5
r175	32.5
r176	35.0
r177	35.0
r178	35.0
r179	35.0
r180	35.0
r181	35.0
r182	35.0
r183	35.0
r184	37.5
r185	37.5
r186	37.5
r187	37.5
r188	37.5
r189	37.5
r190	37.5
r191	37.5

Caution There is no connection between V₇ and V₈ in the chip.

Figure 5-2. Relationship between Input Data and Output Voltage (4/4)

$$V_{DD2} - 0.2\text{ V} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > 0.5 V_{DD2}$$



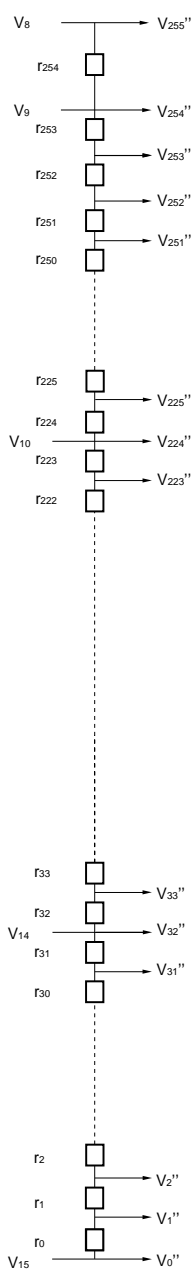
Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage			
C0H	1	1	0	0	0	0	0	0	V192'	V4		
C1H	1	1	0	0	0	0	0	1	V193'	V5+(V4-V5) X	1557.5 /	1600.0
C2H	1	1	0	0	0	0	1	0	V194'	V5+(V4-V5) X	1515.0 /	1600.0
C3H	1	1	0	0	0	0	1	1	V195'	V5+(V4-V5) X	1472.5 /	1600.0
C4H	1	1	0	0	0	1	0	0	V196'	V5+(V4-V5) X	1430.0 /	1600.0
C5H	1	1	0	0	0	1	0	1	V197'	V5+(V4-V5) X	1387.5 /	1600.0
C6H	1	1	0	0	0	1	1	0	V198'	V5+(V4-V5) X	1345.0 /	1600.0
C7H	1	1	0	0	0	1	1	1	V199'	V5+(V4-V5) X	1302.5 /	1600.0
C8H	1	1	0	0	1	0	0	0	V200'	V5+(V4-V5) X	1260.0 /	1600.0
C9H	1	1	0	0	1	0	0	1	V201'	V5+(V4-V5) X	1212.5 /	1600.0
CAH	1	1	0	0	1	0	1	0	V202'	V5+(V4-V5) X	1165.0 /	1600.0
CBH	1	1	0	0	1	0	1	1	V203'	V5+(V4-V5) X	1117.5 /	1600.0
CCH	1	1	0	0	1	1	0	0	V204'	V5+(V4-V5) X	1070.0 /	1600.0
CDH	1	1	0	0	1	1	0	1	V205'	V5+(V4-V5) X	1022.5 /	1600.0
CEH	1	1	0	0	1	1	1	0	V206'	V5+(V4-V5) X	975.0 /	1600.0
CFH	1	1	0	0	1	1	1	1	V207'	V5+(V4-V5) X	927.5 /	1600.0
D0H	1	1	0	1	0	0	0	0	V208'	V5+(V4-V5) X	880.0 /	1600.0
D1H	1	1	0	1	0	0	0	1	V209'	V5+(V4-V5) X	827.5 /	1600.0
D2H	1	1	0	1	0	0	1	0	V210'	V5+(V4-V5) X	775.0 /	1600.0
D3H	1	1	0	1	0	0	1	1	V211'	V5+(V4-V5) X	722.5 /	1600.0
D4H	1	1	0	1	0	1	0	0	V212'	V5+(V4-V5) X	670.0 /	1600.0
D5H	1	1	0	1	0	1	0	1	V213'	V5+(V4-V5) X	617.5 /	1600.0
D6H	1	1	0	1	0	1	1	0	V214'	V5+(V4-V5) X	565.0 /	1600.0
D7H	1	1	0	1	0	1	1	1	V215'	V5+(V4-V5) X	512.5 /	1600.0
D8H	1	1	0	1	1	0	0	0	V216'	V5+(V4-V5) X	460.0 /	1600.0
D9H	1	1	0	1	1	0	0	1	V217'	V5+(V4-V5) X	402.5 /	1600.0
DAH	1	1	0	1	1	0	1	0	V218'	V5+(V4-V5) X	345.0 /	1600.0
DBH	1	1	0	1	1	0	1	1	V219'	V5+(V4-V5) X	287.5 /	1600.0
DCH	1	1	0	1	1	1	0	0	V220'	V5+(V4-V5) X	230.0 /	1600.0
DDH	1	1	0	1	1	1	0	1	V221'	V5+(V4-V5) X	172.5 /	1600.0
DEH	1	1	0	1	1	1	1	0	V222'	V5+(V4-V5) X	115.0 /	1600.0
DFH	1	1	0	1	1	1	1	1	V223'	V5+(V4-V5) X	57.5 /	1600.0
E0H	1	1	1	0	0	0	0	0	V224'	V5		
E1H	1	1	1	0	0	0	0	1	V225'	V6+(V5-V6) X	4630.0 /	4687.5
E2H	1	1	1	0	0	0	1	0	V226'	V6+(V5-V6) X	4560.0 /	4687.5
E3H	1	1	1	0	0	0	1	1	V227'	V6+(V5-V6) X	4490.0 /	4687.5
E4H	1	1	1	0	0	1	0	0	V228'	V6+(V5-V6) X	4420.0 /	4687.5
E5H	1	1	1	0	0	1	0	1	V229'	V6+(V5-V6) X	4337.5 /	4687.5
E6H	1	1	1	0	0	1	1	0	V230'	V6+(V5-V6) X	4255.0 /	4687.5
E7H	1	1	1	0	0	1	1	1	V231'	V6+(V5-V6) X	4172.5 /	4687.5
E8H	1	1	1	0	1	0	0	0	V232'	V6+(V5-V6) X	4077.5 /	4687.5
E9H	1	1	1	0	1	0	0	1	V233'	V6+(V5-V6) X	3982.5 /	4687.5
EAH	1	1	1	0	1	0	1	0	V234'	V6+(V5-V6) X	3887.5 /	4687.5
EBH	1	1	1	0	1	0	1	1	V235'	V6+(V5-V6) X	3775.0 /	4687.5
ECH	1	1	1	0	1	1	0	0	V236'	V6+(V5-V6) X	3662.5 /	4687.5
EDH	1	1	1	0	1	1	0	1	V237'	V6+(V5-V6) X	3550.0 /	4687.5
EEH	1	1	1	0	1	1	1	0	V238'	V6+(V5-V6) X	3420.0 /	4687.5
EFH	1	1	1	0	1	1	1	1	V239'	V6+(V5-V6) X	3290.0 /	4687.5
F0H	1	1	1	1	0	0	0	0	V240'	V6+(V5-V6) X	3142.5 /	4687.5
F1H	1	1	1	1	0	0	0	1	V241'	V6+(V5-V6) X	2995.0 /	4687.5
F2H	1	1	1	1	0	0	1	0	V242'	V6+(V5-V6) X	2830.0 /	4687.5
F3H	1	1	1	1	0	0	1	1	V243'	V6+(V5-V6) X	2665.0 /	4687.5
F4H	1	1	1	1	0	1	0	0	V244'	V6+(V5-V6) X	2482.5 /	4687.5
F5H	1	1	1	1	0	1	0	1	V245'	V6+(V5-V6) X	2300.0 /	4687.5
F6H	1	1	1	1	0	1	1	0	V246'	V6+(V5-V6) X	2100.0 /	4687.5
F7H	1	1	1	1	0	1	1	1	V247'	V6+(V5-V6) X	1900.0 /	4687.5
F8H	1	1	1	1	1	0	0	0	V248'	V6+(V5-V6) X	1675.0 /	4687.5
F9H	1	1	1	1	1	0	0	1	V249'	V6+(V5-V6) X	1450.0 /	4687.5
FAH	1	1	1	1	1	0	1	0	V250'	V6+(V5-V6) X	1200.0 /	4687.5
FBH	1	1	1	1	1	0	1	1	V251'	V6+(V5-V6) X	950.0 /	4687.5
FCH	1	1	1	1	1	1	0	0	V252'	V6+(V5-V6) X	650.0 /	4687.5
FDH	1	1	1	1	1	1	0	1	V253'	V6+(V5-V6) X	350.0 /	4687.5
FEH	1	1	1	1	1	1	1	0	V254'	V6		
FFH	1	1	1	1	1	1	1	1	V255'	V7		

rn	(Ω)
r192	42.5
r193	42.5
r194	42.5
r195	42.5
r196	42.5
r197	42.5
r198	42.5
r199	42.5
r200	47.5
r201	47.5
r202	47.5
r203	47.5
r204	47.5
r205	47.5
r206	47.5
r207	47.5
r208	52.5
r209	52.5
r210	52.5
r211	52.5
r212	52.5
r213	52.5
r214	52.5
r215	52.5
r216	57.5
r217	57.5
r218	57.5
r219	57.5
r220	57.5
r221	57.5
r222	57.5
r223	57.5
r224	57.5
r225	70.0
r226	70.0
r227	70.0
r228	82.5
r229	82.5
r230	82.5
r231	95.0
r232	95.0
r233	95.0
r234	112.5
r235	112.5
r236	112.5
r237	130.0
r238	130.0
r239	147.5
r240	147.5
r241	165.0
r242	165.0
r243	182.5
r244	182.5
r245	200.0
r246	200.0
r247	225.0
r248	225.0
r249	250.0
r250	250.0
r251	300.0
r252	300.0
r253	350.0
r254	350.0
TOTAL	15002.5

Caution There is no connection between V7 and V8 in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage (1/4)

0.5 VDD2 - 0.3 V > V8 > V9 > V10 > V11 > V12 > V13 > V14 > V15 > VSS2 + 0.2 V, POL21/22 = L



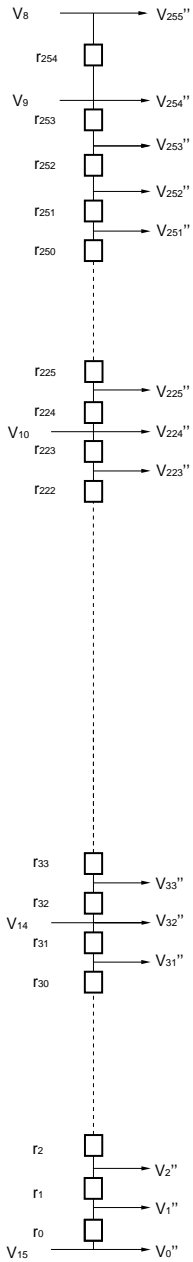
Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage	
00H	0	0	0	0	0	0	0	0	V0"	V15
01H	0	0	0	0	0	0	0	1	V1"	V15+(V14-V15) X
02H	0	0	0	0	0	0	1	0	V2"	V15+(V14-V15) X
03H	0	0	0	0	0	0	1	1	V3"	V15+(V14-V15) X
04H	0	0	0	0	0	1	0	0	V4"	V15+(V14-V15) X
05H	0	0	0	0	0	1	0	1	V5"	V15+(V14-V15) X
06H	0	0	0	0	0	1	1	0	V6"	V15+(V14-V15) X
07H	0	0	0	0	0	1	1	1	V7"	V15+(V14-V15) X
08H	0	0	0	0	1	0	0	0	V8"	V15+(V14-V15) X
09H	0	0	0	0	1	0	0	1	V9"	V15+(V14-V15) X
0AH	0	0	0	0	1	0	1	0	V10"	V15+(V14-V15) X
0BH	0	0	0	0	1	0	1	1	V11"	V15+(V14-V15) X
0CH	0	0	0	0	1	1	0	0	V12"	V15+(V14-V15) X
0DH	0	0	0	0	1	1	0	1	V13"	V15+(V14-V15) X
0EH	0	0	0	0	1	1	1	0	V14"	V15+(V14-V15) X
0FH	0	0	0	0	1	1	1	1	V15"	V15+(V14-V15) X
10H	0	0	0	1	0	0	0	0	V16"	V15+(V14-V15) X
11H	0	0	0	1	0	0	0	1	V17"	V15+(V14-V15) X
12H	0	0	0	1	0	0	1	0	V18"	V15+(V14-V15) X
13H	0	0	0	1	0	0	1	1	V19"	V15+(V14-V15) X
14H	0	0	0	1	0	1	0	0	V20"	V15+(V14-V15) X
15H	0	0	0	1	0	1	0	1	V21"	V15+(V14-V15) X
16H	0	0	0	1	0	1	1	0	V22"	V15+(V14-V15) X
17H	0	0	0	1	0	1	1	1	V23"	V15+(V14-V15) X
18H	0	0	0	1	1	0	0	0	V24"	V15+(V14-V15) X
19H	0	0	0	1	1	0	0	1	V25"	V15+(V14-V15) X
1AH	0	0	0	1	1	0	1	0	V26"	V15+(V14-V15) X
1BH	0	0	0	1	1	0	1	1	V27"	V15+(V14-V15) X
1CH	0	0	0	1	1	1	0	0	V28"	V15+(V14-V15) X
1DH	0	0	0	1	1	1	0	1	V29"	V15+(V14-V15) X
1EH	0	0	0	1	1	1	1	0	V30"	V15+(V14-V15) X
1FH	0	0	0	1	1	1	1	1	V31"	V15+(V14-V15) X
20H	0	0	1	0	0	0	0	0	V32"	V14
21H	0	0	1	0	0	0	0	1	V33"	V14+(V13-V14) X
22H	0	0	1	0	0	0	1	0	V34"	V14+(V13-V14) X
23H	0	0	1	0	0	0	1	1	V35"	V14+(V13-V14) X
24H	0	0	1	0	0	1	0	0	V36"	V14+(V13-V14) X
25H	0	0	1	0	0	1	0	1	V37"	V14+(V13-V14) X
26H	0	0	1	0	0	1	1	0	V38"	V14+(V13-V14) X
27H	0	0	1	0	0	1	1	1	V39"	V14+(V13-V14) X
28H	0	0	1	0	1	0	0	0	V40"	V14+(V13-V14) X
29H	0	0	1	0	1	0	0	1	V41"	V14+(V13-V14) X
2AH	0	0	1	0	1	0	1	0	V42"	V14+(V13-V14) X
2BH	0	0	1	0	1	0	1	1	V43"	V14+(V13-V14) X
2CH	0	0	1	0	1	1	0	0	V44"	V14+(V13-V14) X
2DH	0	0	1	0	1	1	0	1	V45"	V14+(V13-V14) X
2EH	0	0	1	0	1	1	1	0	V46"	V14+(V13-V14) X
2FH	0	0	1	0	1	1	1	1	V47"	V14+(V13-V14) X
30H	0	0	1	1	0	0	0	0	V48"	V14+(V13-V14) X
31H	0	0	1	1	0	0	0	1	V49"	V14+(V13-V14) X
32H	0	0	1	1	0	0	1	0	V50"	V14+(V13-V14) X
33H	0	0	1	1	0	0	1	1	V51"	V14+(V13-V14) X
34H	0	0	1	1	0	1	0	0	V52"	V14+(V13-V14) X
35H	0	0	1	1	0	1	0	1	V53"	V14+(V13-V14) X
36H	0	0	1	1	0	1	1	0	V54"	V14+(V13-V14) X
37H	0	0	1	1	0	1	1	1	V55"	V14+(V13-V14) X
38H	0	0	1	1	1	0	0	0	V56"	V14+(V13-V14) X
39H	0	0	1	1	1	0	0	1	V57"	V14+(V13-V14) X
3AH	0	0	1	1	1	0	1	0	V58"	V14+(V13-V14) X
3BH	0	0	1	1	1	0	1	1	V59"	V14+(V13-V14) X
3CH	0	0	1	1	1	1	0	0	V60"	V14+(V13-V14) X
3DH	0	0	1	1	1	1	0	1	V61"	V14+(V13-V14) X
3EH	0	0	1	1	1	1	1	0	V62"	V14+(V13-V14) X
3FH	0	0	1	1	1	1	1	1	V63"	V14+(V13-V14) X

rn	(Ω)
r0	400.0
r1	362.5
r2	325.0
r3	287.5
r4	250.0
r5	222.5
r6	195.0
r7	170.0
r8	145.0
r9	120.0
r10	120.0
r11	120.0
r12	95.0
r13	95.0
r14	95.0
r15	75.0
r16	75.0
r17	75.0
r18	62.5
r19	62.5
r20	62.5
r21	50.0
r22	50.0
r23	50.0
r24	37.5
r25	37.5
r26	37.5
r27	37.5
r28	37.5
r29	37.5
r30	37.5
r31	37.5
r32	35.0
r33	35.0
r34	35.0
r35	35.0
r36	35.0
r37	35.0
r38	35.0
r39	35.0
r40	32.5
r41	32.5
r42	32.5
r43	32.5
r44	32.5
r45	32.5
r46	32.5
r47	32.5
r48	30.0
r49	30.0
r50	30.0
r51	30.0
r52	30.0
r53	30.0
r54	30.0
r55	30.0
r56	27.5
r57	27.5
r58	27.5
r59	27.5
r60	27.5
r61	27.5
r62	27.5
r63	27.5

Caution There is no connection between V7 and V8 in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage (2/4)

0.5 V_{DD2} – 0.3 V > V₈ > V₉ > V₁₀ > V₁₁ > V₁₂ > V₁₃ > V₁₄ > V₁₅ > V_{SS2} + 0.2 V, POL21/22 = L



Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage			
40H	0	1	0	0	0	0	0	0	V ₆₄ ⁿ	V ₁₃		
41H	0	1	0	0	0	0	0	1	V ₆₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	25	/ 1600
42H	0	1	0	0	0	0	1	0	V ₆₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	50	/ 1600
43H	0	1	0	0	0	0	1	1	V ₆₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	75	/ 1600
44H	0	1	0	0	0	1	0	0	V ₆₈ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	100	/ 1600
45H	0	1	0	0	0	1	0	1	V ₆₉ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	125	/ 1600
46H	0	1	0	0	0	1	1	0	V ₇₀ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	150	/ 1600
47H	0	1	0	0	0	1	1	1	V ₇₁ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	175	/ 1600
48H	0	1	0	0	1	0	0	0	V ₇₂ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	200	/ 1600
49H	0	1	0	0	1	0	0	1	V ₇₃ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	225	/ 1600
4AH	0	1	0	0	1	0	1	0	V ₇₄ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	250	/ 1600
4BH	0	1	0	0	1	0	1	1	V ₇₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	275	/ 1600
4CH	0	1	0	0	1	1	0	0	V ₇₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	300	/ 1600
4DH	0	1	0	0	1	1	0	1	V ₇₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	325	/ 1600
4EH	0	1	0	0	1	1	1	0	V ₇₈ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	350	/ 1600
4FH	0	1	0	0	1	1	1	1	V ₇₉ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	375	/ 1600
50H	0	1	0	1	0	0	0	0	V ₈₀ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	400	/ 1600
51H	0	1	0	1	0	0	0	1	V ₈₁ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	425	/ 1600
52H	0	1	0	1	0	0	1	0	V ₈₂ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	450	/ 1600
53H	0	1	0	1	0	0	1	1	V ₈₃ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	475	/ 1600
54H	0	1	0	1	0	1	0	0	V ₈₄ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	500	/ 1600
55H	0	1	0	1	0	1	0	1	V ₈₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	525	/ 1600
56H	0	1	0	1	0	1	1	0	V ₈₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	550	/ 1600
57H	0	1	0	1	0	1	1	1	V ₈₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	575	/ 1600
58H	0	1	0	1	1	0	0	0	V ₈₈ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	600	/ 1600
59H	0	1	0	1	1	0	0	1	V ₈₉ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	625	/ 1600
5AH	0	1	0	1	1	0	1	0	V ₉₀ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	650	/ 1600
5BH	0	1	0	1	1	0	1	1	V ₉₁ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	675	/ 1600
5CH	0	1	0	1	1	1	0	0	V ₉₂ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	700	/ 1600
5DH	0	1	0	1	1	1	0	1	V ₉₃ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	725	/ 1600
5EH	0	1	0	1	1	1	1	0	V ₉₄ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	750	/ 1600
5FH	0	1	0	1	1	1	1	1	V ₉₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	775	/ 1600
60H	0	1	1	0	0	0	0	0	V ₉₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	800	/ 1600
61H	0	1	1	0	0	0	0	1	V ₉₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	825	/ 1600
62H	0	1	1	0	0	0	1	0	V ₉₈ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	850	/ 1600
63H	0	1	1	0	0	0	1	1	V ₉₉ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	875	/ 1600
64H	0	1	1	0	0	1	0	0	V ₁₀₀ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	900	/ 1600
65H	0	1	1	0	0	1	0	1	V ₁₀₁ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	925	/ 1600
66H	0	1	1	0	0	1	1	0	V ₁₀₂ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	950	/ 1600
67H	0	1	1	0	0	1	1	1	V ₁₀₃ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	975	/ 1600
68H	0	1	1	0	1	0	0	0	V ₁₀₄ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1000	/ 1600
69H	0	1	1	0	1	0	0	1	V ₁₀₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1025	/ 1600
6AH	0	1	1	0	1	0	1	0	V ₁₀₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1050	/ 1600
6BH	0	1	1	0	1	0	1	1	V ₁₀₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1075	/ 1600
6CH	0	1	1	0	1	1	0	0	V ₁₀₈ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1100	/ 1600
6DH	0	1	1	0	1	1	0	1	V ₁₀₉ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1125	/ 1600
6EH	0	1	1	0	1	1	1	0	V ₁₁₀ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1150	/ 1600
6FH	0	1	1	0	1	1	1	1	V ₁₁₁ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1175	/ 1600
70H	0	1	1	1	0	0	0	0	V ₁₁₂ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1200	/ 1600
71H	0	1	1	1	0	0	0	1	V ₁₁₃ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1225	/ 1600
72H	0	1	1	1	0	0	1	0	V ₁₁₄ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1250	/ 1600
73H	0	1	1	1	0	0	1	1	V ₁₁₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1275	/ 1600
74H	0	1	1	1	0	1	0	0	V ₁₁₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1300	/ 1600
75H	0	1	1	1	0	1	0	1	V ₁₁₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1325	/ 1600
76H	0	1	1	1	0	1	1	0	V ₁₁₈ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1350	/ 1600
77H	0	1	1	1	0	1	1	1	V ₁₁₉ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1375	/ 1600
78H	0	1	1	1	1	0	0	0	V ₁₂₀ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1400	/ 1600
79H	0	1	1	1	1	0	0	1	V ₁₂₁ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1425	/ 1600
7AH	0	1	1	1	1	0	1	0	V ₁₂₂ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1450	/ 1600
7BH	0	1	1	1	1	0	1	1	V ₁₂₃ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1475	/ 1600
7CH	0	1	1	1	1	1	0	0	V ₁₂₄ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1500	/ 1600
7DH	0	1	1	1	1	1	0	1	V ₁₂₅ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1525	/ 1600
7EH	0	1	1	1	1	1	1	0	V ₁₂₆ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1550	/ 1600
7FH	0	1	1	1	1	1	1	1	V ₁₂₇ ⁿ	V ₁₃ +(V ₁₂ -V ₁₃) X	1575	/ 1600

m	(Ω)
r64	25.0
r65	25.0
r66	25.0
r67	25.0
r68	25.0
r69	25.0
r70	25.0
r71	25.0
r72	25.0
r73	25.0
r74	25.0
r75	25.0
r76	25.0
r77	25.0
r78	25.0
r79	25.0
r80	25.0
r81	25.0
r82	25.0
r83	25.0
r84	25.0
r85	25.0
r86	25.0
r87	25.0
r88	25.0
r89	25.0
r90	25.0
r91	25.0
r92	25.0
r93	25.0
r94	25.0
r95	25.0
r96	25.0
r97	25.0
r98	25.0
r99	25.0
r100	25.0
r101	25.0
r102	25.0
r103	25.0
r104	25.0
r105	25.0
r106	25.0
r107	25.0
r108	25.0
r109	25.0
r110	25.0
r111	25.0
r112	25.0
r113	25.0
r114	25.0
r115	25.0
r116	25.0
r117	25.0
r118	25.0
r119	25.0
r120	25.0
r121	25.0
r122	25.0
r123	25.0
r124	25.0
r125	25.0
r126	25.0
r127	25.0

Caution There is no connection between V₇ and V₈ in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage (3/4)

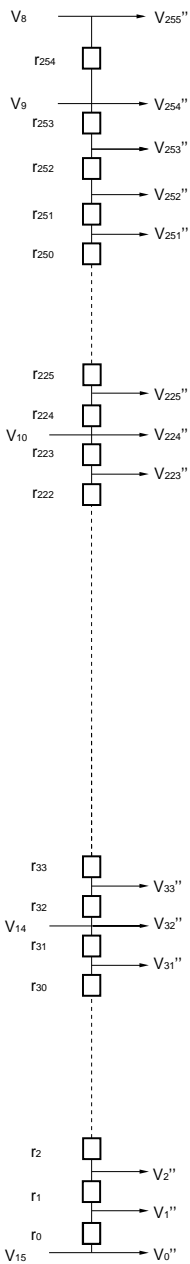
0.5 VDD2 – 0.3 V > V8 > V9 > V10 > V11 > V12 > V13 > V14 > V15 > VSS2 + 0.2 V, POL21/22 = L

Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage		r	(Ω)
80H	1	0	0	0	0	0	0	0	V128''	V12	r128	25.0
81H	1	0	0	0	0	0	0	1	V129''	V12+(V11-V12) X	r129	25.0
82H	1	0	0	0	0	0	1	0	V130''	V12+(V11-V12) X	r130	25.0
83H	1	0	0	0	0	0	1	1	V131''	V12+(V11-V12) X	r131	25.0
84H	1	0	0	0	0	1	0	0	V132''	V12+(V11-V12) X	r132	25.0
85H	1	0	0	0	0	1	0	1	V133''	V12+(V11-V12) X	r133	25.0
86H	1	0	0	0	0	1	1	0	V134''	V12+(V11-V12) X	r134	25.0
87H	1	0	0	0	0	1	1	1	V135''	V12+(V11-V12) X	r135	25.0
88H	1	0	0	0	1	0	0	0	V136''	V12+(V11-V12) X	r136	25.0
89H	1	0	0	0	1	0	0	1	V137''	V12+(V11-V12) X	r137	25.0
8AH	1	0	0	0	1	0	1	0	V138''	V12+(V11-V12) X	r138	25.0
8BH	1	0	0	0	1	0	1	1	V139''	V12+(V11-V12) X	r139	25.0
8CH	1	0	0	0	1	1	0	0	V140''	V12+(V11-V12) X	r140	25.0
8DH	1	0	0	0	1	1	0	1	V141''	V12+(V11-V12) X	r141	25.0
8EH	1	0	0	0	1	1	1	0	V142''	V12+(V11-V12) X	r142	25.0
8FH	1	0	0	0	1	1	1	1	V143''	V12+(V11-V12) X	r143	25.0
90H	1	0	0	1	0	0	0	0	V144''	V12+(V11-V12) X	r144	25.0
91H	1	0	0	1	0	0	0	1	V145''	V12+(V11-V12) X	r145	25.0
92H	1	0	0	1	0	0	1	0	V146''	V12+(V11-V12) X	r146	25.0
93H	1	0	0	1	0	0	1	1	V147''	V12+(V11-V12) X	r147	25.0
94H	1	0	0	1	0	1	0	0	V148''	V12+(V11-V12) X	r148	25.0
95H	1	0	0	1	0	1	0	1	V149''	V12+(V11-V12) X	r149	25.0
96H	1	0	0	1	0	1	1	0	V150''	V12+(V11-V12) X	r150	25.0
97H	1	0	0	1	0	1	1	1	V151''	V12+(V11-V12) X	r151	25.0
98H	1	0	0	1	1	0	0	0	V152''	V12+(V11-V12) X	r152	27.5
99H	1	0	0	1	1	0	0	1	V153''	V12+(V11-V12) X	r153	27.5
9AH	1	0	0	1	1	0	1	0	V154''	V12+(V11-V12) X	r154	27.5
9BH	1	0	0	1	1	0	1	1	V155''	V12+(V11-V12) X	r155	27.5
9CH	1	0	0	1	1	1	0	0	V156''	V12+(V11-V12) X	r156	27.5
9DH	1	0	0	1	1	1	0	1	V157''	V12+(V11-V12) X	r157	27.5
9EH	1	0	0	1	1	1	1	0	V158''	V12+(V11-V12) X	r158	27.5
9FH	1	0	0	1	1	1	1	1	V159''	V12+(V11-V12) X	r159	27.5
A0H	1	0	1	0	0	0	0	0	V160''	V12+(V11-V12) X	r160	30.0
A1H	1	0	1	0	0	0	0	1	V161''	V12+(V11-V12) X	r161	30.0
A2H	1	0	1	0	0	0	1	0	V162''	V12+(V11-V12) X	r162	30.0
A3H	1	0	1	0	0	0	1	1	V163''	V12+(V11-V12) X	r163	30.0
A4H	1	0	1	0	0	1	0	0	V164''	V12+(V11-V12) X	r164	30.0
A5H	1	0	1	0	0	1	0	1	V165''	V12+(V11-V12) X	r165	30.0
A6H	1	0	1	0	0	1	1	0	V166''	V12+(V11-V12) X	r166	30.0
A7H	1	0	1	0	0	1	1	1	V167''	V12+(V11-V12) X	r167	30.0
A8H	1	0	1	0	1	0	0	0	V168''	V12+(V11-V12) X	r168	32.5
A9H	1	0	1	0	1	0	0	1	V169''	V12+(V11-V12) X	r169	32.5
AAH	1	0	1	0	1	0	1	0	V170''	V12+(V11-V12) X	r170	32.5
ABH	1	0	1	0	1	0	1	1	V171''	V12+(V11-V12) X	r171	32.5
ACH	1	0	1	0	1	1	0	0	V172''	V12+(V11-V12) X	r172	32.5
ADH	1	0	1	0	1	1	0	1	V173''	V12+(V11-V12) X	r173	32.5
AEH	1	0	1	0	1	1	1	0	V174''	V12+(V11-V12) X	r174	32.5
AFH	1	0	1	0	1	1	1	1	V175''	V12+(V11-V12) X	r175	32.5
BOH	1	0	1	1	0	0	0	0	V176''	V12+(V11-V12) X	r176	35.0
B1H	1	0	1	1	0	0	0	1	V177''	V12+(V11-V12) X	r177	35.0
B2H	1	0	1	1	0	0	1	0	V178''	V12+(V11-V12) X	r178	35.0
B3H	1	0	1	1	0	0	1	1	V179''	V12+(V11-V12) X	r179	35.0
B4H	1	0	1	1	0	1	0	0	V180''	V12+(V11-V12) X	r180	35.0
B5H	1	0	1	1	0	1	0	1	V181''	V12+(V11-V12) X	r181	35.0
B6H	1	0	1	1	0	1	1	0	V182''	V12+(V11-V12) X	r182	35.0
B7H	1	0	1	1	0	1	1	1	V183''	V12+(V11-V12) X	r183	35.0
B8H	1	0	1	1	1	0	0	0	V184''	V12+(V11-V12) X	r184	37.5
B9H	1	0	1	1	1	0	0	1	V185''	V12+(V11-V12) X	r185	37.5
BAH	1	0	1	1	1	0	1	0	V186''	V12+(V11-V12) X	r186	37.5
BBH	1	0	1	1	1	0	1	1	V187''	V12+(V11-V12) X	r187	37.5
BCH	1	0	1	1	1	1	0	0	V188''	V12+(V11-V12) X	r188	37.5
BDH	1	0	1	1	1	1	0	1	V189''	V12+(V11-V12) X	r189	37.5
BEH	1	0	1	1	1	1	1	0	V190''	V12+(V11-V12) X	r190	37.5
BFH	1	0	1	1	1	1	1	1	V191''	V12+(V11-V12) X	r191	37.5

Caution There is no connection between V7 and V8 in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage (4/4)

0.5 V_{DD2} - 0.3 V > V₈ > V₉ > V₁₀ > V₁₁ > V₁₂ > V₁₃ > V₁₄ > V₁₅ > V_{SS2} + 0.2 V, POL21/22 = L



Data	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Output voltage	
C0H	1	1	0	0	0	0	0	0	V192 ⁿ	V11
C1H	1	1	0	0	0	0	0	1	V193 ⁿ	V11+(V10-V11) X
C2H	1	1	0	0	0	0	1	0	V194 ⁿ	V11+(V10-V11) X
C3H	1	1	0	0	0	0	1	1	V195 ⁿ	V11+(V10-V11) X
C4H	1	1	0	0	0	1	0	0	V196 ⁿ	V11+(V10-V11) X
C5H	1	1	0	0	0	1	0	1	V197 ⁿ	V11+(V10-V11) X
C6H	1	1	0	0	0	1	1	0	V198 ⁿ	V11+(V10-V11) X
C7H	1	1	0	0	0	1	1	1	V199 ⁿ	V11+(V10-V11) X
C8H	1	1	0	0	1	0	0	0	V200 ⁿ	V11+(V10-V11) X
C9H	1	1	0	0	1	0	0	1	V201 ⁿ	V11+(V10-V11) X
CAH	1	1	0	0	1	0	1	0	V202 ⁿ	V11+(V10-V11) X
CBH	1	1	0	0	1	0	1	1	V203 ⁿ	V11+(V10-V11) X
CCH	1	1	0	0	1	1	0	0	V204 ⁿ	V11+(V10-V11) X
CDH	1	1	0	0	1	1	0	1	V205 ⁿ	V11+(V10-V11) X
CEH	1	1	0	0	1	1	1	0	V206 ⁿ	V11+(V10-V11) X
CFH	1	1	0	0	1	1	1	1	V207 ⁿ	V11+(V10-V11) X
D0H	1	1	0	1	0	0	0	0	V208 ⁿ	V11+(V10-V11) X
D1H	1	1	0	1	0	0	0	1	V209 ⁿ	V11+(V10-V11) X
D2H	1	1	0	1	0	0	1	0	V210 ⁿ	V11+(V10-V11) X
D3H	1	1	0	1	0	0	1	1	V211 ⁿ	V11+(V10-V11) X
D4H	1	1	0	1	0	1	0	0	V212 ⁿ	V11+(V10-V11) X
D5H	1	1	0	1	0	1	0	1	V213 ⁿ	V11+(V10-V11) X
D6H	1	1	0	1	0	1	1	0	V214 ⁿ	V11+(V10-V11) X
D7H	1	1	0	1	0	1	1	1	V215 ⁿ	V11+(V10-V11) X
D8H	1	1	0	1	1	0	0	0	V216 ⁿ	V11+(V10-V11) X
D9H	1	1	0	1	1	0	0	1	V217 ⁿ	V11+(V10-V11) X
DAH	1	1	0	1	1	0	1	0	V218 ⁿ	V11+(V10-V11) X
DBH	1	1	0	1	1	0	1	1	V219 ⁿ	V11+(V10-V11) X
DCH	1	1	0	1	1	1	0	0	V220 ⁿ	V11+(V10-V11) X
DDH	1	1	0	1	1	1	0	1	V221 ⁿ	V11+(V10-V11) X
DEH	1	1	0	1	1	1	1	0	V222 ⁿ	V11+(V10-V11) X
DFH	1	1	0	1	1	1	1	1	V223 ⁿ	V11+(V10-V11) X
E0H	1	1	1	0	0	0	0	0	V224 ⁿ	V10
E1H	1	1	1	0	0	0	0	1	V225 ⁿ	V10+(V9-V10) X
E2H	1	1	1	0	0	0	1	0	V226 ⁿ	V10+(V9-V10) X
E3H	1	1	1	0	0	0	1	1	V227 ⁿ	V10+(V9-V10) X
E4H	1	1	1	0	0	1	0	0	V228 ⁿ	V10+(V9-V10) X
E5H	1	1	1	0	0	1	0	1	V229 ⁿ	V10+(V9-V10) X
E6H	1	1	1	0	0	1	1	0	V230 ⁿ	V10+(V9-V10) X
E7H	1	1	1	0	0	1	1	1	V231 ⁿ	V10+(V9-V10) X
E8H	1	1	1	0	1	0	0	0	V232 ⁿ	V10+(V9-V10) X
E9H	1	1	1	0	1	0	0	1	V233 ⁿ	V10+(V9-V10) X
EAH	1	1	1	0	1	0	1	0	V234 ⁿ	V10+(V9-V10) X
EBH	1	1	1	0	1	0	1	1	V235 ⁿ	V10+(V9-V10) X
ECH	1	1	1	0	1	1	0	0	V236 ⁿ	V10+(V9-V10) X
EDH	1	1	1	0	1	1	0	1	V237 ⁿ	V10+(V9-V10) X
EEH	1	1	1	0	1	1	1	0	V238 ⁿ	V10+(V9-V10) X
EFH	1	1	1	0	1	1	1	1	V239 ⁿ	V10+(V9-V10) X
F0H	1	1	1	1	0	0	0	0	V240 ⁿ	V10+(V9-V10) X
F1H	1	1	1	1	0	0	0	1	V241 ⁿ	V10+(V9-V10) X
F2H	1	1	1	1	0	0	1	0	V242 ⁿ	V10+(V9-V10) X
F3H	1	1	1	1	0	0	1	1	V243 ⁿ	V10+(V9-V10) X
F4H	1	1	1	1	0	1	0	0	V244 ⁿ	V10+(V9-V10) X
F5H	1	1	1	1	0	1	0	1	V245 ⁿ	V10+(V9-V10) X
F6H	1	1	1	1	0	1	1	0	V246 ⁿ	V10+(V9-V10) X
F7H	1	1	1	1	0	1	1	1	V247 ⁿ	V10+(V9-V10) X
F8H	1	1	1	1	1	0	0	0	V248 ⁿ	V10+(V9-V10) X
F9H	1	1	1	1	1	0	0	1	V249 ⁿ	V10+(V9-V10) X
FAH	1	1	1	1	1	0	1	0	V250 ⁿ	V10+(V9-V10) X
FBH	1	1	1	1	1	0	1	1	V251 ⁿ	V10+(V9-V10) X
FCH	1	1	1	1	1	1	0	0	V252 ⁿ	V10+(V9-V10) X
FDH	1	1	1	1	1	1	0	1	V253 ⁿ	V10+(V9-V10) X
FEH	1	1	1	1	1	1	1	0	V254 ⁿ	V9
FFH	1	1	1	1	1	1	1	1	V255 ⁿ	V8

r	(Ω)
r192	42.5
r193	42.5
r194	42.5
r195	42.5
r196	42.5
r197	42.5
r198	42.5
r199	42.5
r200	47.5
r201	47.5
r202	47.5
r203	47.5
r204	47.5
r205	47.5
r206	47.5
r207	47.5
r208	52.5
r209	52.5
r210	52.5
r211	52.5
r212	52.5
r213	52.5
r214	52.5
r215	52.5
r216	57.5
r217	57.5
r218	57.5
r219	57.5
r220	57.5
r221	57.5
r222	57.5
r223	57.5
r224	57.5
r225	70.0
r226	70.0
r227	70.0
r228	82.5
r229	82.5
r230	82.5
r231	95.0
r232	95.0
r233	95.0
r234	112.5
r235	112.5
r236	112.5
r237	130.0
r238	130.0
r239	147.5
r240	147.5
r241	165.0
r242	165.0
r243	182.5
r244	182.5
r245	200.0
r246	200.0
r247	225.0
r248	225.0
r249	250.0
r250	250.0
r251	300.0
r252	300.0
r253	350.0
r254	350.0
TOTAL	15002.5

Caution There is no connection between V7 and V8 in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 8 bits x 2 RGBs (6 dots)

Input width : 48 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

(2) R,/L = L (Left shift)

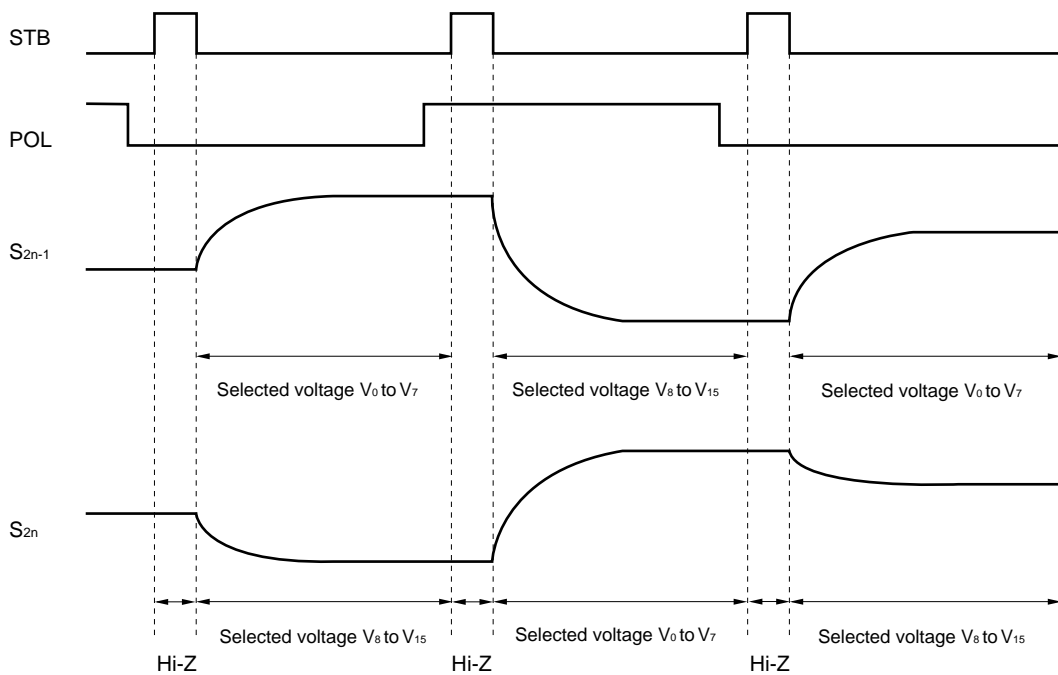
Output	S ₁	S ₂	S ₃	S ₄	...	S ₃₈₃	S ₃₈₄
Data	D ₀₀ to D ₀₇	D ₁₀ to D ₁₇	D ₂₀ to D ₂₇	D ₃₀ to D ₃₇	...	D ₄₀ to D ₄₇	D ₅₀ to D ₅₇

POL	S _{2n-1} ^{Note}	S _{2n} ^{Note}
L	V ₀ to V ₇	V ₈ to V ₁₅
H	V ₈ to V ₁₅	V ₀ to V ₇

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V _{DD1}	-0.5 to +4.0	V
Driver Part Supply Voltage	V _{DD2}	-0.5 to +10.0	V
Logic Part Input Voltage	V _{I1}	-0.5 to V _{DD1} + 0.5	V
Driver Part Input Voltage	V _{I2}	-0.5 to V _{DD2} + 0.5	V
Logic Part Output Voltage	V _{O1}	-0.5 to V _{DD1} + 0.5	V
Driver Part Output Voltage	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Operating Ambient Temperature	T _A	-10 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = -10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V _{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V _{DD2}	8.5	9.0	9.5	V
High-Level Input Voltage	V _{IH}	0.7 V _{DD1}		V _{DD1}	V
Low-Level Input Voltage	V _{IL}	0		0.3 V _{DD1}	V
γ-Corrected Voltage	V ₀ to V ₇	0.5 V _{DD2}		V _{DD2} - 0.2	V
	V ₈ to V ₁₅	V _{SS2} + 0.2		0.5 V _{DD2} - 0.3	V
Driver Part Output Voltage	V _O	V _{SS2} + 0.2		V _{DD2} - 0.2	V
Clock Frequency	f _{CLK}			40	MHz

Electrical Characteristics (T_A = -10 to +75°C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 9.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input Leak Current	I _{IL}			±0.1	±1.0	μA	
High-Level Output Voltage	V _{OH}	STHR (STHL), I _{OH} = 0 mA	V _{DD1} - 0.1		V _{DD1}	V	
Low-Level Output Voltage	V _{OL}	STHR (STHL), I _{OL} = 0 mA	0		0.1	V	
γ-Corrected Supply Current	I _γ	V ₀ to V ₇ = V ₈ to V ₁₅ = 4.0 V	V ₀ pin, V ₈ pin	225	450	900	μA
			V ₇ pin, V ₁₅ pin	-900	-450	-225	μA
Driver Output Current	I _{VOH}	V _X = 7.0 V, V _{OUT} = 6.5 V ^{Note}		-185	-90	μA	
	I _{VOL}	V _X = 1.0 V, V _{OUT} = 1.5 V ^{Note}	120	238		μA	
Output Voltage Deviation	ΔV _O	V _O = 0.2 V to 1.2 V		±30	±50	mV	
		V _O = V _{DD2} - 1.2 V to V _{DD2} - 0.2 V					
		V _O = 1.2 V to 0.5 V _{DD2} - 0.3 V		±10	±20	mV	
		V _O = 0.5 V _{DD2} to V _{DD2} - 1.2 V					
Output Swing Difference Deviation	ΔV _{P-P}	V _O = 0.2 V to 0.8 V		±20	±40	mV	
		V _O = V _{DD2} - 0.8 V to V _{DD2} - 0.2 V					
		V _O = 0.8 V to 1.2 V		±10	±20	mV	
		V _O = V _{DD2} - 1.2 V to V _{DD2} - 0.8 V					
		V _O = 1.2 V to 0.5 V _{DD2} - 0.3 V		±3	±10	mV	
		V _O = 0.5 V _{DD2} to V _{DD2} - 1.2 V					
Output Swing Average Difference Deviation	AV _O	V _{DD2} = 8.5 V, V ₀ = 7.9 V, V ₃ = 6.22 V, V ₇ = 4.0 V, V ₈ = 4.0 V, V ₁₂ = 1.78 V, V ₁₂ = 0.1 V, V ₁ , V ₂ , V ₄ , V ₅ , V ₆ , V ₉ , V ₁₀ , V ₁₁ , V ₁₃ , V ₁₄ : Open, T _A = 25°C, Input data: 80 H	4.433	4.440	4.447	V	
Output Voltage Range	V _O		0.2		V _{DD2} - 0.2	V	
Logic Part Dynamic Current Consumption	I _{DD1}	V _{DD1} , with no load		0.8	6.0	mA	
Driver Part Dynamic Current Consumption	I _{DD2}	V _{DD2} , with no load		4.5	11.0	mA	

Note V_X refers to the output voltage of analog output pins S₁ to S₃₈₄.

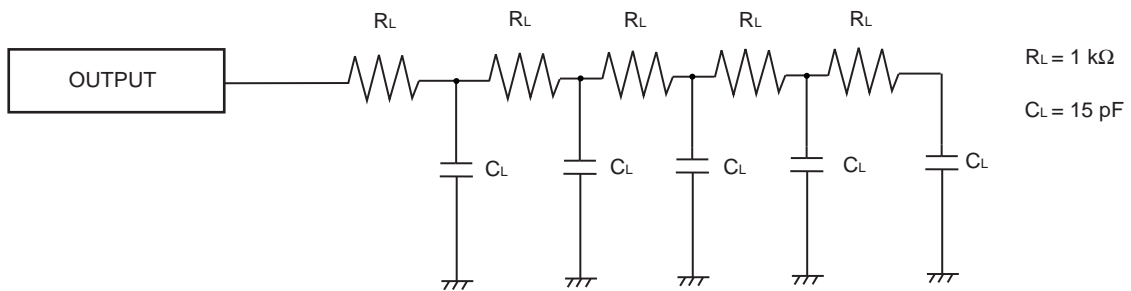
V_{OUT} refers to the voltage applied to analog output pins S₁ to S₃₈₄.

- Cautions**
1. The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz.
 2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
 3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DD2} = 9.0\text{ V} \pm 0.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	$C_L = 15\text{ pF}$		8	20	ns
Driver Output Delay Time	t_{PLH2}	$C_L = 75\text{ pF}$, $R_L = 5\text{ k}\Omega$		3	6	μs
	t_{PLH3}			4	8	μs
	t_{PHL2}			3	6	μs
	t_{PHL3}			4	8	μs
Input Capacitance	C_{i1}	STHR (STHL) excluded, $T_A = 25^\circ\text{C}$		4.8	10	pF
	C_{i2}	STHR (STHL), $T_A = 25^\circ\text{C}$		8.6	15	pF

<Measurement Condition>



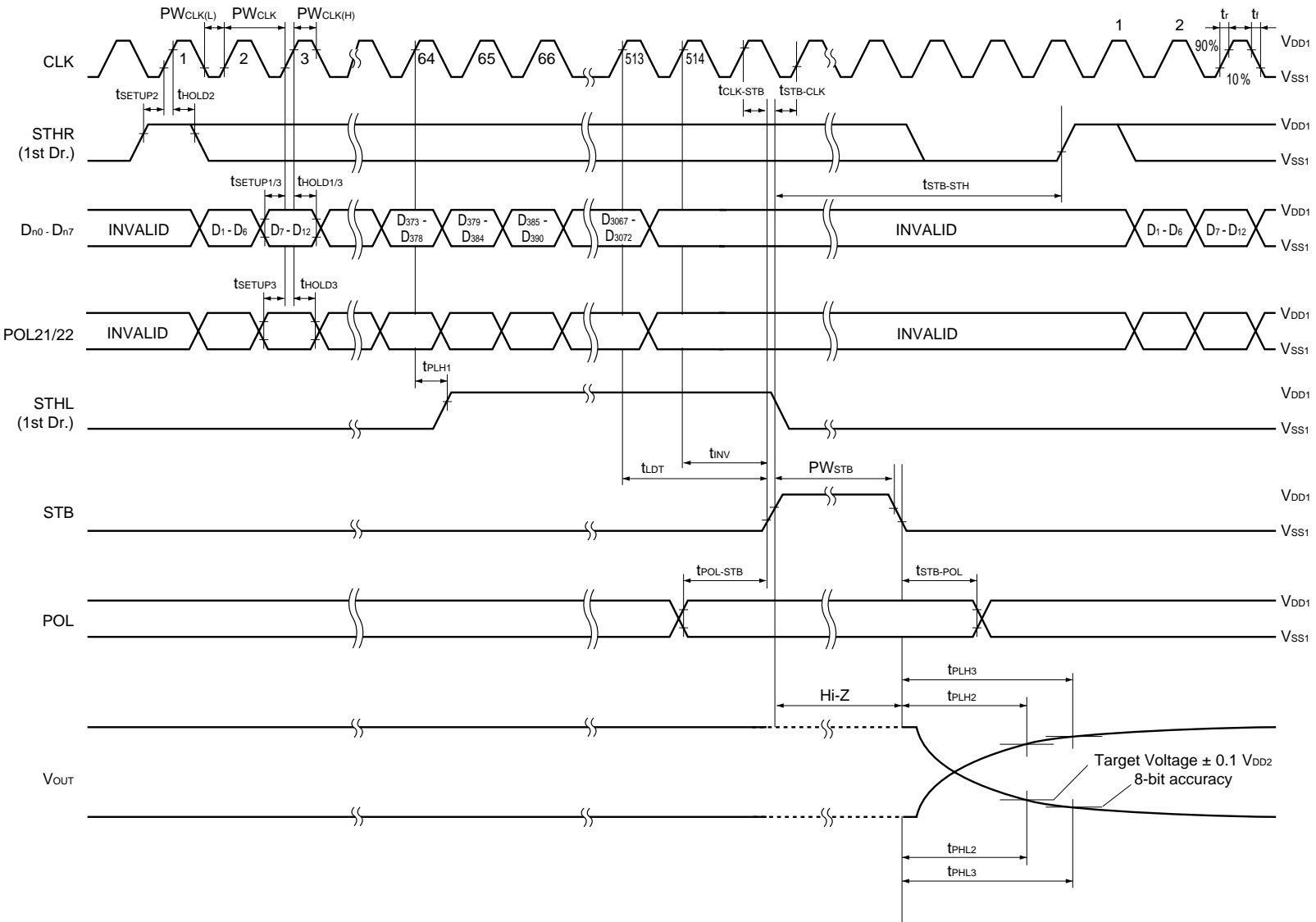
Timing Requirements ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS1} = 0\text{ V}$, $t_r = t_f = 8.0\text{ ns}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		25			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		2			ns
Data Hold Time	t_{HOLD1}		2			ns
Start Pulse Setup Time	t_{SETUP2}		2			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
★ POL21/22 Setup Time	t_{SETUP3}		2			ns
★ POL21/22 Hold Time	t_{HOLD3}		2			ns
Start Pulse Low Period	t_{SPL}		1			CLK
STB Pulse Width	PW_{STB}		2			μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK \uparrow \rightarrow STB \uparrow	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB \uparrow \rightarrow CLK \uparrow	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB \uparrow \rightarrow STHR(STHL) \uparrow	2			CLK
POL-STB Time	$t_{POL-STB}$	POL \uparrow or \downarrow \rightarrow STB \uparrow	-5			ns
STB-POL Time	$t_{STB-POL}$	STB \downarrow \rightarrow POL \downarrow or \uparrow	6			ns

Remark Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.

9. SWITCHING CHARACTERISTIC WAVEFORM (R,L=H)

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.



10. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μ PD16750.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μ PD16750N-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm ² : time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm ² : time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System(C10983E)****Quality Grades to NEC's Semiconductor Devices(C11531E)**

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 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
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