

FEATURES

Low Power Smallest Pin compatible Octal DACs

AD5668: 16 Bits

AD5648: 14 Bits

AD5628: 12 Bits

12-Bit Accuracy Guaranteed

14/16-Lead TSSOP Package

On-chip 1.25/2.5V, 10ppm/°C Reference

Power-Down to 200 nA @ 5V, 50 nA @ 3V

3V/5V Power Supply

Guaranteed Monotonic by Design

Power-On-Reset to Zero/Midscale

Three Power-Down Functions

Hardware /LDAC and /CLR functions

Rail-to-Rail Operation

Temperature Range -40°C to +125°C

APPLICATIONS

ProcessControl

Data Acquisition Systems

Portable Battery Powered Instruments

GENERAL DESCRIPTION

The AD5628/48/68 family of devices are low power, octal, 12-14-16-bit buffered voltage-out DACs. All devices operate from a single +2.7V to +5.5V, and are guaranteed monotonic by design.

The AD5628/48/68 have an on-chip reference with an internal gain of two. The AD56x8-1 has a 1.25V 10ppm/°C max reference and the AD56x8-2,-3 have a 2.5V 10ppm/°C max reference. The on-board reference is off at power-up allowing the use of an external reference. The internal reference is turned on by writing to the DAC. The part incorporates a power-on-reset circuit that ensures that the DAC output powers up to zero volts (AD56x8-1,-2/) or midscale (AD5668-3) and remains there until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 200nA at 5V and provides software selectable output loads while in power-down mode for any or all DACs channels.

Rev. PrA

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Digital Gain and Offset Adjustment

Programmable Voltage and Current Sources

Programmable Attenuators

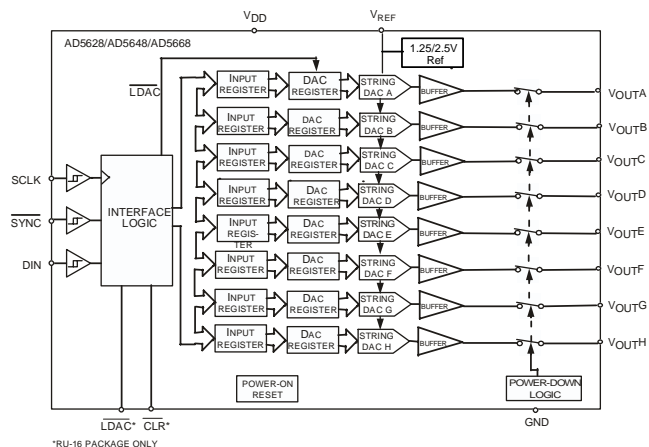


Figure 1. Functional Block Diagram

The outputs of all DACs may be updated simultaneously using the /LDAC function, with the added functionality of selecting through software any number of DAC channels to synchronize. There is also an asynchronous active low /CLR that clears all DACs to a software selectable code - 0 V, midscale or fullscale.

The AD5628/48/68 utilizes a versatile three-wire serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™ and DSP interface standards. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved.

PRODUCT HIGHLIGHTS

1. Octal 12/14/16-Bit DAC; 12-Bit Accuracy Guaranteed.
2. On-chip 1.25/2.5V, 10ppm/°C max Reference.
3. Available in 14/16-lead TSSOP package.
4. Power-On-Reset to Zero volts or Midscale.
5. Power-down capability. When powered down, the DAC typically consumes 50nA at 3V and 200nA at 5V.

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REVISION HISTORY

Revision 0: Initial Version

AD5628/AD5648/AD5668—SPECIFICATIONS

($V_{DD} = +4.5\text{ V to }+5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; External $REFIN = V_{DD}$; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Table 1.

Parameter	A Grade			B Grade			Unit	B Version ^{1,2} Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
STATIC PERFORMANCE ^{3,4}								
AD5628								
Resolution	12			12			Bits	
Relative Accuracy		± 0.5	± 6		± 0.5	± 1	LSB	See Figure 4
Differential Nonlinearity			± 1			± 1	LSB	Guaranteed Monotonic by Design. See Figure 5.
AD5648								
Resolution	14			14			Bits	
Relative Accuracy		± 2	± 8		± 2	± 4	LSB	See Figure 4
Differential Nonlinearity			± 1			± 1	LSB	Guaranteed Monotonic by Design. See Figure 5.
AD5668								
Resolution	16			16			Bits	
Relative Accuracy			± 32			± 16	LSB	See Figure 4
Differential Nonlinearity			± 1			± 1	LSB	Guaranteed Monotonic by Design. See Figure 5.
Load Regulation			2			2	LSB/mA	$V_{DD} = V_{ref} = 5\text{ V}$, Midscale $I_{out} = 0\text{ mA}$ to 15 mA sourcing/sinking
Zero Code Error		+1	+9		+1	+9	mV	All Zeroes Loaded to DAC Register. See Figure 8.
Zero Code Error Drift ³		± 20			± 20		$\mu\text{V}/^\circ\text{C}$	
Full-Scale Error		-0.15	-1.25		-0.15	-1.25	% of FSR	All Ones Loaded to DAC Register. See Figure 8.
Gain Error			± 1.5			± 1.5	% of FSR	
Gain Temperature Coefficient		± 5			± 5		ppm	of FSR/ $^\circ\text{C}$
Offset Error		± 1	± 9		± 1	± 9	mV	
Offset Temperature Coefficient		1.7			1.7		$\mu\text{V}/^\circ\text{C}$	
DC Power Supply Rejection Ratio ⁶		-80			-80		dB	$V_{DD} \pm 10\%$
DC Crosstalk ⁶ (Ext Ref)								
		10			10		μV	$R_L = 2\text{ k}\Omega$ to GND or V_{DD}
		4.5			4.5		$\mu\text{V}/\text{mA}$	Due to Load current change
		10			10		μV	Due to Powering Down (per channel)
DC Crosstalk ⁶ (Int Ref)								
		20			20		μV	$R_L = 2\text{ k}\Omega$ to GND or V_{DD}
		4.5			4.5		$\mu\text{V}/\text{mA}$	Due to Load current change
		20			20		μV	Due to Powering Down (per channel)

¹ Temperature ranges are as follows: B Version: -40°C to $+125^\circ\text{C}$, typical at 25°C .

² Linearity calculated using a reduced code range of 485 to 64714. Output unloaded.

³ DC specifications tested with the outputs unloaded unless stated otherwise.

⁴ Linearity is tested using a reduced code range: AD5628 (Code 48 to Code 4047), AD5648 (Code / to Code /), and AD5668 (Code 485 to 64714).

⁶ Guaranteed by design and characterization; not production tested.

⁸ Interface inactive. All DACs active. DAC outputs unloaded.

⁹ All eight DACs powered down.

Specifications subject to change without notice.

Parameter	A Grade			B Grade			Unit	B Version ^{1,2} Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
OUTPUT CHARACTERISTICS ⁶								
Output Voltage Range	0		V _{DD}	0		V _{DD}	V	
Capacitive Load Stability		2			2		pF	R _L =∞
		10			10		pF	R _L =2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short Circuit Current		30			30		mA	V _{DD} =+5V
Power-Up Time		4			4		μs	Coming out of Power-Down Mode. V _{DD} =+5V
REFERENCE INPUTS ³								
Reference Input voltage		V _{DD}			V _{DD}		V	±1% for specified performance
Reference Current		35	45		35	45	μA	V _{REF} = V _{DD} = +5.5V (per DAC channel)
Reference Input Range	0		V _{DD}	0		V _{DD}		
Reference Input Impedance		14.6			14.6		kΩ	Per DAC channel
REFERENCE OUTPUT								
Output Voltage	2.495	2.5	2.505	2.495	2.5	2.505	V	
AD5628/AD5648/AD5668x-2/3 Reference TC			±10			±10	ppm/°C	
Reference Output Impedance		2			2		kΩ	
LOGIC INPUTS ³								
Input Current			±1			±1	μA	
V _{INL} , Input Low Voltage			0.8			0.8	V	V _{DD} =+5 V
V _{INH} , Input High Voltage	2			2			V	V _{DD} =+5 V
Pin Capacitance		3			3		pF	
POWER REQUIREMENTS								
V _{DD}	4.5		5.5	4.5		5.5	V	All Digital Inputs at 0 or V _{DD}
I _{DD} (Normal Mode) ⁸ V _{DD} =4.5 V to +5.5 V		2	4		2	4	mA	DAC Active and Excluding Load Current V _{IH} =V _{DD} and V _{IL} =GND
I _{DD} (All Power-Down Modes) ⁹ V _{DD} =4.5 V to +5.5 V		0.2	1		0.2	1	μA	V _{IH} =V _{DD} and V _{IL} =GND
POWER EFFICIENCY								
I _{OUT} /I _{DD}		89			89		%	I _{LOAD} =2 mA, V _{DD} =+5 V

AC CHARACTERISTICS¹

($V_{DD} = +4.5\text{ V to }+5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; External $REFIN = V_{DD}$; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter ²	Min	Typ	Max	Unit	B Version ¹ Conditions/Comments
Output Voltage Settling Time					
AD5628		6	8	μs	1/4 to 3/4 scale settling to $\pm 2\text{LSB}$
AD5648		7	9	μs	1/4 to 3/4 scale settling to $\pm 2\text{LSB}$
AD5668		8	10	μs	1/4 to 3/4 scale settling to $\pm 2\text{LSB}$
Settling Time for 1LSB Step					
Slew Rate		1.5		$\text{V}/\mu\text{s}$	
Digital-to-Analog Glitch Impulse		5		$\text{nV}\cdot\text{s}$	1 LSB Change Around Major Carry. See Figure 21.
Channel –to–Channel Isolation		100		dB	
Digital Feedthrough		0.1		$\text{nV}\cdot\text{s}$	
Digital Crosstalk		0.5		$\text{nV}\cdot\text{s}$	
Analog Crosstalk		1		$\text{nV}\cdot\text{s}$	
DAC-to-DAC Crosstalk		3		$\text{nV}\cdot\text{s}$	
Multiplying Bandwidth		200		kHz	$V_{REF} = 2\text{V} \pm 0.1\text{ V p-p}$.
Total Harmonic Distortion		-80		dB	$V_{REF} = 2\text{V} \pm 0.1\text{ V p-p}$. Frequency = 10kHz
Output Noise Spectral Density		120		$\text{nV}/\sqrt{\text{Hz}}$	DAC code=8400 _H , 1kHz
		100		$\text{nV}/\sqrt{\text{Hz}}$	DAC code=8400 _H , 10kHz
Output Noise		15		$\mu\text{Vp-p}$	0.1Hz to 10Hz;

NOTES

¹Guaranteed by design and characterization; not production tested.

²See the Terminology section.

³Temperature range (Y Version): -40°C to $+125^\circ\text{C}$; typical at $+25^\circ\text{C}$.
Specifications subject to change without notice.

AD5628/AD5648/AD5668—SPECIFICATIONS

($V_{DD} = +2.7\text{ V to }+3.6\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; External $REFIN = V_{DD}$; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Table 2.

Parameter	A Grade			B Grade			Unit	B Version ^{1,1} Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
STATIC PERFORMANCE ^{3,4}								
AD5628								
Resolution	12			12			Bits	
Relative Accuracy		± 0.5	± 6		± 0.5	± 1	LSB	See Figure 4
Differential Nonlinearity			± 1			± 1	LSB	Guaranteed Monotonic by Design. See Figure 5.
AD5648								
Resolution	14			14			Bits	
Relative Accuracy		± 2	± 8		± 2	± 4	LSB	See Figure 4
Differential Nonlinearity			± 1			± 1	LSB	Guaranteed Monotonic by Design. See Figure 5.
AD5668								
Resolution	16			16			Bits	
Relative Accuracy			± 32			± 16	LSB	See Figure 4
Differential Nonlinearity			± 1			± 1	LSB	Guaranteed Monotonic by Design. See Figure 5.
Load Regulation			4			4	LSB/mA	$V_{DD} = V_{ref} = 3\text{V}$, Midscale $I_{out} = 0\text{mA to }7.5\text{mA}$ sourcing/sinking
Zero Code Error		+1	+9		+1	+9	mV	All Zeroes Loaded to DAC Register. See Figure 8.
Zero Code Error Drift ¹		± 20			± 20		$\mu\text{V}/^\circ\text{C}$	
Full-Scale Error		-0.15	-1.25		-0.15	-1.25	% of FSR	All Ones Loaded to DAC Register. See Figure 8.
Gain Error			± 0.7			± 0.7	% of FSR	
Gain Temperature Coefficient		± 5			± 5		ppm	of FSR/ $^\circ\text{C}$
Offset Error		± 1	± 9		± 1	± 9	mV	
Offset Temperature Coefficient		1.7			1.7		$\mu\text{V}/^\circ\text{C}$	
DC Power Supply Rejection Ratio ⁶		-80			-80		dB	$V_{DD} \pm 10\%$
DC Crosstalk ⁶ (Ext Ref)		10			10		μV	$R_L = 2\text{ k}\Omega$ to GND or V_{DD}
		4.5			4.5		$\mu\text{V}/\text{mA}$	Due to Load current change
		10			10		μV	Due to Powering Down (per channel)
DC Crosstalk ⁶ (Int Ref)		20			20		μV	$R_L = 2\text{ k}\Omega$ to GND or V_{DD}
		4.5			4.5		$\mu\text{V}/\text{mA}$	Due to Load current change
		20			20		μV	Due to Powering Down (per channel)
OUTPUT CHARACTERISTICS ⁶								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		pF	$R_L = \infty$

DC Output Impedance	10			10			pF	$R_L=2\text{ k}\Omega$
Short Circuit Current	0.5			0.5			Ω	
Power-Up Time	30			30			mA	$V_{DD}=+3\text{V}$
	5			5			μs	Coming Out of Power-Down Mode. $V_{DD}=+3\text{V}$
REFERENCE INPUTS ³								
Reference Input voltage	V_{DD}			V_{DD}			V	$\pm 1\%$ for specified performance
Reference Current	20	20		20	20		μA	$V_{REF} = V_{DD} = +3.6\text{V}$ (per DAC channel)
Reference Input Range	0		V_{DD}	0		V_{DD}		
Reference Input Impedance	14.6			14.6			$\text{k}\Omega$	Per DAC channel
REFERENCE OUTPUT								
Output Voltage	1.248	1.25	1.252	1.248	1.25	1.252	V	
AD5628/AD5648/AD5668x-1								
Reference TC			± 10			± 10	ppm/ $^{\circ}\text{C}$	
Reference Output Impedance	2			2			$\text{k}\Omega$	
LOGIC INPUTS ³								
Input Current			± 1			± 1	μA	
V_{INL} , Input Low Voltage			0.8			0.8	V	$V_{DD}=+3\text{V}$
V_{INH} , Input High Voltage	2			2			V	$V_{DD}=+3\text{V}$
Pin Capacitance	3			3			pF	
POWER REQUIREMENTS								
V_{DD}	2.7		3.6	2.7		3.6	V	All Digital Inputs at 0 or V_{DD}
I_{DD} (Normal Mode) ⁸								DAC Active and Excluding Load Current
$V_{DD}=2.7\text{V}$ to $+3.6\text{V}$		2	4		2	4	mA	$V_{IH}=V_{DD}$ and $V_{IL}=\text{GND}$
I_{DD} (All Power-Down Modes) ⁹								
$V_{DD}=2.7\text{V}$ to $+3.6\text{V}$		0.2	1		0.2	1	μA	$V_{IH}=V_{DD}$ and $V_{IL}=\text{GND}$
POWER EFFICIENCY								
I_{OUT}/I_{DD}	89			89			%	$I_{LOAD}=2\text{ mA}$, $V_{DD}=+5\text{V}$

AC CHARACTERISTICS¹

($V_{DD} = +2.7\text{V}$ to $+3.6\text{V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; External $REFIN = V_{DD}$; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter ²	Min	Typ	Max	Unit	B Version ¹ Conditions/Comments
Output Voltage Settling Time					
AD5628		6	8	μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to $\pm 2\text{LSB}$
AD5648		7	9	μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to $\pm 2\text{LSB}$
AD5668		8	10	μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to $\pm 2\text{LSB}$
Settling Time for 1LSB Step					
Slew Rate		1.5		V/ μs	
Digital-to-Analog Glitch Impulse		10		nV-s	
Channel -to-Channel Isolation		100		dB	
Digital Feedthrough		0.5		nV-s	1 LSB Change Around Major Carry. See Figure 21.

Digital Crosstalk	0.5	nV-s	
Analog Crosstalk	1	nV-s	
DAC-to-DAC Crosstalk	3	nV-s	
Multiplying Bandwidth	200	kHz	VREF = 2V ± 0.1 V p-p.
Total Harmonic Distortion	-80	dB	VREF = 2V ± 0.1 V p-p. Frequency = 10kHz
Output Noise Spectral Density	120	nV/√Hz	DAC code=8400 _H , 1kHz
	100	nV/√Hz	DAC code=8400 _H , 10kHz
Output Noise	15	μVp-p	0.1Hz to 10Hz;

NOTES

¹Guaranteed by design and characterization; not production tested.

²See the Terminology section.

³Temperature range (Y Version): -40°C to +125°C; typical at +25°C.

Specifications subject to change without notice.

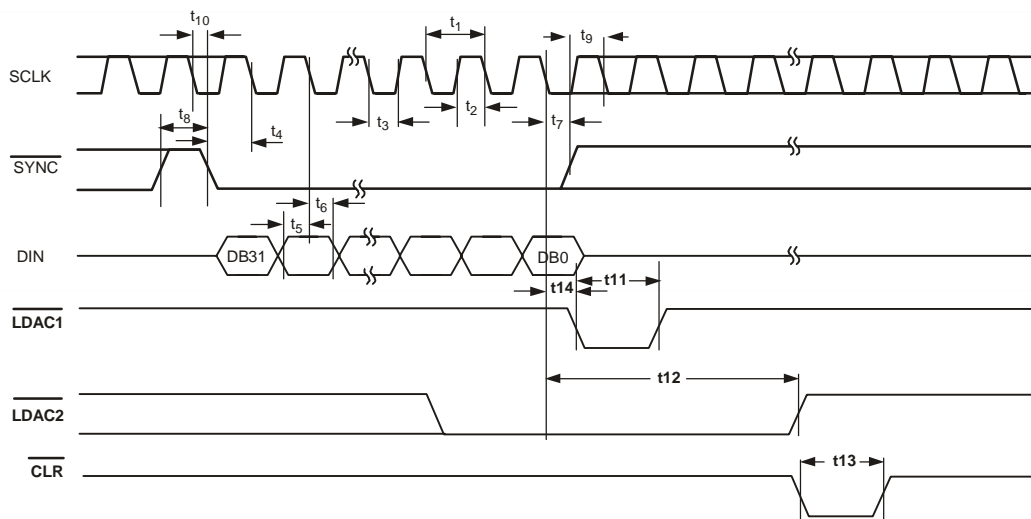
TIMING CHARACTERISTICS

All input signals are specified with $t_r = t_f = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

See Figure 2.

($V_{DD} = +2.7 \text{ V}$ to $+5.5 \text{ V}$; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Conditions/Comments
	$V_{DD} = 2.7 \text{ V}$ to 3.6 V	$V_{DD} = 3.6 \text{ V}$ to 5.5 V		
t_1 ¹	20	20	ns min	SCLK Cycle Time
t_2	11	9	ns min	SCLK High Time
t_3	9	9	ns min	SCLK Low Time
t_4	13	13	ns min	$\overline{\text{SYNC}}$ to SCLK Falling Edge Setup Time
t_5	4	4	ns min	Data Setup Time
t_6	4	4	ns min	Data Hold Time
t_7	0	0	ns min	SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge
t_8	25	20	ns min	Minimum $\overline{\text{SYNC}}$ High Time
t_9	13	13	ns min	$\overline{\text{SYNC}}$ Rising Edge to SCLK Fall Ignore
t_{10}	0	0	ns min	SCLK Falling Edge to $\overline{\text{SYNC}}$ Fall Ignore
t_{11}	20	20	ns min	LDAC Pulsewidth Low
t_{12}	20	20	ns min	SCLK Falling Edge to LDAC Rising Edge
t_{13}	20	20	ns min	/CLR Pulse Width Low
t_{14}	0	0	ns min	SCLK Falling Edge to LDAC Falling Edge
t_{15}	tbd	tbd	ns min	/CLR Pulse Activation Time (AD5380?)



NOTES
 1. ASYNCHRONOUS LDAC UPDATE MODE.
 2. SYNCHRONOUS LDAC UPDATE MODE.

Figure 2. Serial Write Operation

¹ Maximum SCLK frequency is 50 MHz at $V_{DD} = +2.7 \text{ V}$ to $+5.5 \text{ V}$

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

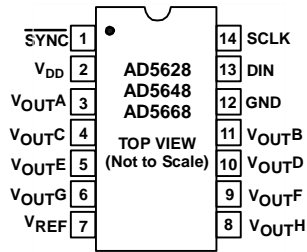


Figure 3. 14-Lead TSSOP (RU-14)

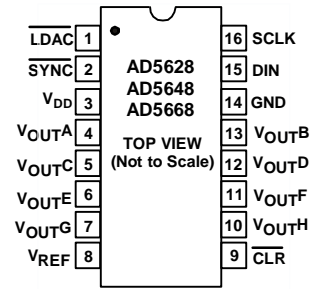


Figure 4. 16-Lead TSSOP (RU-16)

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	/LDAC	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	/SYNC	Active Low-Control Input. This is the frame synchronization signal for the input data. When SYNC goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following 32 clocks. If SYNC is taken high before the 32nd falling edge, the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the device.
3	VDD	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 μ F capacitor in parallel with a 0.1 μ F capacitor to GND.
4	VOUTA	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
13	VOUTB	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
5	VOUTC	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
12	VOUTD	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
8	VREF	Reference Input/Output Pin
9	/CLR	Active Low Control Input that Loads Software selectable code – Zero, midscale, fullscale - to All Input and DAC Registers. Therefore, the outputs also go to selected code. Default clears the output to 0V.
6	VOUTE	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
11	VOUTF	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
7	VOUTG	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
10	VOUTH	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
14	GND	Ground Reference Point for All Circuitry on the Part.
15	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

($T_A = +25^\circ\text{C}$ unless otherwise noted)

Parameter	Rating
V_{DD} to GND	-0.3 V to +7 V
Digital Input Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V

V_{OUT} to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range Industrial (B Version)	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T_J Max)	+150°C
TSSOP Package	
Power Dissipation	$(T_J \text{ Max} - T_A) / \theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 2.

Differential Nonlinearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 3.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5668 with Code ??? loaded into the DAC register.

This is a measure of the offset error of the DAC and the output amplifier (see Figures 2 and 3). It can be negative or positive, and is expressed in mV.

Zero-Code Error

Zero-code error is a measure of the output error when zero code

(0000Hex) is loaded to the DAC register. Ideally the output should be 0 V. The zero-code error is always positive in the AD56x8 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 6.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/ $^\circ\text{C}$.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFFF Hex) is loaded to the DAC register. Ideally the output should be $V_{DD} - 1$ LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 6.

Total Unadjusted Error

Total Unadjusted Error (TUE) is a measure of the output error

taking the various offset and gain errors into account. A typical TUE vs. code plot can be seen in Figure 4.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FFF Hex to 8000 Hex). See Figure 19.

DC Power Supply Rejection Ratio (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied $\pm 10\%$.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC kept at midscale. It is expressed in μV .

Reference Feedthrough

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $LDAC$ is high). It is expressed in dB.

Channel-to-Channel Isolation

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

Major-Code Transition Glitch Energy

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the

analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($SYNC$ held high). It is specified in nV-s and is measured with a fullscale change on the digital input pins, i.e., from all 0s to all 1s and vice versa.

Digital Crosstalk

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $LDAC$ high. Then pulse $LDAC$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $LDAC$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in dB.

AD5628/AD5648/AD5668—TYPICAL PERFORMANCE CHARACTERISTICS



Figure 2. Typical INL Plot

Figure 4. Typical INL Plot



Figure 5. INL Error and DNL Error vs. Temperature

Figure 7. INL Error and DNL Error vs. Temperature



Figure 3. Typical DNL Plot

Figure 5. Typical DNL Plot



Figure 6. Zero-Scale Error and Full-Scale Error vs. Temperature

Figure 8. Zero-Scale Error and Full-Scale Error vs. Temperature



Figure 4. Typical Total Unadjusted Error Plot

Figure 6. Typical Total Unadjusted Error Plot

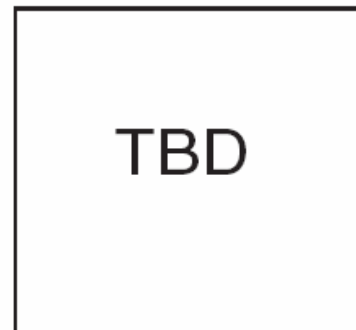


Figure 7. I_{DD} Histogram with $V_{DD}=3V$ and $V_{DD}=5V$

Figure 9. I_{DD} Histogram with $V_{DD}=3V$ and $V_{DD}=5V$



Figure 8. Source and Sink Current Capability with $V_{DD} = 3\text{ V}$

Figure 10. Source and Sink Current Capability with $V_{DD}=3\text{V}$

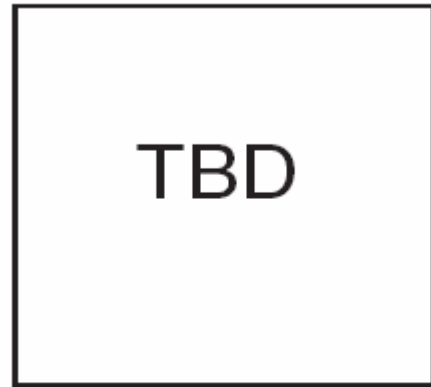


Figure 11. Supply Current vs. Temperature

Figure 13. Supply Current vs. Temperature



Figure 9. Source and Sink Current Capability with $V_{DD} = 5\text{ V}$

Figure 11. Source and Sink Current Capability with $V_{DD}=5\text{ V}$

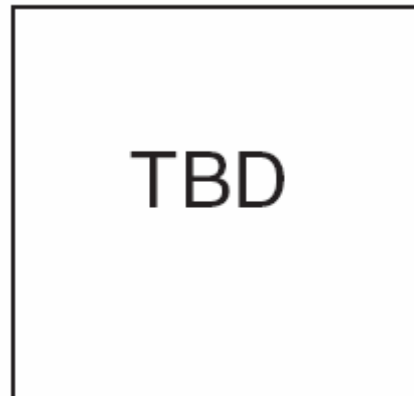


Figure 12. Supply Current vs. Supply Voltage

Figure 14. Supply Current vs. Supply Voltage



Figure 10. Supply Current vs. Code

Figure 12. Supply Current vs. Code

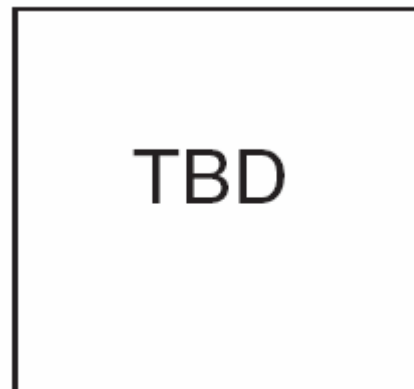


Figure 13. Power-Down Current vs. Supply Voltage

Figure 15. Power-Down Current vs. Supply Voltage



Figure 14. Supply Current vs. Logic Input Voltage

Figure 16. Supply Current vs. Logic Input Voltage



Figure 15. Full-Scale Settling Time

Figure 17. Full-Scale Settling Time



Figure 16. Half-Scale Settling Time

Figure 18. Half-Scale Settling Time



Figure 17. Power-On Reset to 0 V

Figure 19. Power-On Reset to 0V



Figure 18. Exiting Power-Down (800 Hex Loaded)

Figure 20. Exiting Power-Down (800 Hex Loaded)



Figure 19. Digital-to-Analog Glitch Impulse

Figure 21. Digital-to-Analog Glitch Impulse

GENERAL DESCRIPTION

D/A Section

The AD5628/AD5648/AD5668 DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. The parts include an internal 1.25/2.5V, 10ppm/°C reference with an internal gain of two. Figure 22 shows a block diagram of the DAC architecture.

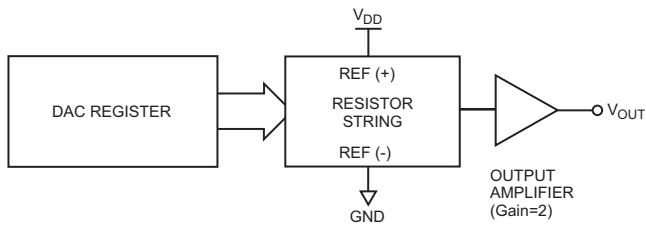


Figure 22. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{ref}(ext) \times \left(\frac{D}{2^N} \right)$$

$$V_{OUT} = 2 * V_{ref}(int) \times \left(\frac{D}{2^N} \right)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register;

0 - 4095 for AD5628 (12 bit)

0 - 16383 for AD5648 (14 bit)

0 - 65535 for AD5668 (16 bit)

N = the DAC resolution

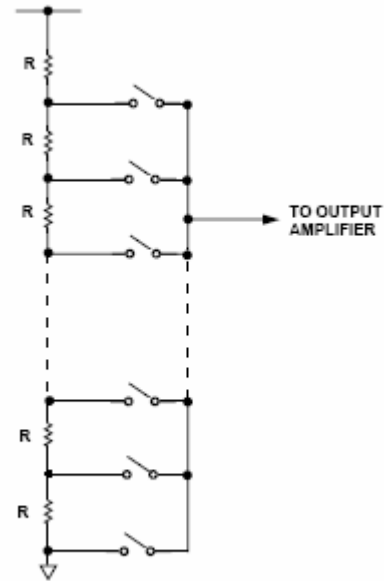


Figure 21. Resistor String

Figure 23. Resistor String

Resistor String

The resistor string section is shown in Figure 23. It is simply a string of resistors, each of value R . The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to V_{DD} . It is capable of driving a load of 2 k Ω in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 10 and Figure 11. The slew rate is 1.5 V/ μ s with a half-scale settling time of 8 μ s with the output unloaded.

SERIAL INTERFACE

The AD5628/AD5648/AD5668 has a three-wire serial interface ($\overline{\text{SYNC}}$, SCLK and DIN), which is compatible with SPI, QSPI and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5628/AD5648/AD5668 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed

(i.e., a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{\text{SYNC}}$ line may be kept low or be brought high. In either case, it must be brought high for a minimum of 50 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Since the $\overline{\text{SYNC}}$ buffer draws more current when $V_{\text{IN}} = 2\text{V}$ than it does when $V_{\text{IN}} = 0.8\text{V}$, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned above, however, it must be brought high again just before the next write sequence.

Input Shift Register

The input shift register is 32 bits wide (see Figure 24). The first four bits are “don’t cares.” The next four bits are the Command bits C3-C0, (see Table 1) followed by the 4-bit DAC address A3-A0, (see Table 2) and finally the 16/14/12-bit data word. The data word comprises the 16- 14- 12- bit input code followed by 4, 6 or 8 don’t care bits, the AD5668, AD5648 and AD5628 respectively. See figure 24, 25, 26. These data bits are transferred to the DAC register on the 32nd falling edge of SCLK.

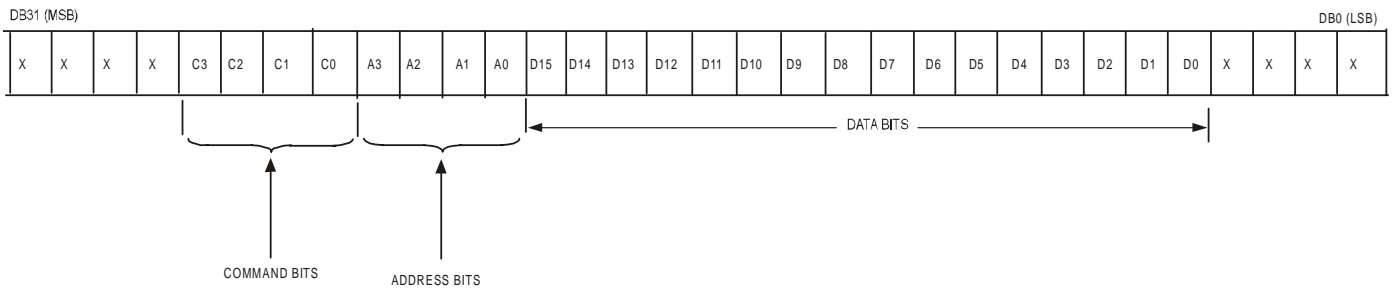


Figure 24 AD5668. Input Register Contents

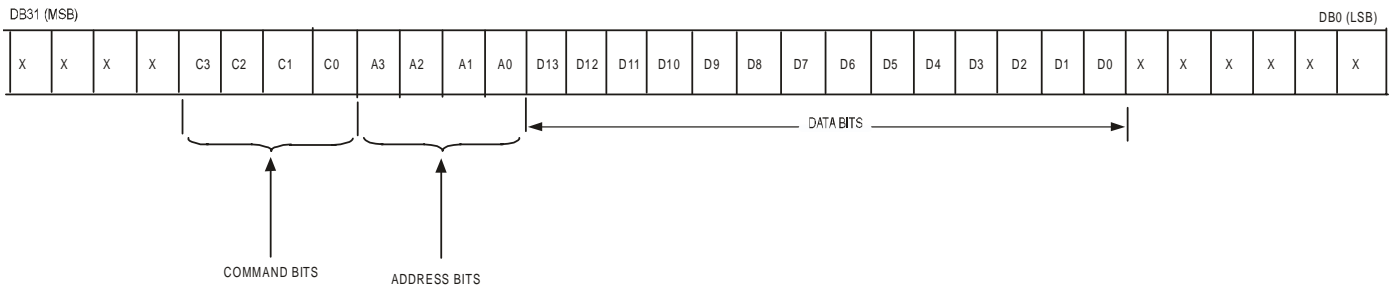


Figure 25. AD5648. Input Register Contents

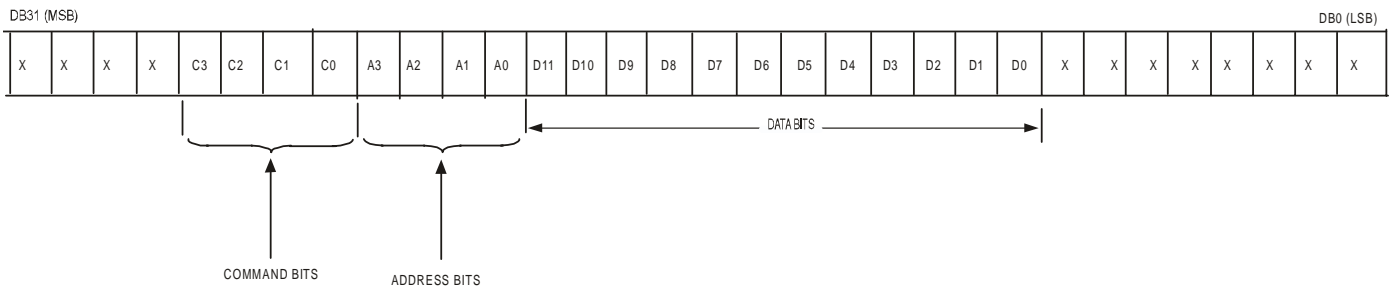


Figure 26. AD5628 Input Register Contents

Command				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, Update All
0	0	1	1	Write to and Update DAC channel n
0	1	0	0	Power Down DAC (Power-up)
0	1	0	1	Load Clear Code Register
0	1	1	0	Load LDAC Register (LDAC overwrite)
0	1	1	1	Reset (Power-on-Reset)
1	0	0	0	REF Setup Register
1	0	0	1	Reserved
*	*	*	*	Reserved
1	1	1	1	Reserved

ADDRESS (n)				
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

Table 1. Command Definition

Table 2. Address Command

SYNC Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for 32 falling edges of SCLK and the DAC is updated on the 32nd falling edge and rising edge of SYNC. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs—see Figure 27.

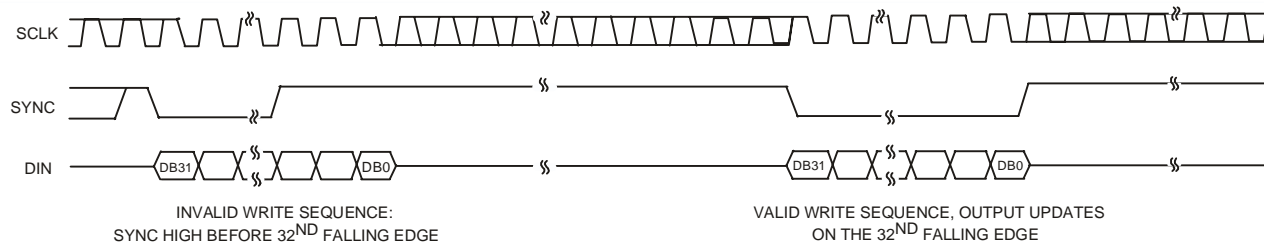


Figure 27. SYNC Interrupt Facility

Reference Setup –External to Internal

The on-board reference is turned off at power-up by default. This allows the use of an external reference. The AD5628/48/68 have an on-chip reference with an internal gain of two. The AD56x8-1 has a 1.25V 10ppm/°C max reference and the AD56x8-2,-3 have a 2.5V 10ppm/°C max reference. The on-board reference can be turned on/off through a software executable REF Setup function, see Table 3. Command 1000 is reserved for this REF Setup function, see Table 1. The reference mode is software-programmable by setting a bit (DB0) in the REF Setup register.

Table 4 shows how the state of the bits corresponds to the mode of operation of the device.

REF Setup Register (DB0)	Action
0	Ref Off (Default)
1	Ref On

Table 3. Reference Set-up Register

MSB										LSB
DB31 – DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB1-DB19	DB0
x	1	0	0	0	x	x	x	x	x	1/0
<i>Don't Cares</i>	<i>COMMAND BITS (C3-C0)</i>				<i>ADDRESS BITS (A3 – A0)</i>				<i>Don't Cares</i>	REF Setup Register

Table 4 32-Bit Input Shift Register Contents for Reference Setup Function

Power-On-Reset

The AD5628/AD5648/AD5668 family contains a power-on-reset circuit that controls the output voltage during power-up. The AD5628/AD5648/AD5668x-1/2 DAC output powers up to zero volts and the AD5668-3 DAC output powers up to midscale. The output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

There is also a software executable Reset function that will reset the DAC to the Power-on -Reset code. Command 0111 is reserved for this Reset function, see Table 1.

Power-Down Modes

The AD5628/AD5648/AD5668 contains four separate modes of operation. Command 0100 is reserved for the Power-Down function, see Table 1. These modes are software-programmable by setting two bits (DB9 and DB8) in the control register.

Table 5 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs, (DacH to DacA) may be powered down to the selected mode by setting the corresponding 8 bits (DB7 to DB0) to a “1”. See Table 6 for contents of the Input Shift Register during power down/up operation.

When both bits are set to 0, the part works normally with its normal power consumption of 250 µA at 5 V. However, for the three power-

down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or it is left open-circuited (Tri-State). The output stage is illustrated in figure 24.

The bias generator of selected DAC(s), the output amplifier, the resistor string and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically (2.5 μs for V_{DD} = 5 V and 5 μs for V_{DD} = 3 V). See Figure 20 for a plot.

Any combination of DACs can be powered up by setting PD1 and PD0 to “0” (normal operation). Output powers-up to value in input register (/LDAC Low) or to value in DAC register before Power-Down (/LDAC High).

DB9	DB8	Operating Mode
0	0	Normal Operation Power Down Modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Tri State

Table 5. Modes of Operation for the AD5628/AD5648/AD5668

MSB																			LSB	
DB31 – DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB10—DB19	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
x	0	1	0	0	x	x	x	x	x	PD1	PD0	DacH	DacG	DacF	DacE	DacD	DacC	DacB	DacA	
Don't Cares	COMMAND BITS (C2-C0)				ADDRESS BITS (A3 – A0) Don't cares				Don't Cares	Power Down Mode	Power Down/Up Channel Selection – Set Bit to a “1” to select									

Table 6. 32-Bit Input Shift Register Contents for Power Down/Up Function

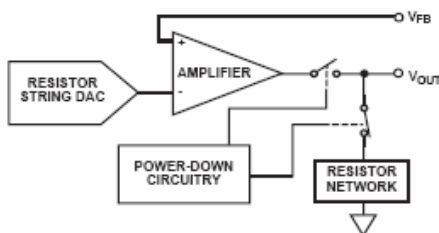


Figure 24. Output Stage During Power-Down

Clear Code Register

The AD5628/AD5648/AD5668 gives the option of clearing any one or all DAC channels to 0, midscale or fullscale code. Command 0101 is reserved for the Clear Code function. See Table1. These clear code values are software-programmable by setting two bits (DB1 and DB0) in the control register.

Table shows how the state of the bits corresponds to the clear code values of the device. Upon execution of the hardware /CLR pin (active LOW), the DAC output is cleared to the clear code register value (default setting is zero). See Table 8 for contents of the Input Shift Register during the Clear Code Register operation. The part will exit Clear code mode on the 32nd falling edge of the next write to the part.

Clear Code Register		
CR1	CR0	Clears to code
0	0	0000h
0	1	8000h
1	0	FFFFh
1	1	No operation

Table 7. Clear Code Register

MSB											LSB
DB31 – DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB2-DB19	DB1	DB0
X	0	1	0	1	1/0	1/0	1/0	1/0	x	1/0	1/0
Don't Cares	COMMAND BITS (C2-C0)				ADDRESS BITS (A3 – A0)				Don't Cares	Clear Code Register (CR1-CR0)	

Table 8. 32-Bit Input Shift Register Contents Clear Code Function

LDAC Function

The outputs of all DACs may be updated simultaneously using the hardware /LDAC pin.

Synchronous LDAC: The DAC registers are updated after new data is read in on the falling edge of the 32nd SCLK pulse. LDAC can be permanently low or pulsed as in Figure 1.

Asynchronous LDAC: The outputs are not updated at the same time that the input registers are written to. When LDAC goes low, the DAC registers are updated with the contents of the input register.

The outputs of all DACs may be updated simultaneously using the /LDAC function, with the added functionality of selecting through software any number of DAC channels to synchronize.

Writing to the DAC using command 0110, the hardware /LDAC pin can be overwritten by setting the bits of the 8-bit /LDAC register (DB7-DB0). See Table 9 for the /LDAC mode of operation. The default for each channel is “0” ie /LDAC pin works normally. Setting the bits to a “1” means the DAC channel will be updated regardless of the state of the /LDAC pin. This gives the added benefit of allowing any combination of channels to be synchronously updated. See Table 10 for contents of the Input Shift Register during the /LDAC overwrite mode of operation.

Load DAC OVERWRITE		
/LDACBITS (DB7-DB0)	/LDAC PIN	/LDAC Operation
0	1/0	Determined by /LDAC pin
1	x – Don't Care	DAC channels will update, overwriting the /LDAC pin

Table 9. LDAC Overwrite Definition

MSB																	LSB
DB31 – DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 – DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB0
x	0	1	1	0	x	x	x	x	x	DacH	DacG	DacF	DacE	DacD	DacC	DacB	DacA
<i>Don't Cares</i>	<i>COMMAND BITS (C2-C0)</i>				<i>ADDRESS BITS (A3 – A0)</i> <i>Don't cares</i>					<i>Don't Cares</i>	Setting /LDAC bit to "1" overwrites /LDAC pin						

Table 10. 32-Bit Input Shift Register Contents for /LDAC Overwrite Function

Power Supply Bypassing and Grounding

When accuracy is important in a circuit it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5628/AD5648/AD5668 should have separate analog and digital sections, each having its own area of the board. If the AD5628/AD5648/AD5668 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5628/AD5648/AD5668.

The power supply to the AD5628/AD5648/AD5668 should be bypassed with 10 μ F and 0.1 μ F capacitors. The capacitors should be physically as close as possible to the device with the 0.1 μ F capacitor ideally right up against the device. The 10 μ F capacitors are the tantalum bead type. It is important that the 0.1 μ F capacitor has low Effective Series Resistance (ESR) and

Effective Series Inductance (ESI), e.g., common ceramic types of capacitors. This 0.1 μ F capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

OUTLINE DIMENSIONS

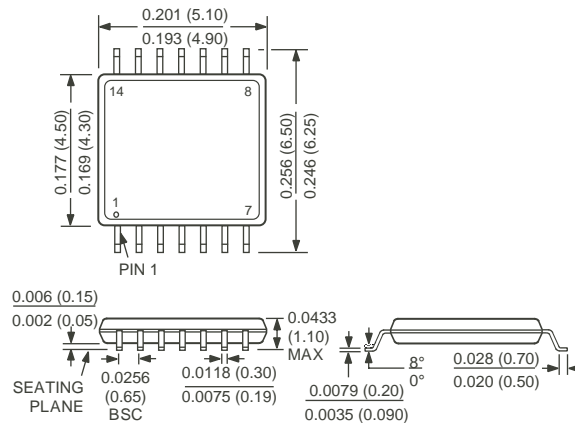


Figure 28. 14-Thin Shrink Small Outline Package [TSSOP] (RU-14)
Dimensions shown in millimeters

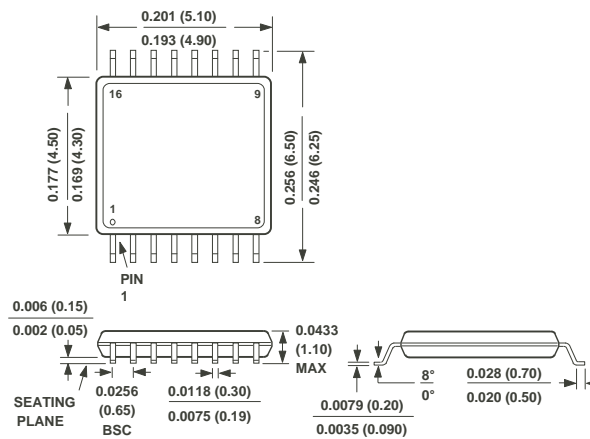


Figure 29. 16-Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Bit	Power-On-Reset	Internal Reference	Package Option1
AD5628BRUZ-1	12	Zero	1.25V	RU-14
AD5628BRUZ-2	12	Zero	2.5V	RU-16
AD5628ARUZ-2	12	Zero	2.5V	RU-16
AD5648BRUZ-1	14	Zero	1.25V	RU-14
AD5648BRUZ-2	14	Zero	2.5V	RU-16
AD5648ARUZ-2	14	Zero	2.5V	RU-16
AD5668BRUZ-1	16	Zero	1.25V	RU-14

AD5628/AD5648/AD5668

Preliminary Technical Data

AD5668BRUZ-2	16	Zero	2.5V	RU-16
AD5668BRUZ-3	16	Midscale	2.5V	RU-16
AD5668ARUZ-2	16	Zero	2.5V	RU-16
AD5668ARUZ-3	16	Midscale	2.5V	RU-16

1 Thin Shrink Small Outline Package (TSSOP)

This datasheet has been download from:

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Datasheets for electronics components.