Single Wire CAN Transceiver

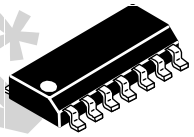
33897/A/B/C/D

SINGLE WIRE CAN TRANSCEIVER

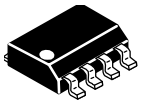
The 33897 Series provides a physical layer for digital communications purposes using a Carrier Sense Multiple Access/ Collision Resolution (CSMA/CR) data link operating over a single wire medium. This is more commonly referred to as Single Wire Controller Area Network (CAN).

The 33897 Series operates directly from a vehicle's 12 V battery system or a broad range of DC-power sources. It can operate at either low or high (33.33 kbps or 83.33 kbps) data rates. A high-voltage wake-up feature allows the device to control the regulator used in support of the MCU and other logic. The device includes a control terminal that can be used to put the module regulator into Sleep mode. The presence of a defined wake-up voltage level on the bus will reactivate the control line to turn the regulator and the system back on.

The device complies with the GMW3089v2.4 General Motors Corporation specification.



D SUFFIX
EF (Pb-FREE) SUFFIX
98ASB42565B
14-TERMINAL SOICN



EF (Pb-FREE) SUFFIX
98ASB42564B
8-TERMINAL SOICN

Features

- Waveshaping for Low Electromagnetic Interference (EMI)
- Detects and Automatically Handles Loss of Ground
- Worst-Case Sleep Mode Current of Only 60 µA
- Current Limit Prevents Damage Due to Bus Shorts
- Built-In Thermal Shutdown on Bus Output
- Protected Against Vehicular Electrical Transients
- Undervoltage Lockout Prevents False Data with Low Battery
- Pb-Free Packaging Designated by Suffix Code EF

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33897D/R2	-40°C to 125°C	14 SOICN
MC33897EF/R2		
MC33897AD/R2		
MC33897AEF/R2		
*MC/PC33897CEF/R2		
MC33897BEF/R2		8 SOICN
*MC/PC33897DEF/R2		

* Recommended device for all new designs

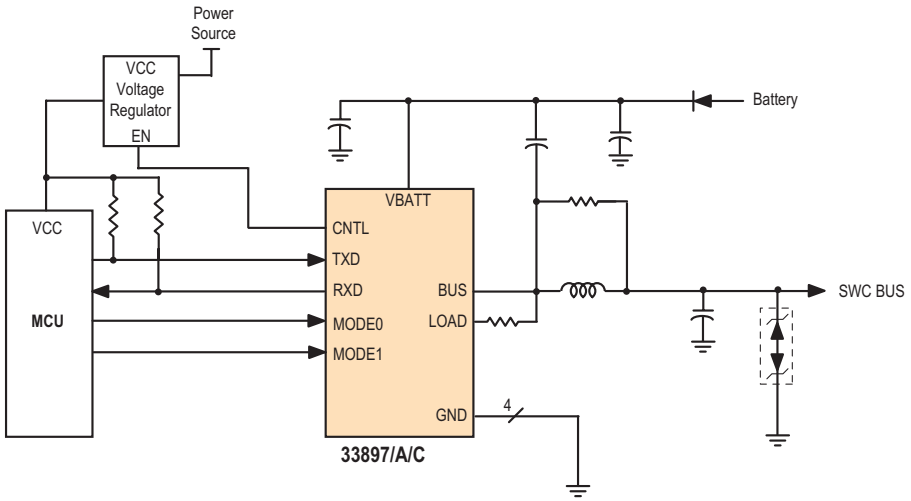


Figure 1. 33897/A/C Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

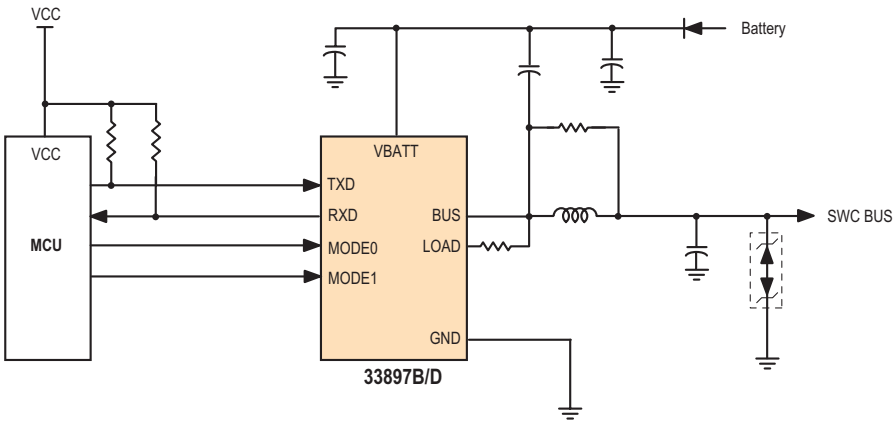


Figure 2. 33897B/D Simplified Application Diagram

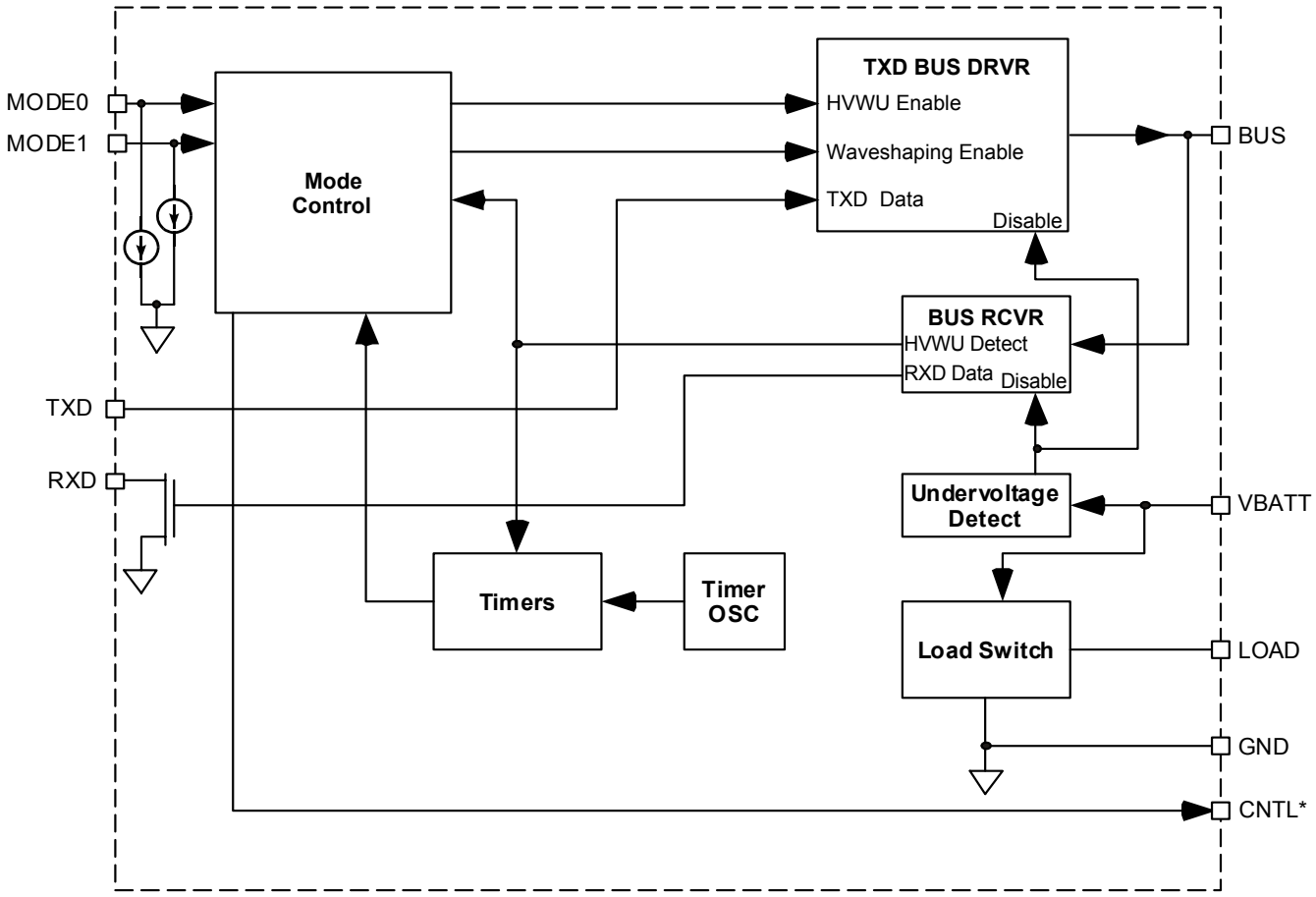
DEVICE VARIATIONS

Table 1. Device Variations

Part No.	Load Voltage Sleep Mode	Other Significant Differences	See Page
33897	1.0 V Max	• 14-Terminal Package	7
33897A	0.1 V Max	• 14-Terminal Package • Removes diode drop during Sleep Mode • May not detect Loss of Ground under certain module characteristics.	7
33897B	0.1 V Max	• 8-Terminal Package • Removes diode drop during Sleep Mode • Does not include the CNTL terminal • May not detect Loss of Ground under certain module characteristics.	2, 3, 4, 6, 7, 10, 12, 14
*33897C	0.1 V Max	• 14-Terminal Package • Removes diode drop during Sleep Mode • Effectively detects Loss of Ground	7
*33897D	0.1 V Max	• 8-Terminal Package • Removes diode drop during Sleep Mode • Effectively detects Loss of Ground • Does not include the CNTL terminal	2, 3, 4, 6, 7, 10, 12, 14

*Recommended device for all new designs

INTERNAL BLOCK DIAGRAM



*CNTL terminal is present on 33897/A/C only.

Figure 3. 33897/A/B/C/D Simplified Internal Block Diagram

TERMINAL CONNECTIONS

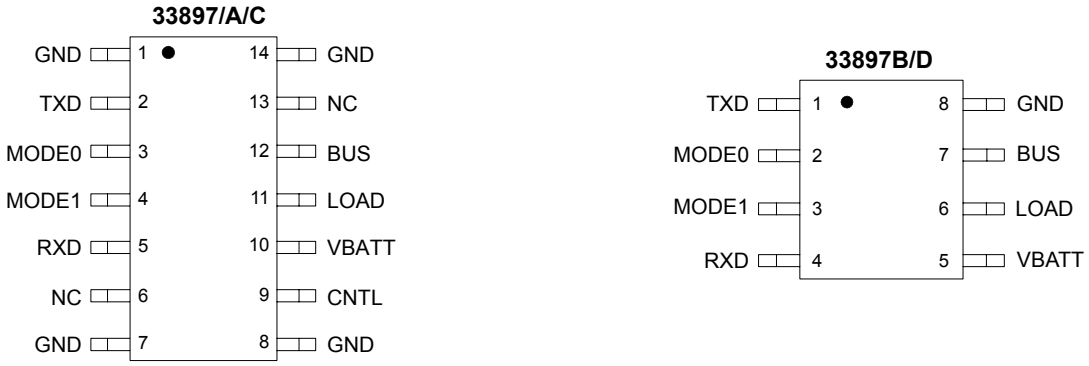


Figure 4. 33897/A/B/C/D Terminal Connections

Table 2. Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section, begining on page 12.

33897/A/C Terminal	33897B/D Terminal	Terminal Name	Formal Name	Definition
1, 7, 8, 14	8	GND	Ground	Electrical Common Ground and Heat removal. A good thermal path will also reduce the die temperature.
2	1	TXD	Transmit Data	Data input here will appear on the BUS terminal. A logic [0] will assert the bus, a logic [1] will make the bus go to the recessive state.
3, 4	2, 3	MODE0, MODE1	Mode Control	These terminals control Sleep Mode, Transmit Level, and Speed. They have weak pulldowns.
5	4	RXD	Receive Data	Open drain output of the data on BUS. A recessive bus = a logic [1], a dominant bus = logic [0]. An external pullup is required.
6, 13	–	NC	No Connect	No internal connection to these terminals. Terminal 13 can be connected to GND to allow the use of the 14-terminal or 8-terminal device. (1)
9	–	CNTL	Control	Provides a battery-level logic signal.
10	5	VBATT	Battery	Power input. An external diode is needed for reverse battery protection.
11	6	LOAD	Load	The external bus load resistor connects here to prevent bus pullup in the event of loss of module ground.
12	7	BUS	Bus	This terminal connects to the bus through external components.

Notes

1. Module boards can be planned for the 14-terminal package and still use the 8-terminal package.

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Electrical Ratings			
Supply Voltage	V_{BATT}	-0.3 to 40	V
Input Logic Voltage	V_{IN}	-0.3 to 7.0	V
RXD Terminal Voltage	V_{RXD}	-0.3 to 7.0	V
CNTL Terminal Voltage (33897/A/C only)	V_{CNTL}	-0.3 to 40	V
ESD Voltage[2] Human Body Model All Terminals Except BUS BUS Terminal Machine Model	V_{ESD}	 ±2000 ±4000 ±200	V
Thermal Ratings			
Ambient Operating Temperature[3]	T_A	-40 to 125	°C
Junction Operating Temperature	T_J	-40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	150	°C/W
Peak Package Reflow Temperature During Solder Mounting [4] D Suffix EF (Pb-Free) Suffix	T_{SOLDER}	 245 260	°C

Notes

2. ESD testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω)
3. When using the 8-terminal device, consider the power dissipation at a high operating voltage and maximum network loading at ambient temperatures exceeding 85°C.
4. Terminal soldering temperature limit is for 10 second maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Unless otherwise noted, characteristics noted under the following conditions: -40°C ≤ T_A ≤ 125°C. Voltages are relative to GND unless otherwise noted. All positive currents are into the terminal. All negative currents are out of the terminal.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Quiescent Current Sleep 5.0 V ≤ V_{BATT} ≤ 13 V (5)	I_{QSLP}	–	45	60	µA
Awake with Transmitter Disabled 5.0 V ≤ V_{BATT} ≤ 26.5 V	I_{QATDIS}	–	–	4.0	mA
Awake with Transmitter Enabled 5.0 V ≤ V_{BATT} ≤ 26.5 V	I_{QATEN}	–	–	9.0	mA
Undervoltage Shutdown	V_{BATTUV}	4.0	–	5.0	V
Thermal Shutdown (6) 5.0 V ≤ V_{BATT} ≤ 26.5 V	T_{SD}	150	–	190	°C
Thermal Shutdown Hysteresis (6) 5.0 V ≤ V_{BATT} ≤ 26.5 V	T_{SDHYS}	10	–	20	°C
LOGIC I/O, MODE0, MODE1, TXD, RXD					
Logic Input Low Level (MODE0, MODE1, and TXD) 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{IL}	–	–	0.8	V
Logic Input High Level (MODE0, MODE1, and TXD) 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{IH}	2.0	–	–	V
Mode Terminal Pulldown Current (MODE0 and MODE1) Terminal Voltage = 0.8 V, 5.0 V ≤ V_{BATT} ≤ 26.5 V	I_{PD}	10	–	50	µA
Receiver Output Low (RXD) I_{IN} = 2.0 mA, 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{OL}	–	–	0.45	V
CNTL (33897/A/C ONLY)					
CNTL Output Low I_{IN} = 5.0 µA, 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{OLCNTL}	–	–	0.8	V
CNTL Output High I_{OUT} = 180 µA, 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{OHCNTL}	V_{BATT} - 0.8	–	V_{BATT}	V

Notes

5. After $t_{CNTLFDLY}$
6. Thermal shutdown causes the BUS output driver to be disabled. Guaranteed by characterization.

Table 4. Static Electrical Characteristics (continued)

Unless otherwise noted, characteristics noted under the following conditions: -40°C ≤ T_A ≤ 125°C. Voltages are relative to GND unless otherwise noted. All positive currents are into the terminal. All negative currents are out of the terminal.

Characteristic	Symbol	Min	Typ	Max	Unit
LOAD					
LOAD Voltage Rise [7]	V_{LDRISE}				V
Normal Speed and Voltage Mode, Transmit High-Voltage Mode, Transmit High-Speed Mode					
I_{IN} = 1.0 mA, 5.0 V ≤ V_{BATT} ≤ 26.5 V		–	–	0.1	
Sleep Mode					
33897, I_{IN} = 7.0 mA		–	–	1.0	
33897A/B/C/D I_{IN} = 7.0 mA [8]		–	–	0.1	
Loss of Battery					
I_{IN} = 7.0 mA		–	–	1.0	
LOAD Leakage During Loss of Module Ground [9]	I_{LDLEAK}				µA
0.0 V ≤ V_{BATT} ≤ 18 V		0.0	–	-90	
BUS					
Passive Out BUS Leakage					µA
Passive In					
0.0 V ≤ V_{BATT} ≤ 26.5 V, -1.5 V ≤ V_{BUS} < 0 V	I_{LEAK}	-5.0	–	5.0	
Active In					
0.0 V ≤ V_{BATT} ≤ 26.5 V, 0 V < V_{BUS} ≤ 12.5 V	I_{LKAI}	-5.0	–	5.0	
BUS Leakage During Loss of Module Ground [10]					
0.0 V ≤ V_{BATT} ≤ 18 V	I_{BLKLOG}	-10	–	10	
High-Voltage Wake-up Mode Output High Voltage					V
12 V ≤ V_{BATT} ≤ 26.5 V, 200 Ω ≤ R_L ≤ 3332 Ω					
33897	$V_{HVWUOHF}$	9.7	–	12.5	
33897A/B/C/D	$V_{HVWUOHO}$	9.9	–	12.5	
5.0 V ≤ V_{BATT} < 12 V, 200 Ω ≤ R_L ≤ 3332 Ω		Lesser of V_{BAT} - 1.5 or 9.7		V_{BATT}	
High-Speed Mode Output High Voltage	V_{OHHS}				V
8.0 V ≤ V_{BATT} ≤ 16 V, 75 Ω ≤ R_L ≤ 135 Ω		4.2	–	5.1	
Normal Mode Output High Voltage					V
6.0 V ≤ V_{BATT} ≤ 26.5 V, 200 Ω ≤ R_L ≤ 3332 Ω	V_{NOHF}	4.4	–	5.1	
5.0 V ≤ V_{BATT} < 6.0 V, 200 Ω ≤ R_L ≤ 3332 Ω	V_{NOHO}	Lesser of V_{BATT} - 1.6 or 4.4	–	Lesser of V_{BATT} or 5.1	
BUS Low Voltage	V_{OL}				V
5.0 V ≤ V_{BATT} ≤ 26.5 V, 200 Ω ≤ R_L ≤ 3332 Ω		-0.2	–	0.2	
Short Circuit BUS Output Current	I_{BSC}				mA
Dominant State, 5.0 V ≤ V_{BATT} ≤ 26.5 V		-350	–	-150	

Notes

7. GMW3089V2.4 specifies the maximum load voltage rise to be 0.1 V whenever module battery is intact, including when in Sleep mode. The maximum load voltage rise of 1.0 V in Sleep mode is a GM-approved exception to GMW3089V2.4.
8. 33897A/B/C/D remove diode drop during Sleep mode.
9. LOAD terminal is at system ground voltage.
10. BUS terminal is at system ground voltage

Table 4. Static Electrical Characteristics (continued)

Unless otherwise noted, characteristics noted under the following conditions: -40°C ≤ T_A ≤ 125°C. Voltages are relative to GND unless otherwise noted. All positive currents are into the terminal. All negative currents are out of the terminal.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS (continued)					
Input Threshold					V
Awake 5.0 V ≤ V_{BATT} ≤ 26.5 V	V_{BIA}	2.0	–	2.2	
Sleep 12 V ≤ V_{BATT} ≤ 26.5 V	V_{BISF}	6.6	–	7.9	
Sleep 5.0 V ≤ V_{BATT} < 12 V	V_{BISO}	Lesser of 6.6 V or V_{BATT} - 4.3	–	Lesser of 7.9 V or V_{BATT} - 3.25	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Unless otherwise noted, characteristics noted under the following conditions: -40°C ≤ T_A ≤ 125°C. Voltages are relative to GND unless otherwise noted. All positive currents are into the terminal. All negative currents are out of the terminal.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS					
Normal Speed Rising Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs Measured from TXD = V_{IL} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 3.7 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (11) Min Time to V_{BUSMOD} = 1.0 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (11) Max Time to V_{BUSMOD} = 2.7 V, V_{BATT} = 5.0 V (11) Min Time to V_{BUSMOD} = 1.0 V, V_{BATT} = 5.0 V (11)	$t_{DLYNORMRO}$	2.0	–	6.3	µs
Normal Speed Falling Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs Measured from TXD = V_{IH} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 1.0 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (11) Min Time to V_{BUSMOD} = 3.7 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (11) Max Time to V_{BUSMOD} = 1.0 V, V_{BATT} = 5.0 V (11) Min Time to V_{BUSMOD} = 2.7 V, V_{BATT} = 5.0 V (11)	$t_{DLYNORMFO}$	1.8	–	8.5	µs
High-Speed Rising Output Delay 75 Ω ≤ R_L ≤ 135 Ω, 0.0 µs ≤ Load Time Constants ≤ 1.5 µs, 8.0 V ≤ V_{BATT} ≤ 16 V Measured from TXD = V_{IL} to V_{BUS} as follows: Max Time to V_{BUS} = 3.7 V (12) Min Time to V_{BUS} = 1.0 V (12)	$t_{DLYHSRO}$	0.1	–	1.7	µs
High-Speed Falling Output Delay 75 Ω ≤ R_L ≤ 135 Ω, 0.0 µs ≤ Load Time Constants ≤ 1.5 µs, 8.0 V ≤ V_{BATT} ≤ 16 V Measured from TXD = V_{IH} to V_{BUS} as follows: Max Time to V_{BUS} = 1.0 V (12) Min Time to V_{BUS} = 3.7 V (12)	$t_{DLYHSFO}$	0.04	–	3.0	µs

Notes

11. V_{BUSMOD} is the voltage at the BUSMOD node in Figure 7, page 14.
12. V_{BUS} is the voltage at the BUS terminal in Figure 8, page 14.

Table 5. Dynamic Electrical Characteristics (continued)

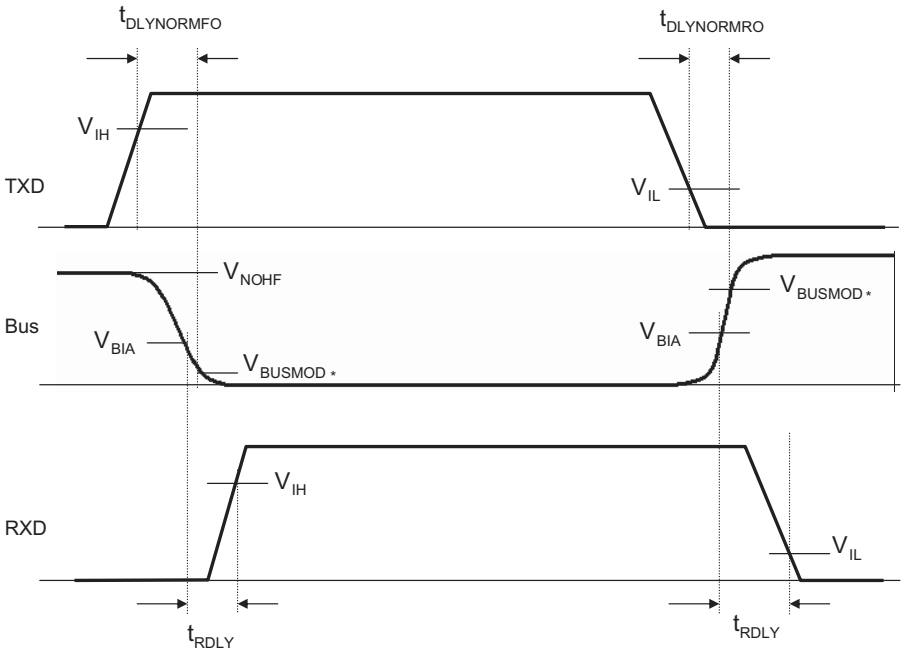
Unless otherwise noted, characteristics noted under the following conditions: -40°C ≤ T_A ≤ 125°C. Voltages are relative to GND unless otherwise noted. All positive currents are into the terminal. All negative currents are out of the terminal.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS (continued)					
High-Voltage Rising Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs Measured from TXD=V_{IL} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 3.7 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (13) Min Time to V_{BUSMOD} = 1.0 V, 6.0 V ≤ V_{BATT} ≤ 26.5 V (13) Max Time to V_{BUSMOD} = 9.4 V, 12.0 V ≤ V_{BATT} ≤ 26.5 V (13)	$t_{DLYHVRO}$	 2.0 2.0 2.0	 – – –	 6.3 6.3 18	µs
High-Voltage Falling Output Delay 200 Ω ≤ R_L ≤ 3332 Ω, 1.0 µs ≤ Load Time Constants ≤ 4.0 µs, 12.0 V ≤ V_{BATT} ≤ 26.5 V Measured from TXD=V_{IH} to V_{BUS} as follows: Max Time to V_{BUSMOD} = 1.0 V (13) Min Time to V_{BUSMOD} = 3.7 V (13)	$t_{DLYHVFO}$	 1.8 1.8	 – –	 14 14	µs
Receiver RXD					
Receive Delay Time (5.0 V ≤ V_{BATT} ≤ 26.5 V) Awake	t_{RDLY}	0.2	–	1.0	µs
Receive Delay Time (BUS Rising to RXD Falling, 5.0 V ≤ V_{BATT} ≤ 26.5 V) Sleep	t_{RDLYSL}	10	–	70	µs
CNTL					
CNTL Falling Delay Time (5.0 V ≤ V_{BATT} ≤ 26.5 V) (33897/A/C only)	$t_{CNTLFDLY}$	300	–	1000	ms

Notes

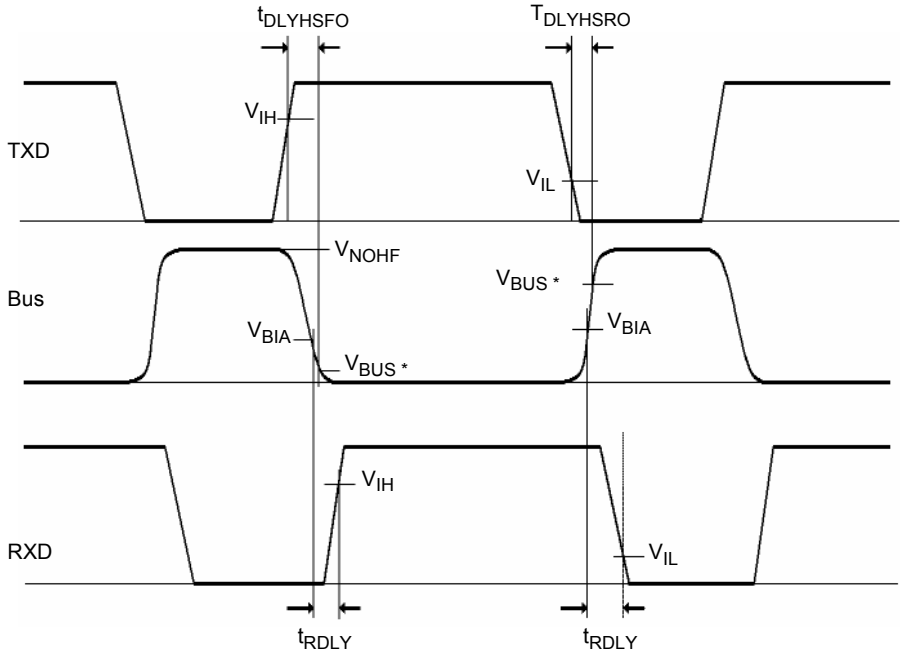
13. V_{BUSMOD} is the voltage at the BUSMOD node in Figure 7, page 14.

TIMING DIAGRAMS



* V_{BUSMOD} is the voltage at the BUSMOD node in Figure 7.

Figure 5. TXD, Bus and RXD Waveforms in Normal Mode



* V_{BUS} is the voltage at the BUS terminal in Figure 8.

Figure 6. TXD, Bus and RXD Waveforms in High Speed Mode

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33897 Series is intended for use as a physical layer device in a Single Wire CAN communications bus. Communications takes place from a single terminal over a single wire using a common ground for a current return path. Two data rates are available, with the high rate used for factory or assembly line communications and the lower for actual system communications where the radiated EMI of the higher rate could be an issue.

Two terminals control the mode of operation (sleep, low-speed, high-speed, and high-voltage wake-up).

FUNCTIONAL TERMINAL DESCRIPTION

The 33897 Series is intended to be used with an MCU to control its operation and to process and generate the data for the bus.

Ground Terminals (33897/A/C)

The four ground terminals are not only for electrical conduction, their number and locations at each of the four corners serve also to remove heat from the IC. The biggest benefit of this is obtained by putting a lot of copper on the PCB in this area and, if ground is an internal layer, by adding numerous plated-through connections to it with the largest diameter holes the layout can use.

TXD Data

The data driven onto the SWCAN bus is inverted from the TXD terminal. A “1” driven on TXD will result in an undriven (recessive) state (bus at near zero volts). When the TXD terminal is low, the output goes to a driven state. The voltage and waveshaping in the driven state is determined by the levels on the MODE0 and MODE1 terminals (refer to Table 6).

Table 6. Mode Control Logic Levels

Logic Level		Operation
MODE0	MODE1	
0	0	Sleep Mode
0	1	High Voltage Wake-Up Mode
1	0	High Speed Mode
1	1	Normal Mode

Mode Control

The MODE terminals control the transmitter filtering and BUS voltage and the IC sleep mode operation. Table 6 shows the mode versus the logic levels on MODE0 and MODE1.

The MODE0 and MODE1 terminals have a weak pulldown in the IC so that in case the terminals are not driven, the device will enter the sleep mode. This is usually the situation as the MCU comes out of reset, before the driving signals have been configured as outputs.

RXD Data

The data received on the bus is translated to logic levels on this terminal. This terminal is a logic high when the bus is in the recessive state (near zero volts) and is logic low when the bus is in either the normal or high-voltage dominant state.

This is an open-drain type of output that requires an external resistor to pull it up. When the device is in sleep mode, the output will be off unless a high-voltage wake-up level is detected on the bus. If the wake-up level is detected, the output will be driven by the data on the bus. If the level of the data returns to normal level, the output will return to off after a short delay unless a non-sleep mode condition is set by the MCU.

LOAD Switch

This switch is on in all operating modes unless a loss of ground is detected. If this happens, the switch is opened and the resistor normally attached to its terminal will no longer pass current to or from the bus.

CNTL Output (33897/A/C Only)

This logic level signal is used to control a V_{CC} regulator. When the output is low, the V_{CC} regulator is expected to shutdown. This is normally used to shut down the MCU and all the devices powered by V_{CC} when the IC is in sleep mode. This is done to save power. When the part is taken out of the sleep mode by the higher-than-normal bus voltage, this terminal is asserted high and the V_{CC} regulator brings its output up to the regulated level. This starts the MCU, which controls the mode of the IC. The MCU must change the mode signals to non-sleep mode levels in order to keep this terminal from going low. There is a delay to allow the MCU to fully wake up and take control after the high-voltage signaling is removed before the level on this output returns low. After a delay time, even if the bus is at high voltage, the IC will return to sleep mode if both MODE terminals are low.

VBATT Input

This power input is not reverse battery protected and should use an external diode to protect it from damage owing to reverse battery if this protection is desired. The voltage drop of the diode must be taken into consideration when the operating range of the system is being determined. This

diode is generally used to protect the entire module from reverse battery and should be selected accordingly.

BUS I/O

This input/output may require electrostatic discharge (ESD) and/or EMI external circuitry. A set of components is shown in the simplified application diagrams on page 15 of this datasheet. The value of the capacitor should be adjusted downward in direct proportion to the added capacitance of the ESD or EMI circuits. The series resistance of the inductor should be kept below 3.5 Ω to prevent its voltage drop from significantly degrading system noise margins.

FUNCTIONAL BLOCK DIAGRAM COMPONENTS

Timer OSC

This circuit generates a 500 kHz signal to be used for internal logic. It is the reference for some of the required delays.

Timers

This circuit contains the timing logic used to hold the CNTL active for the required time after the conditions for sleep mode have been met. It is also used to keep the TXD driver active for a period of time after it has generated a passive level on the bus.

Mode Control

This circuit contains the control logic for the various operating modes and conditions required for the IC.

BUS RCVR

This circuit translates the levels on the BUS terminal to a CMOS level indicating the presence of a logic [0] or a logic [1]. It also determines the presence of a high-voltage wake-up (HVWU) signal that is passed to Mode Control and Timers circuits. An analog filter is used to “de-glitch” the high-voltage wake-up signal and prevent false exits from the sleep mode.

TXD BUS DRVR

This circuit drives the BUS. It can drive it with the higher voltage wake-up signals when enabled by the Mode Control circuit. It can also provide waveshaping for reduced EMI or not provide it for the higher data rate mode. The actual data is received on TXD at CMOS logic levels, then translated by this circuit to the necessary operating voltages.

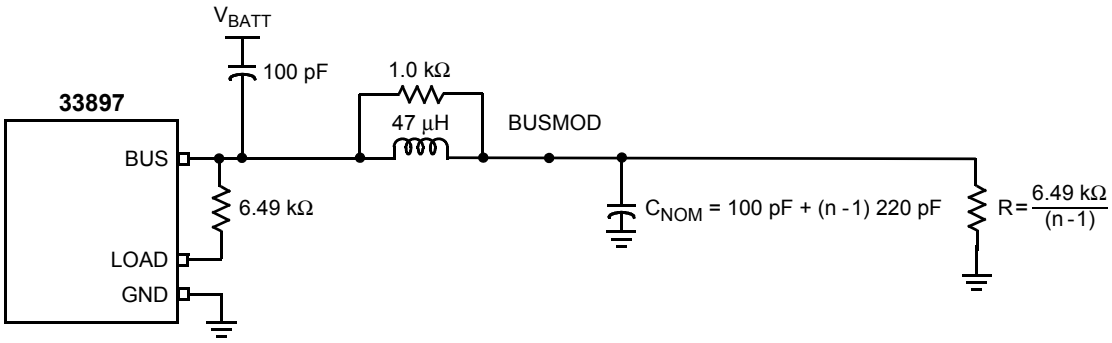
Undervoltage Detect

This circuit monitors internal operating voltage to assure proper operation of the part. If a low-voltage condition is detected, it sends a signal to disable the BUS RCVR and TXD BUS DRVR circuits. This prevents incorrect data from being put on the bus or sent to the MCU.

Load Switch

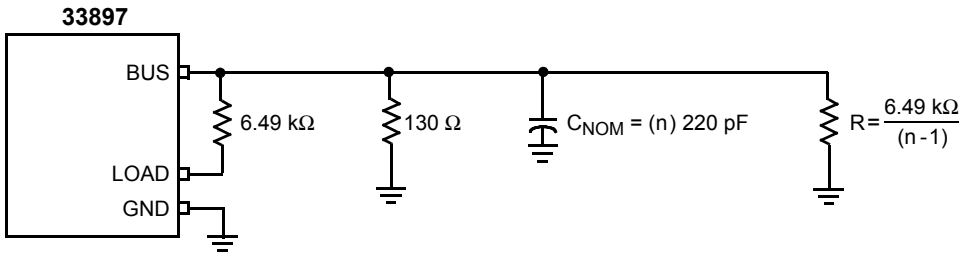
The LOAD switch provides a path for an external resistor connected to the BUS to be connected to ground. When a loss of ground is detected, this switch is opened to prevent the current that would normally be flowing to the ground from the module from going back through the load resistor and raising the bus level. The circuit is opened when the voltage between GND and VBATT becomes too low as would be the case if module ground were lost.

BUS LOADING PARAMETERS



Note: The letter “n” represents the number of nodes in the system.

Figure 7. Transmitter Delays in Normal and Transmit High-Voltage Wake-Up Modes



Note: The letter “n” represents the number of nodes in the system.

Figure 8. Transmitter Delays in Transmit High-Speed Mode

TYPICAL APPLICATIONS

The 33897/A/C can be used in applications where the module includes a regulator that has the capability of going into Sleep mode by having an Enable terminal. See Figure 9. When the module's regulator is in sleep mode, the module is turned off. The module waits for a defined wake-up voltage level on the bus. This wake-up voltage will activate the control line, which enables the regulator and turns the module back on. This 33897/A/C feature allows the module to be more energy efficient since the current consumption is significantly lowered when it goes into sleep mode.

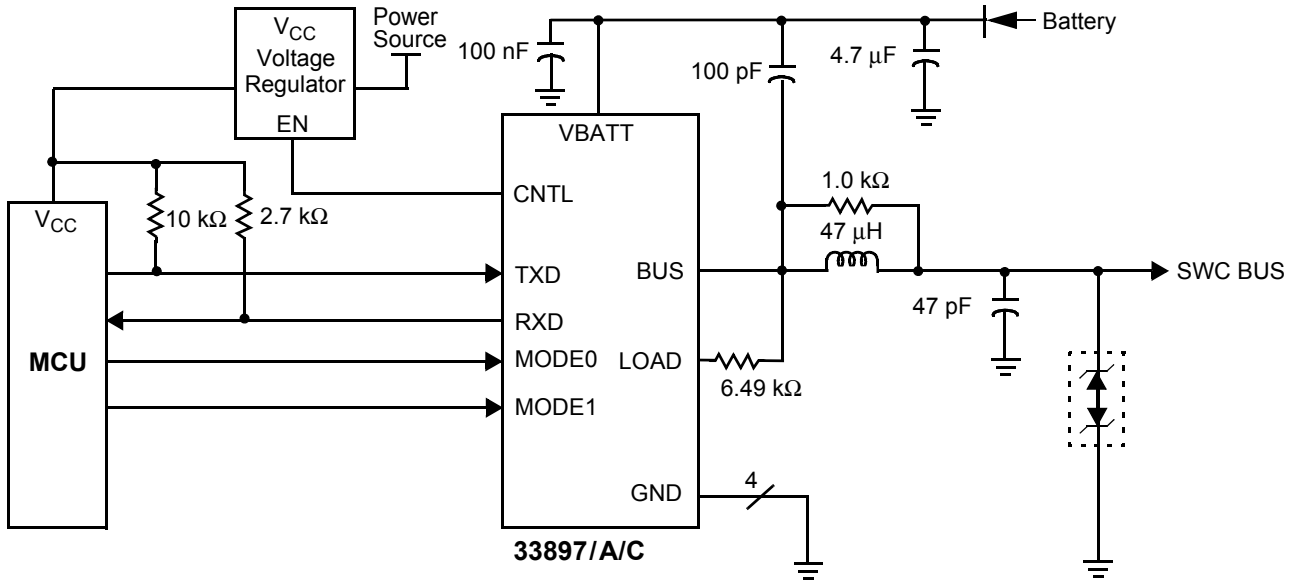


Figure 9. 33897/A/C Typical Application Schematic

The 33897B/D do not have a control terminal to enable the module's regulator. See Figure 10. The 33897B/D can be used in applications where board space is limited and there is no need for the module to have control over its regulator via the transceiver.

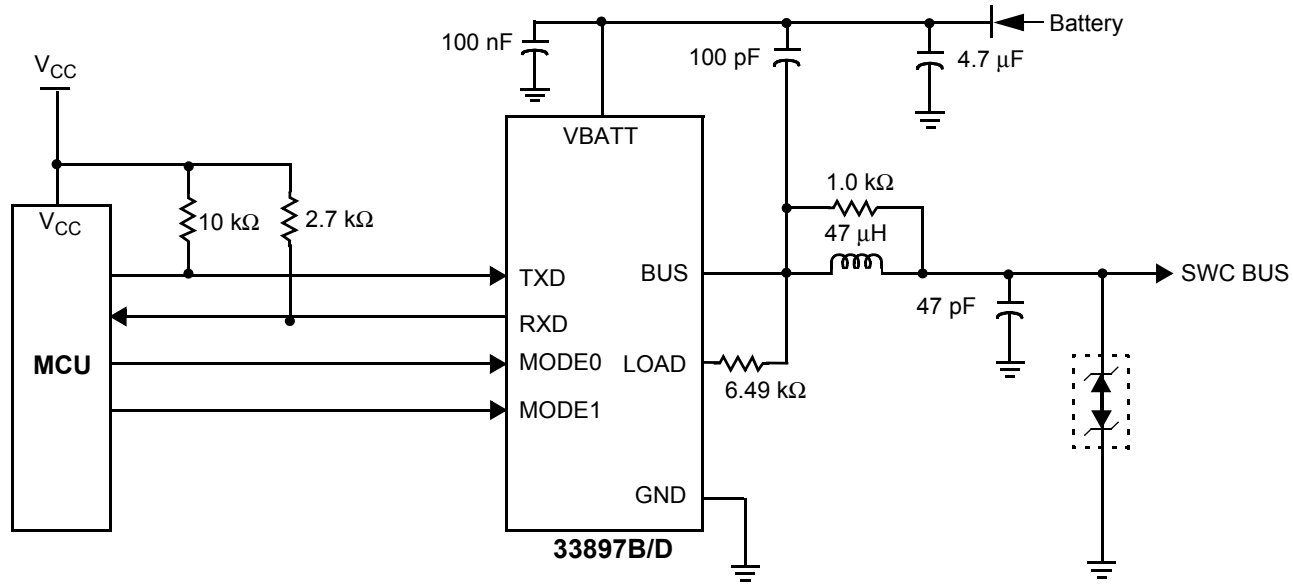


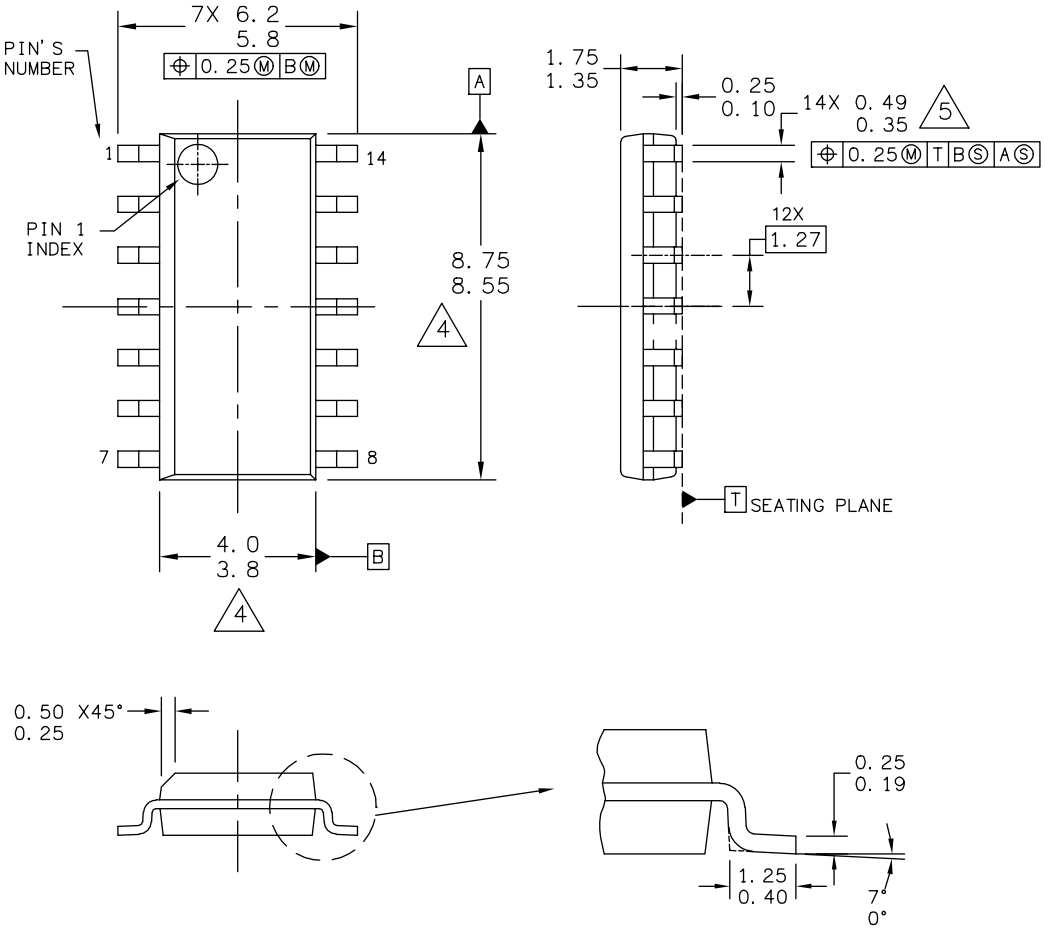
Figure 10. 33897B/D Typical Application Schematic

PACKAGING

PACKAGE DIMENSIONS

Important: For the most current Package revision, visit www.freescale.com and perform a Keyword Search on the “98A” drawing number below.

D SUFFIX
EF (Pb-FREE) SUFFIX
14-TERMINAL SOIC NARROW BODY
PLASTIC PACKAGE
98ASB42565B
ISSUE H



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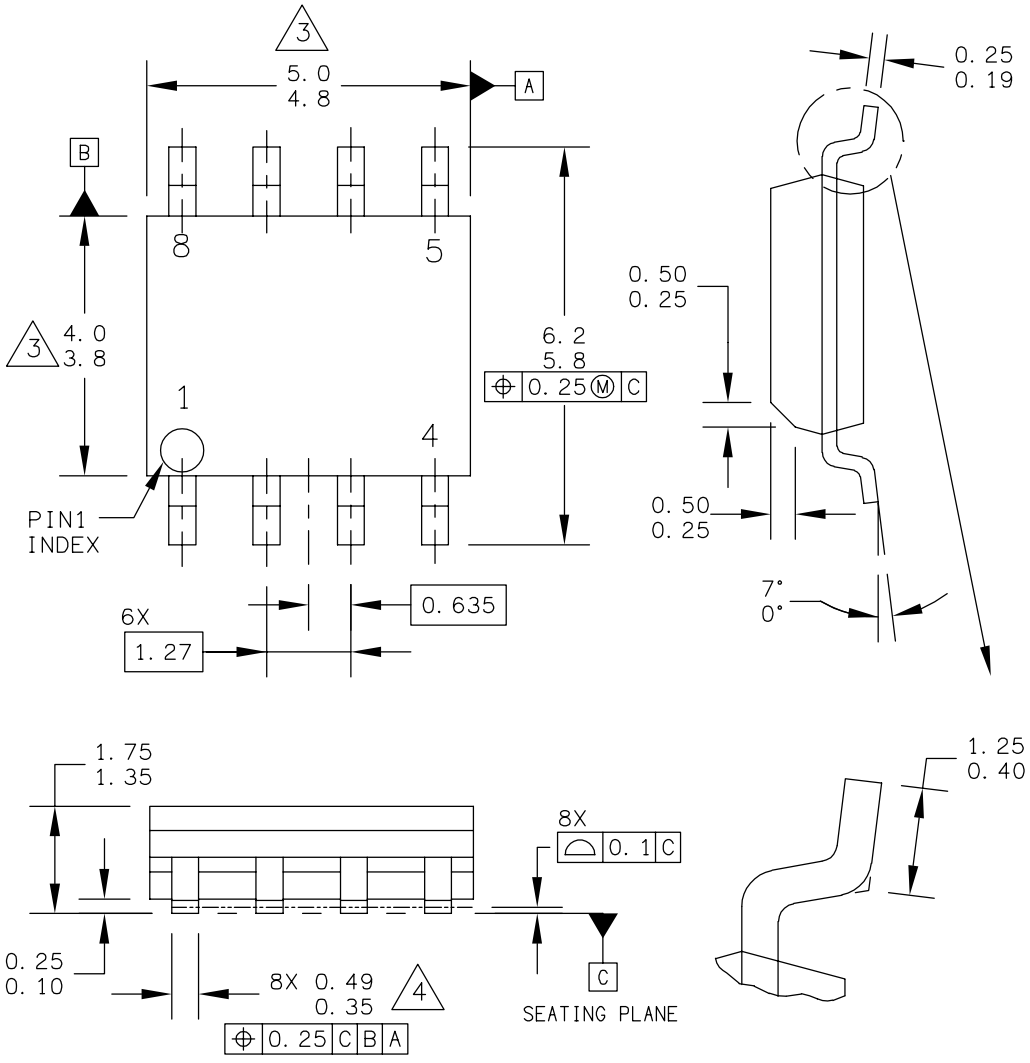
	CASE NUMBER: 751A-03	19 JUL 2005
	STANDARD: JECDEC MS-012AB	

33897/A/B/C/D

PACKAGE DIMENSIONS (CONTINUED)

EF (Pb-FREE) SUFFIX
8-TERMINAL SOIC NARROW BODY
PLASTIC PACKAGE
98ASB42564B
ISSUE U



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	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

33897/A/B/C/D

REVISION HISTORY

Revision	Date	Description of Changes
9.0	5/2005	• Converted to Freescale format • Added A & B Versions • Updated Device Variation Table, and Note “* Recommended device for all new designs” • Added EF (Pb-Free) Devices, and higher soldering temperature
10.0	8/2005	• Implemented Revision History page • Updated Simplified Application Diagrams • Updated Typical Application Schematic
11.0	12/2005	• Added 33897C and D versions and Timing Diagrams

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