

# GD4027B

## DUAL JK FLIP-FLOP

**DESCRIPTION** – The 4027B is a Dual JK Flip-Flop which is edge-triggered and features independent Direct Set, Direct Clear, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct ( $C_D$ ) and Set Direct ( $S_D$ ) are independent and override the J, K, or Clock inputs. The outputs are buffered for best system performance.

### PIN NAMES

J, K	Synchronous Inputs
CP	Clock Input (L → H Edge-Triggered)
$S_D$	Asynchronous Direct Set Input (Active HIGH)
$C_D$	Asynchronous Direct Clear Input (Active HIGH)
Q	True Output
$\bar{Q}$	Complement Output

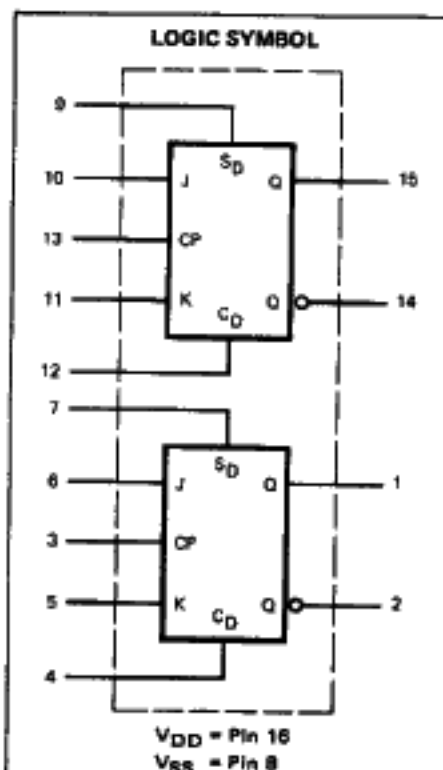
### TRUTH TABLES

ASYNCHRONOUS INPUTS		OUTPUTS	
$S_D$	$C_D$	Q	$\bar{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

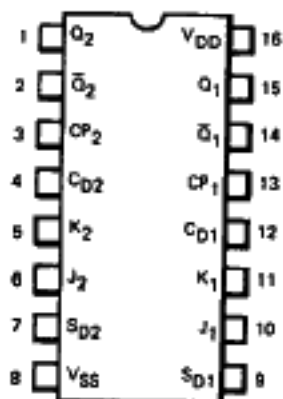
L = LOW Level  
 H = HIGH Level  
 $\uparrow$  = Positive-Going Transition  
 $Q_{n+1}$  = State After Clock Positive Transition

SYNCHRONOUS INPUTS			OUTPUTS	
CP	J	K	$Q_{n+1}$	$\bar{Q}_{n+1}$
$\uparrow$	L	L	NO CHANGE	
$\uparrow$	H	L	H	L
$\uparrow$	L	H	L	H
$\uparrow$	H	H	$\bar{Q}_n$	$Q_n$

Conditions:  $S_D = C_D = \text{LOW}$



### CONNECTION DIAGRAMS DIP (TOP VIEW)



**NOTE:**  
 The SO Package has the same pinouts (Connection Diagram) as the Dual In-Line Package.

GS CMOS · GD4027B

DC CHARACTERISTICS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
$I_{DD}$	Quiescent Power	XC			4			8			16	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$
					30			60			120		MAX	
	Supply Current	XM			1			2			4	$\mu$ A	MIN, 25°C	
					30			60			120		MAX	

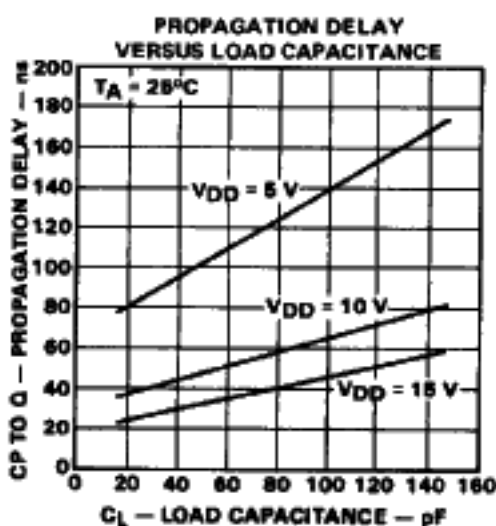
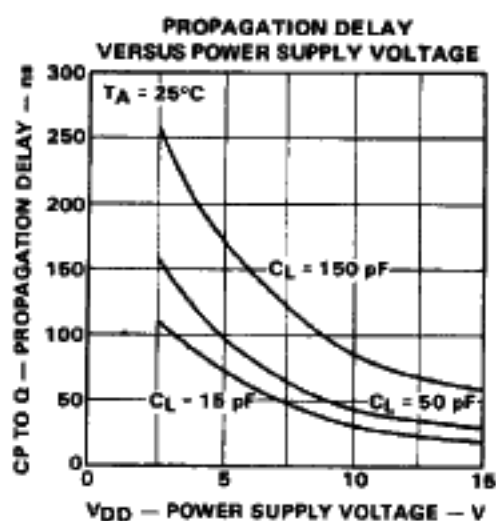
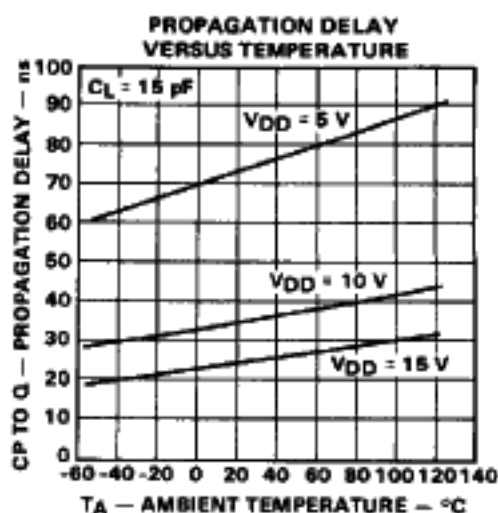
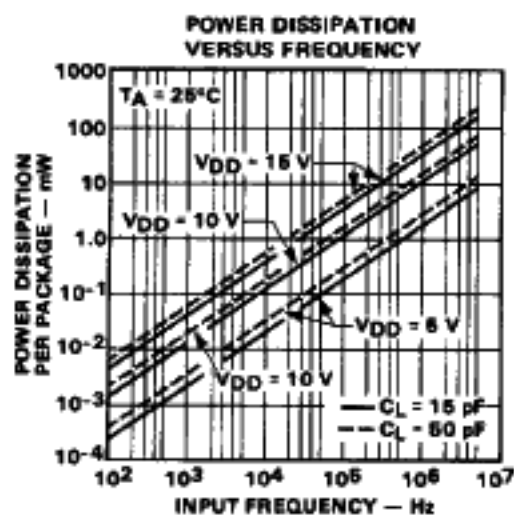
AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$  C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, CP to Q, $\bar{Q}$		100	200		45	85		30	68	ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$ Input Transition Times < 20 ns
$t_{PHL}$			100	200		45	85		30	68	ns	
$t_{PLH}$	Propagation Delay, $S_D$ to Q		180	350		90	175		75	140	ns	
$t_{PHL}$	Propagation Delay, $C_D$ to Q		180	350		90	175		75	140	ns	
$t_{TLH}$	Output Transition Time		85	150		45	85		30	50	ns	
$t_{THL}$			85	150		45	85		30	50	ns	
$t_s$	Set-Up Time, J, K to CP	100	45		40	20		32	15		ns	
$t_h$	Hold Time, J, K to CP	0	-25		0	-10		0	-5		ns	
$t_{wCP(L)}$	Minimum Clock Pulse Width	150	75		70	35		56	25		ns	
$t_{wS_D(H)}$	Minimum $S_D$ Pulse Width	150	75		60	30		48	25		ns	
$t_{wC_D(H)}$	Minimum $C_D$ Pulse Width	150	75		60	30		48	25		ns	
$t_{recS_D}$	Recovery Time for $S_D$	0	-5		0	-4		0	-3		ns	
$t_{recC_D}$	Recovery Time for $C_D$	0	-5		0	-4		0	-3		ns	
$f_{MAX}$	Maximum CP Frequency (Note 2)	4	8		8	16		9	19		MHz	

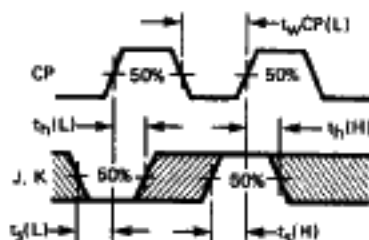
NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- For  $f_{MAX}$  input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
- It is recommended that input rise and fall times to the Clock Input be less than 15  $\mu$ s at  $V_{DD} = 5$  V, 4  $\mu$ s at  $V_{DD} = 10$  V, and 3  $\mu$ s at  $V_{DD} = 15$  V.

TYPICAL ELECTRICAL CHARACTERISTICS

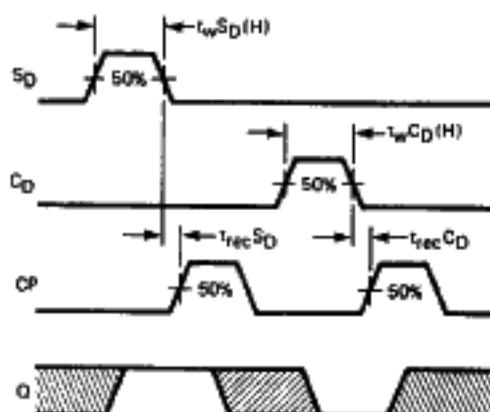


SWITCHING WAVEFORMS



NOTE:  
 $t_s$  &  $t_h$  are shown as positive values but may be specified as negative values.

SET-UP TIMES, HOLD TIMES,  
 AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR  $S_D$ , RECOVERY TIME FOR  $C_D$ ,  
 MINIMUM  $S_D$  PULSE WIDTH, AND MINIMUM  $C_D$  PULSE WIDTH