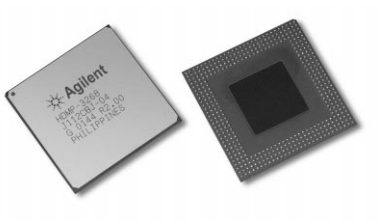
Agilent HDMP-3268
3.2 Gbit/sec 68x68 Crosspoint Switch
Data Sheet



Description

The HDMP-3268 is a 68x68 digital crosspoint switch with data handling capacities of up to 3.2 Gbit/sec on each channel. The non-blocking switch uses 68 fully independent multiplexers to allow each output port to be independently programmed to be connected to any input port. All data channels are designed with a fully differential architecture to insure data integrity and resistance to noise and crosstalk. The part is designed in a reliable BiCMOS process, operates off of a single 2.5 V supply and is packaged in a 400 pin HPBGA.

Data comes in to each of the 68 ports as a DC balanced differential signal (DIN[0:67]). Each input port then presents the data to the input of a multiplexer, which routes the signal to the selected output port (DOUT[0:67]). Input and output ports are required to be AC-coupled unless connected to either this or another HDMP-3268. The crosspoint switch multiplexers are controlled by 68 address registers (one for each multiplexer). The address registers are programmed through the program and control pins.

The high-speed input buffer contains input equalization to improve signal integrity over copper traces. The equalization may be modified on an individual port basis through use of the program and control pins (DATA[6:0], CH[6:0], WSTB, CNTL, CS and RW). The crosspoint switch address and control register configuration may be read back from the switch through use of the RW and CNTL inputs.

The DC levels of the high speed outputs are consistent with the input levels of the high speed inputs. Therefore, the outputs of the HDMP-3268 can be connected to inputs of the HDMP-3268 without blocking capacitors as long as the supply voltages for the two parts are identical.

Features

- **Supports data rates up to 3.2 Gbit/sec on each channel**
- **Fully differential high-speed signal path for highest signal integrity**
- **Implemented as 68 independent 68-input multiplexers**
- **Supports broadcast/multicast modes. Inputs can be connected to multiple outputs**
- **Provides two independent switch matrix configuration register sets**
- **Low jitter, low crosstalk**
- **Individually programmable high-speed output signal amplitude to optimize drive of various PCB and backplane distances**
- **Individually programmable input equalization for better signal integrity**
- **Unused input and output channels can be powered off to reduce power consumption**
- **Broadcast programming mode to rapidly configure the default switch settings**
- **SSTL_2 and LVTTL compatible inputs and outputs on the programming bus and the control signals**
- **Single supply voltage of 2.5 V**
- **Low power 13.5 W maximum**
- **Packaged in a 400-pin High Performance Ball Grid Array (HPBGA)**
- **Implemented in a high performance BiCMOS process**

Applications

- **Optical cross connect switches**
- **Optical add-drop multiplexers**
- **Telecom switches**
- **Other optical (OEO) switch fabrics**
- **Backplane interconnect switch fabrics**

Block Description

Figure 1 gives an overall block diagram for the HDMP-3268. The operation of HDMP-3268 is discussed below.

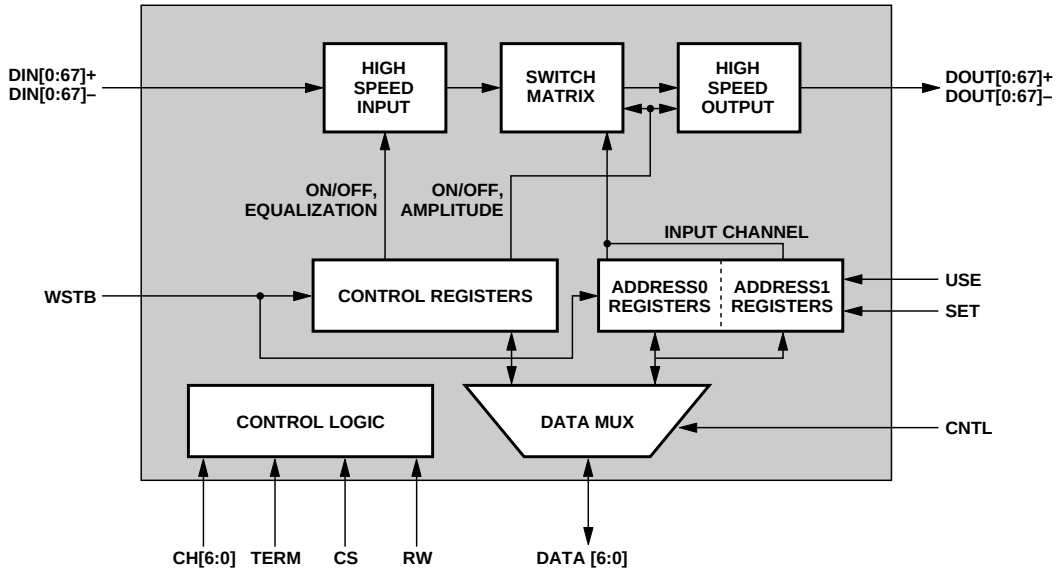


Figure 1. Block diagram for the HDMP-3268.

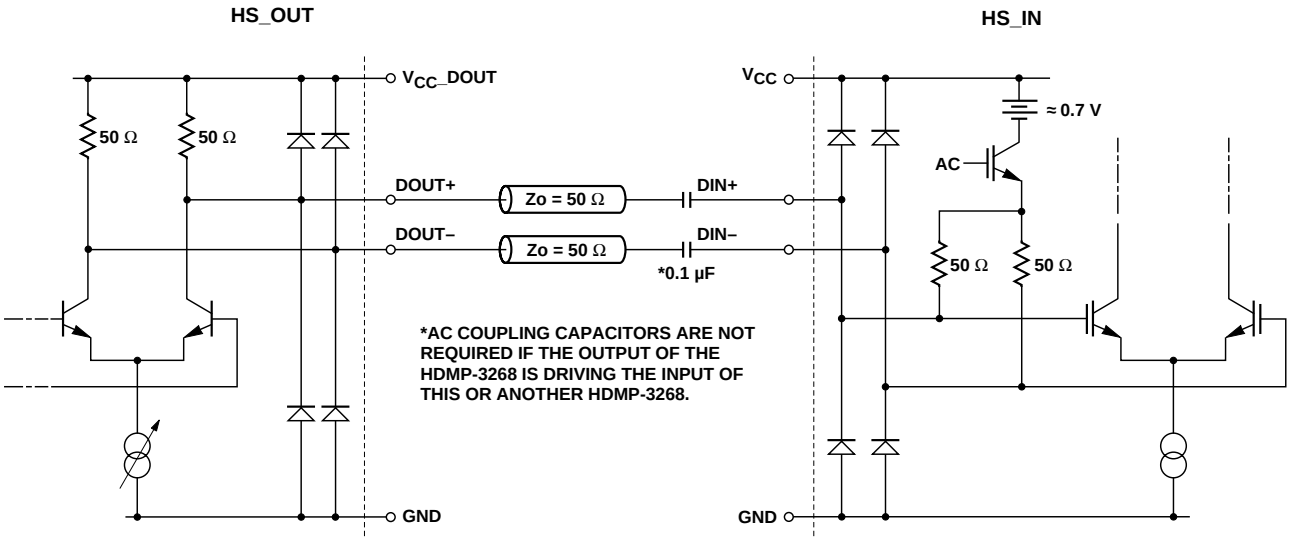


Figure 2. High-speed output and input simplified circuit schematics.

High-Speed Inputs and Outputs

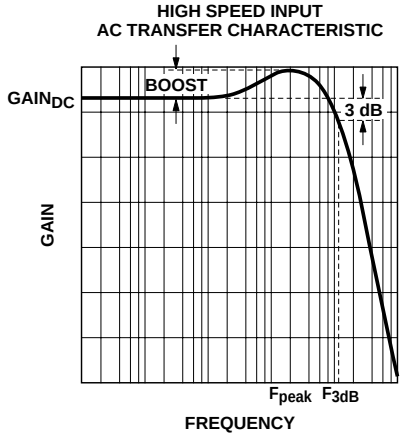
Figure 2 shows simplified circuit diagrams for the HDMP-3268's high speed input and output cells. A typical connection between the output and input cells is also shown. The output cell is designed to drive 50 Ω transmission lines and to be terminated at the destination end in 50 Ω. When the output is intended to connect to the input of another HDMP-3268 as in a CLOS architecture, no AC coupling capacitors are required. The output amplitude of the HDMP-3268 is programmable in three levels from approximately 500 mV to 1.0 V peak-to-peak differential. In addition, the output driver and its associated multiplexer can be turned off to save power if an output is not used.

The HDMP-3268 high speed input cell provides on-chip termination resistors of 50 Ω from each input to an on-chip bias voltage generator which sets the input common mode voltage at approximately 0.7 V below the positive supply. When the input is intended to be DC coupled, as in the case of the input being connected to the output of another HDMP-3268, the common mode bias voltage is disconnected from the termination resistors, and the two 50 Ω resistors form a 100 Ω differential termination. DC coupling is the default setting for the HDMP-3268. The input cell has levels of input equalization which can be programmed through the digital control interface. The AC termination voltage also can be enabled through a control register. Unused input cells can be disabled to save power.

Figure 3 shows a typical transfer characteristic of the high-speed input for the different input equalization settings. The correct equalization setting depends upon the actual PCB environment in which the HDMP-3268 resides. The recommended procedure to set the input equalization setting is to characterize the HDMP-3268 on the PCB and to adjust the equalization setting to give minimum jitter at the output of the HDMP-3268. The correct equalization settings should be stored and loaded into the HDMP-3268 upon power-up. The AC characteristics of the high speed input, high speed output, and multiplexer block are specified in Table 8, AC Electrical Specifications.

Digital Interface

The HDMP-3268 has a parallel bi-directional digital interface for configuring the switch matrix and for controlling the various functions such as input equalization, output amplitude, and power on/off. All of the registers can be read back to check valid programming. There are 204 7-bit registers organized into three sets of 68 registers each. One set is used to control power on/off, equalization, etc. The other two sets are used to configure the switch matrix. The individual registers are accessed using an address/data scheme. The particular register address is placed on the CH[6:0] lines, and the register data is placed on the DATA[6:0] lines, either by the controller in write mode (RW=0), or by the HDMP-3268 in read mode (RW=1). Data is latched into the internal registers on the rising edge of WSTB. The control registers are accessed when the CNTL signal is high. Otherwise, the address registers are accessed. Figure 4 and Table 1 show the register read and write timing diagram and specifications. See the switch matrix configuration section for more details. A chip select signal allows



TYPICAL PERFORMANCE OF HIGH SPEED INPUT CELL WITH DIFFERENT EQUALIZATION SETTINGS

EQUALIZATION SETTING	$GAIN_{DC}$ (dB)	BOOST (dB)	F_{peak} (GHz)	F_{3dB} (GHz)
000	16.0	0	N/A	7.9
001	11.4	3.7	3.4	10.7
010	12.9	4.8	2.7	10.2
011	12.9	5.4	2.3	10.0
100	12.9	5.8	2.0	9.8
101	12.9	6.1	1.8	9.8
110	10.5	6.5	1.8	10.6
111	9.8	7.3	1.8	11.2

THIS DATA IS FOR ILLUSTRATIVE PURPOSES ONLY.

Figure 3. Typical high-speed input equalization curve.

multiple HDMP-3268s to reside on the same address and data buses. When CS is high, the HDMP-3268 does not accept data, and the HDMP-3268's data outputs are tri-stated. In broadcast write mode, (CH[6:0] set to '1111111'), all registers of the selected set (control or address) receive the same data value. This feature simplifies chip configuration upon power-up. By default, all registers are programmed to 0 at power-up provided V_{CC} comes up at the same time or after V_{DD}.

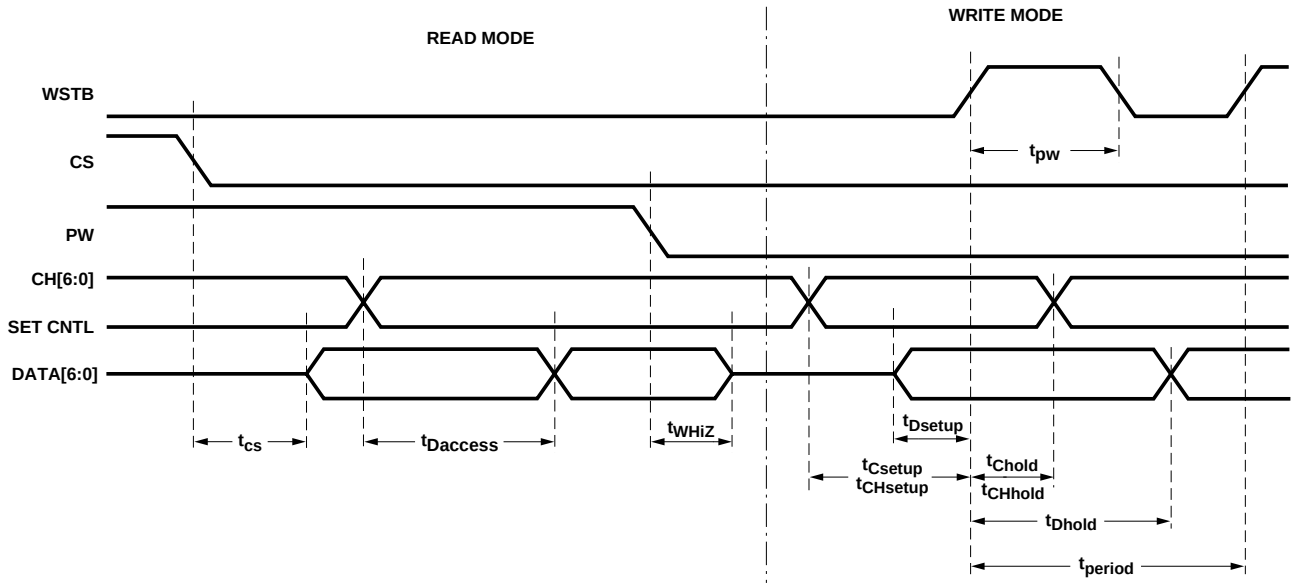


Figure 4. Timing diagram for accessing HDMP-3268 registers.

Table 1. HDMP-3268 Interface Timing Requirements
T_A = 0°C to T_C = 85°C, V_{CC} = V_{DD} = V_{CC}_DOUT = 2.35 V to 2.65 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{period}	Write Strobe Period	ns	15.2		
t_{pw}	Write Strobe Pulse Width	ns	3		0.6* t_{period}
$t_{rise/fall}$	Write Strobe Rise and Fall Times	ns			2
t_{Dsetup}	Data Setup Time	ns	2	1	
t_{Dhold}	Data Hold Time	ns	0.5	0	
$t_{CHsetup}$	Channel Setup Time	ns	8		
t_{CHhold}	Channel Hold Time	ns	1		
t_{Csetup}	Control Setup Time	ns	4	3	
t_{Chold}	Control Hold Time	ns	–0.7	–1.2	
t_{cs}	Chip Select to Data Out	ns		5	7.4
$t_{Daccess}$	Data Access Time	ns		10	13
t_{WHiZ}	Write Assert to High Z Time	ns		3	4

Control Register

The control register is used to program the input AC or DC coupling, input equalization, output amplitude and power on/off settings of each input and output of the crosspoint switch. To access the control register the control signal CNTL must be high. Table 2 gives the specific definition of each bit in the control register. Upon power-up, all bits of the control register are set to 0.

Table 2. HDMP-3268 Control Register Definition

Bit(s)	Name	Value	Definition
6:5	Output On/Off & Amplitude[1]	00	Output stage disabled (power off)
		01	Typical Vop[1] = 550 mV
		10	Typical Vop[1] = 800 mV
		11	Typical Vop[1] = 1050 mV
4:2	Equalization Amplitude	000	Input equalization disabled
		111	Maximum input equalization
1	Input On/Off	0	Input stage disabled (power off)
		1	Input stage active (power on)
0	AC/DC	0	DC input coupling
		1	AC input coupling

Note:

1. Output Peak-to-Peak Differential Voltage, Vop, is specified as DOUT+ minus DOUT-. This measurement is made using a repeating 1010 pattern with a 100 Ω termination resistor across the DOUT+ and DOUT- outputs. The swing doubles if there is no termination resistor.

Switch Matrix Configuration

The address registers are used to program the connectivity of the switch matrix. The address registers are accessed when the CNTL input is low. There are two independent banks of 68 address registers to allow one bank to be programmed while the other bank is controlling the switch matrix if desired. There is one Address0 register and one Address1 register per output channel. The address register selects the input to be connected to its output. Connecting a particular input to a particular output is done by setting CH[6:0] to the desired output channel. DATA[6:0] holds the channel number of the desired input channel. Table 3 summarizes the behavior of the USE and SET bits. See Figure 4 for the timing diagram for SET, and Figure 5 for the timing diagram for USE.

Table 3. USE/SET Truth Table

Use	Set	Address Register Use
0	0	Using Address0 Registers for switch control, Reading/Writing Address0 Registers
0	1	Using Address0 Registers for switch control, Reading/Writing Address1 Registers
1	0	Using Address1 Registers for switch control, Reading/Writing Address0 Registers
1	1	Using Address1 Registers for switch control, Reading/Writing Address1 Registers

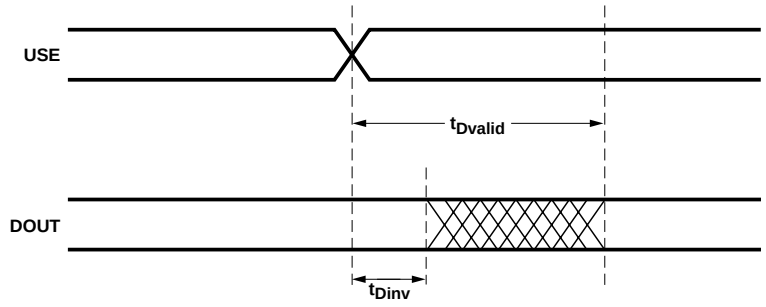


Figure 5. USE bit data valid/invalid timing diagram.

Table 4. USE Bit Timing
T_A = 0°C to T_C = 85°C, V_{CC} = V_{DD} = V_{CC}_DOUT = 2.35 V to 2.65 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_{Dvalid}	USE bit set to valid DOUT	ns			40
t_{Dinv}	USE bit set to DOUT invalid	ns	6		

Digital Interface I/O

Figure 6 shows simplified circuit diagrams of the digital input and output cells. The digital input cell is applicable to all data and control inputs of the HDMP-3268. The digital output cell used for the HDMP-3268's digital I/Os are designed to be compatible with either an SSTL_2 interface or with an LVTTL interface. The digital input cell has the option of providing an on-chip 50 Ω termination resistor. The 50 Ω termination is connected to the digital input when the TERM pin is high. When the HDMP-3268 is used with an SSTL_2 interface, the VREF output of the controlling chip should be connected to the VREFI pin on the HDMP-3268. This gives the best noise margin performance since the VREF output signal of the controlling chip should be centered with respect to its output swing. Alternatively, for best performance, the HDMP-3268's VREFO output, which provides an output voltage of approximately one half of the supply, should be connected to the VREFI pin of the controlling chip. A 0.1 µF bypass capacitor should also be connected at the VREFI pin.

For an LVTTL interface, the HDMP-3268 provides a reference voltage of nominally 1.4 V on the VREF14 pin. When the HDMP-3268 is used with a 3.3 V LVTTL system, its VREF14 pin should be connected to its VREFI pin. The nominal output impedance for the digital output is 25 Ω. Therefore, when connecting the HDMP-3268 unterminated for a distributed point-to-point topology, a 25 Ω resistor should be added in series with the data I/O lines to match 50 Ω traces on the PC board. For lumped circuit connections the 25 Ω series resistor is not necessary.

The HDMP-3268 has termination amplifiers built in for distributed multichip connections where the SSTL_2 I/Os need to be terminated. Note that a terminated connection consumes significant power, so terminations

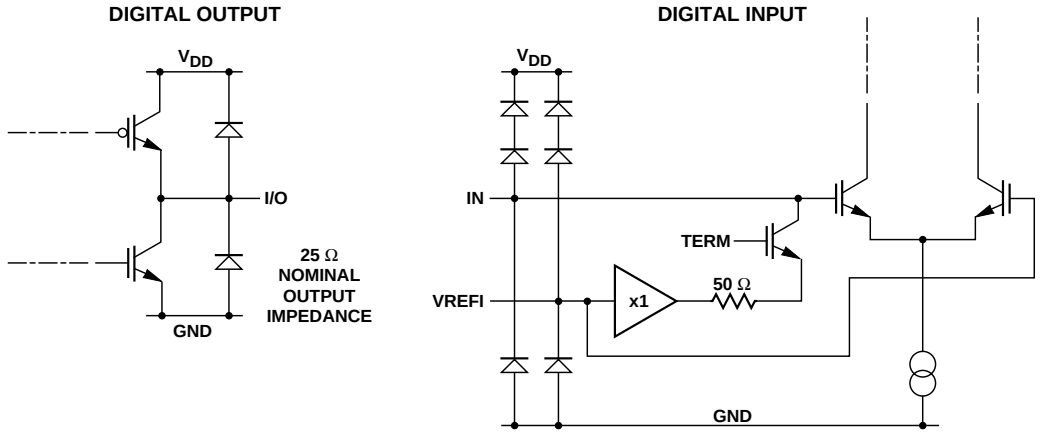


Figure 6. Digital I/O simplified circuit schematics.

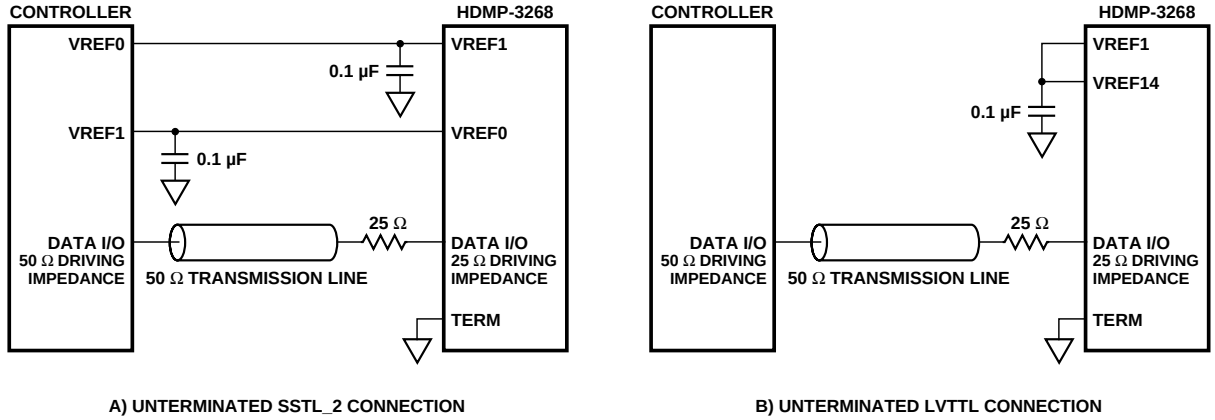


Figure 7. Unterminated digital I/O connections.

should only be used if necessary. When TERM is pulled high to VDD all low speed digital inputs and I/Os except TERM itself are terminated. Pins affected are WSTB, CH[6:0], CS, RW, DATA[6:0], CNTL, USE and SET. Since the transmission line is terminated at both ends, the driving impedance is 25 Ω. HDMP-3268s connected in the middle of the transmission line do not need to be terminated. Figure 8 shows a typical connection.

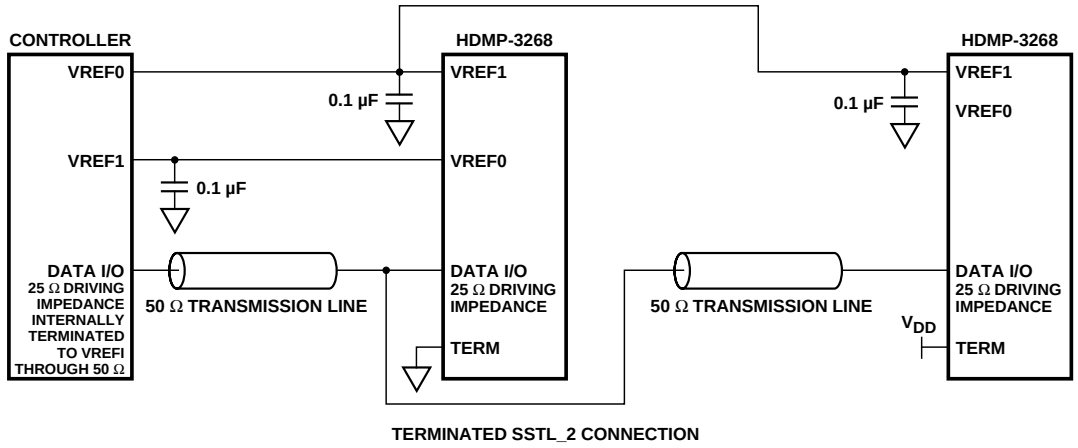


Figure 8. Terminated SSTL_2 connection.

Table 5. HDMP-3268 Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to the device.

Symbol	Parameter	Units	Min.	Max.
VDD	Logic Supply Voltage	V	-0.5	3.6 V
VCC	Switch Array Power Supply	V	-0.5	3.6 V
VCC_DOUT	High Speed Output Supply	V	-0.5	3.6 V
VIN	Input Voltage for WSTB, CH[6:0], CS, RW, DATA[6:0], CNTL	V	-0.5	VDD+1.25 V
VINHS	High Speed Input Voltage for DIN[0:67]+ and DIN[0:67]-	V	-0.5	VCC+0.5 V[1]
Tj	Junction Temperature	°C	0	+125
Tstg	Storage Temperature	°C	-55	+125
ESD	ESD Rating (HBM)	kV		2

Note:
1. VIN must remain less than or equal to the absolute maximum supply voltage of 3.6 V.

Table 6. HDMP-3268 Recommended Operating Conditions

Symbol	Parameter	Units	Min.	Typ.	Max.
VDD	Logic Supply Voltage	V	2.35	2.5	2.65
VCC	Switch Array Power Supply	V	2.35	2.5	2.65
VCC_DOUT	High Speed Output Supply	V	2.35	2.5	2.65
Ta	Ambient Temperature	°C	0	25	
Tc	Case Temperature	°C			85

Table 7. HDMP-3268 DC Electrical Specifications
T_A = 0°C to T_c=+85°C, VCC = VDD = VCC_DOUT =2.35 V to 2.65 V

Symbol	Parameter	Units	Min.	Typ.	Max.
VDD	Logic Supply Voltage	V	2.35	2.5	2.65
VCC	Switch Array Power Supply	V	2.35	2.5	2.65
VCC_DOUT	High Speed Output Supply	V	2.35	2.5	2.65
Pd[2]	Power Dissipation [TERM = 0]	W			13.5
Pd1[3]	Power Dissipation [TERM = 1]	W			15.5
VOH_DU	Digital Interface Unterminated Output High Voltage, IOH = -400 µA	V	2.2		VDD
VOL_DU	Digital Interface Unterminated Output Low Voltage Level, IOL = 1 mA	V	0		0.6
VOH_DT	Digital Interface Terminated Output High Voltage	V	VREFO + 0.38		VDD+ 0.3
VOL_DT	Digital Interface Terminated Output Low Voltage Level	V	-0.3		VREFO- 0.38
VIH_D (LVTTL)	Digital Interface Input High Voltage Level, guaranteed high signal, VREFI tied to VREF14	V	2		
VIL_D (LVTTL)	Digital Interface Input Low Voltage Level, guaranteed low signal, VREFI tied to VREF14	V			0.8
VIH_AC (SSTL_2)	Digital Interface Input AC High Voltage Level, guaranteed high signal, VREFI = 1.15 V to 1.35 V	V	VREFI+ 0.35		VDDQ+ 0.3[1]
VIL_AC (SSTL_2)	Digital Interface Input AC Low Voltage Level, guaranteed low signal, VREFI = 1.15 V to 1.35 V	V	-0.3		VREFI- 0.35
VIH_DC (SSTL_2)	Digital Interface Input DC High Voltage Level, guaranteed high signal, VREFI = 1.15 V to 1.35 V	V	VREFI+ 0.18		VDDQ+ 0.3[1]
VIL_DC (SSTL_2)	Digital Interface Input DC Low Voltage Level, guaranteed low signal, VREFI = 1.15 V to 1.35 V	V	-0.3		VREFI- 0.18
I IH_DU	Digital Interface Unterminated Input High Current, VIN = 2.4 V, VCC=2.5 V	µA	-15		15
I IL_DU	Digital Interface Unterminated Input Low Current, VIN = 0.4 V, VCC=2.5 V	µA	-15		15
IIH_DT	Digital Interface Terminated Input High Current, VIN = 2.4 V, VCC=2.5 V	mA		-12.5	
I IL_DT	Digital Interface Terminated Input Low Current, VIN = 0.4 V, VCC=2.5 V	mA		12.5	
VREF14	LVTTL Reference Output, T_A = 25°C	V		1.4	
VREFI	SSTL_2 Reference Input, T_A = 25°C	V	1.15	1.25	1.35
VREFO	SSTL_2 Reference Output, T_A = 25°C	V	1.15	1.25	1.35

Notes:
1. VDDQ refers to the SSTL_2 power supply of the driving device.
2. Power Dissipation measurement was taken with a toggling pattern of 50 MHz applied to the high-speed input channels at 50% duty cycle. All inputs and outputs are turned on.
3. Power Dissipation measurement was taken with Input logic '0' applied to all control pins with a toggling pattern of 50 MHz applied to the high-speed input channels at 50% duty cycle. All inputs and outputs are turned on.

Table 7.1. HDMP-3268 DC Electrical Specifications for Individual Power Supply Current

T_A = 25°C , VCC = VDD = VCC_DOUT = 2.5 V

Symbol	Units	min_amp[1] (Typ)	mid_amp[2] (Typ)	max_amp[3] (Typ)
Icc[4]	A	1.5	1.5	1.5
Icc_dout[4]	A	1.5	1.9	2.3
Idd (TERM=0)[4]	A	0.0025	0.0025	0.0025
Idd (TERM=1)[5]	A	0.3	0.3	0.3

Notes:

1. Current drawn from power supply, minimum output amplitude (mode 01).
2. Current drawn from power supply, mid output amplitude (mode 10).
3. Current drawn from power supply, maximum output amplitude (mode 11).
4. Current measurement was taken with a toggling pattern at 50 MHz is applied into the high-speed input channels at 50% duty cycle. All inputs and outputs are turned on.
5. Current measurement was taken with input logic '0' applied to all control pins and a toggling pattern at 50 MHz is applied into the high-speed input channels at 50% duty cycle. All inputs and outputs are turned on.

Table 7.2. HDMP-3268 DC Electrical Specifications for Current Drawn for Individual Input/Output Channel Turned on/off

T_A = 25°C , VCC = VDD = VCC_DOUT = 2.5 V

Symbol	Parameters	Units	Typical
Din_ICC[1,2]	Current drawn when 1 input is turned on	mA	16.0
Dout_ICC[1,3]	Current drawn for power supply VCC when 1 output is turned on	mA	7.4
Dout_ICC_DOUT[1,3]	Current drawn for power supply VCC_DOUT when 1 output is turned on	mA	34.0

Notes:

1. Current measurement was carried out using a toggling pattern at maximum amplitude with 50% duty cycle
2. For input channels, the number of input channels turned on/off affects only the power supply current for VCC.
3. For output channels, the number of output channels turned on/off affects only the power supply currents for VCC and VCC_DOUT.

Table 8. HDMP-3268 AC Electrical Specifications

T_A = 0°C to T_C = +85°C, VCC = VDD = VCC_DOUT = 2.35 V to 2.65 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$t_{rd, DOUT}$	DOUT Differential Rise Time	ps		150	
$t_{fd, DOUT}$	DOUT Differential Fall Time	ps		150	
$V_{IP, DIN}$	DIN Input Peak-To-Peak Differential Voltage	mV	200		1600
$V_{OP, DOUT01}$[1]	DOUT Output Pk-Pk Diff. Voltage at minimum amplitude setting (Amplitude code=01) with 100 Ohm differential termination	mV		550	
$V_{OP, DOUT10}$[1]	DOUT Output Pk-Pk Diff. Voltage at mid-range amplitude setting (Amplitude code=10) with 100 Ohm differential termination	mV		800	
$V_{OP, DOUT11}$[1]	DOUT Output Pk-Pk Diff. Voltage at maximum amplitude setting (Amplitude code=11) with 100 Ohm differential termination	mV		1050	
t_{Prop}	Propagation Delay Time (Delay for data to travel from High-speed input to High-speed output)	ns	0.25		0.95
$t_{skew\ part}$	Skew between DOUT channels on a single crosspoint part	ps			350
RJ (Single)[3]	Random Jitter at DOUT[0:67], the High Speed Electrical Data Port, specified as one sigma deviation of the 50% crossing point (RMS). Differential output measurement. Single channel input to single channel output.	ps		2	
DJ (Single)[3]	Deterministic Jitter at DOUT[0:67], the High Speed Electrical Data Port (pk-pk). Differential output measurement Single channel input to single channel output.	ps		30	
TJ (Single)[3]	Total jitter for 1E-12 BER (DJ + 14RJ). Differential output measurement. Single channel input to single channel output.	ps		58	
RJ (Broadcast)[3]	Random Jitter at DOUT[0:67], the High Speed Electrical Data Port, specified as one sigma deviation of the 50% crossing point (RMS). Differential output measurement. Single channel input to all channels output.	ps		2.5	
DJ (Broadcast)[3]	Deterministic Jitter at DOUT[0:67], the High Speed Electrical Data Port (pk-pk). Differential output measurement. Single channel input to all channels output.	ps		40	
TJ (Broadcast)[3]	Total jitter for 1E-12 BER (DJ + 14RJ). Differential output measurement. Single channel input to all channels output.	ps		75	
Drate	Guaranteed Operating Rate	Gbit/sec	Note 2		3.2

Notes:

1. Output Peak-to-Peak Differential Voltage specified as DOUT+ minus DOUT-. This measurement is made using a repeating 1010 pattern. Vop amplitude can be adjusted with the program register.
2. Minimum data rate depends on the value of AC input coupling capacitance and input resistance which is 100 Ohms between the positive and negative inputs.
3. Jitter measurement was carried out using a 3.3G BERT with a base jitter of 19ps for Deterministic Jitter and 0.97ps for Random Jitter. For eye diagrams, please see application notes. Jitter Measurement is taken using a K28.5 pattern at 3.2Gbaud data rate.

Table 9. HDMP-3268 Thermal Characteristics[5]

T_A = 25°C , VCC = VDD = VCC_DOUT = 2.5 V

Symbol	Parameter	Units	Typ.
Ψ_{JT}[2]	Thermal characterization parameter: Junction to case.	^{0}C/W	0.70
Ψ_{JB}[3]	Thermal characterization parameter: Junction to board.	^{0}C/W	4.90
θ_{JC}[4]	Thermal resistance: Junction to case	^{0}C/W	0.65
θ_{JA}[1]	Thermal resistance: Junction to ambient.	^{0}C/W	11.1

Note: Based on independent package testing done by Agilent.
Refer to HDMP-3268 thermal management application note.

1. θ_{JA} is based on thermal measurement in still air environment at 25°C on a standard 5 x 5" FR4 PCB as specified in EIA/JESD 51-9.
2. Ψ_{JT} is used to determine the actual junction temperature in a given application, using the following equation:
   $T_J = \Psi_{JT} \times P_D + T_T$, where T_T is the measured temperature on top center of the package and P_D is the power being dissipated.
3. Ψ_{JB} is used to determine the actual junction temperature in a given application, using the following equation:
   $T_J = \Psi_{JB} \times P_D + T_B$, where T_B is the measured board temperature along centerline at edge of the package and P_D is the power being dissipated.
4. θ_{JC} data is relevant for packages used with external heat sink.
5. Physical tests were carried out using 13.5 W as the power dissipation of the device.

Table 10. HDMP-3268 I/O Type Definitions

I/O Type	Definition
HS_OUT	Differential high speed output, LV PECL compatible
HS_IN	Differential high speed input, LV PECL compatible
S	Power supply or ground
CTL_IN	Control logic input, LVTTL and SSTL_2 compatible
CTL_I/O	Control logic input/output, LVTTL and SSTL_2 compatible
REFO	Reference output voltage for LVTTL and SSTL_2 I/Os
REFI	Reference input voltage for LVTTL and SSTL_2 I/Os

Table 11. HDMP-3268 Pin Definitions

Name	Type	Signal
DIN[0:67]	HS_IN	**High Speed Data Channel Inputs.** Data channel inputs accepting 3.2 Gbit/sec data for rerouting to high speed outputs DOUT[0:67]+ and DOUT[0:67]-. Routing is controlled by the Address Registers.
DOUT[0:67]	HS_OUT	**High Speed Data Outputs.** High-speed data channel outputs. Routing is controlled by the Address Registers.
CNTL	CTL_IN	**Control Input.** Determines whether DATA[6:0] inputs are interpreted as addresses or control (input equalization and power off) settings. When CNTL is low the DATA[6:0] inputs are interpreted as addresses. When CNTL is high the DATA[6:0] inputs are interpreted as input equalization, amplitude, and power off settings.
DATA[6:0]	CTL_I/O	**Data Inputs and Outputs.** Address, input equalization, output amplitude and power off settings. Interpretation is determined by the state of the CNTL input. The direction of the data (input or output) is determined by the RW pin. DATA [6] is MSB.
CH[6:0]	CTL_IN	**Channel Select.** Selects one of the 68 control or address registers from which data is to be written or read. CH [6] is MSB.
CS	CTL_IN	**Chip Select.** When CS is low the crosspoint switch chip is selected and the RW and DATA pins are enabled. This pin can be used to allow multiple crosspoint switches to operate on a shared bus.
RW	CTL_IN	**Read Write.** This input is used to control whether address or program data is being written or read from the internal address and control registers. RW is 1 for Read mode and 0 for Write mode.
WSTB	CTL_IN	**Write Strobe.** Input write strobe for writing DATA inputs to the internal address and control register. Data is latched into the internal registers on the rising edge of WSTB.
GND	S	**Ground.** Normally 0 volts.
VDD	S	**Logic Supply Voltage.** Normally 2.5 volts.
VCC	S	**Switch Array Power Supply.** Normally 2.5 volts. Used for internal PECL logic. It should be isolated from CMOS supply.
VCC_DOUT	S	**High Speed Output Supply.** Normally 2.5 volts. Used only for the last stage of the high-speed transmitter output cell. VCC_DOUT should be well bypassed to a ground plane.
TERM	CTL_IN	**Termination.** Set to high to terminate SSTL_2 I/O lines.
USE	CTL_IN	**Use.** Selects address register bank to use to configure the switch.
SET	CTL_IN	**Set.** Determines which address register is accessed by the CTL_I/O interface.
VREF14	REFO	**LVTTL Voltage Reference Output.** Nominally 1.4 V. Sets input threshold when logic inputs are connected to LVTTL signals
VREFI	REFI	**Voltage Reference Input.** Used with I-SSTL_2 inputs to the HDMP-3268.
VREFO	REFO	**Voltage Reference Output.** Used with O-SSTL_2 outputs from the HDMP-3268.

Table 12. HDMP-3268 Package Specifications

400 Ball 37.5 mm x 37.5 mm HPBGA

Parameter	Units	Typ.
Package Size	mm	37.5x37.5
Ball Matrix	mm	29x29
Ball Layout		4 rows
Ball Pitch	mm	1.27
Package Thickness	mm	2.93

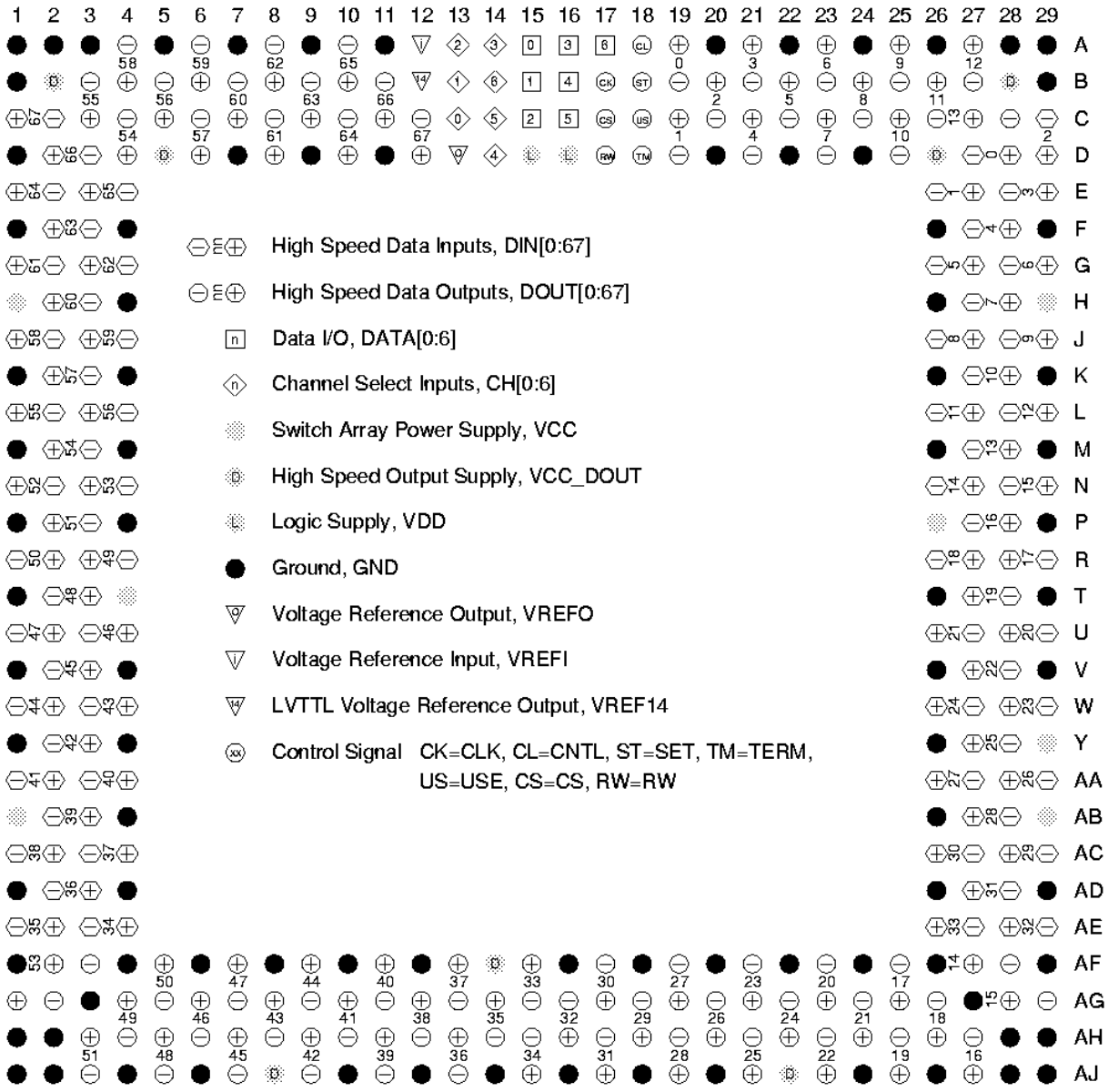


Figure 9. HDMP-3268 pin locations.
Note that the view is through the top of the package. If looking at the package bottom, ball A1 is at the upper right.

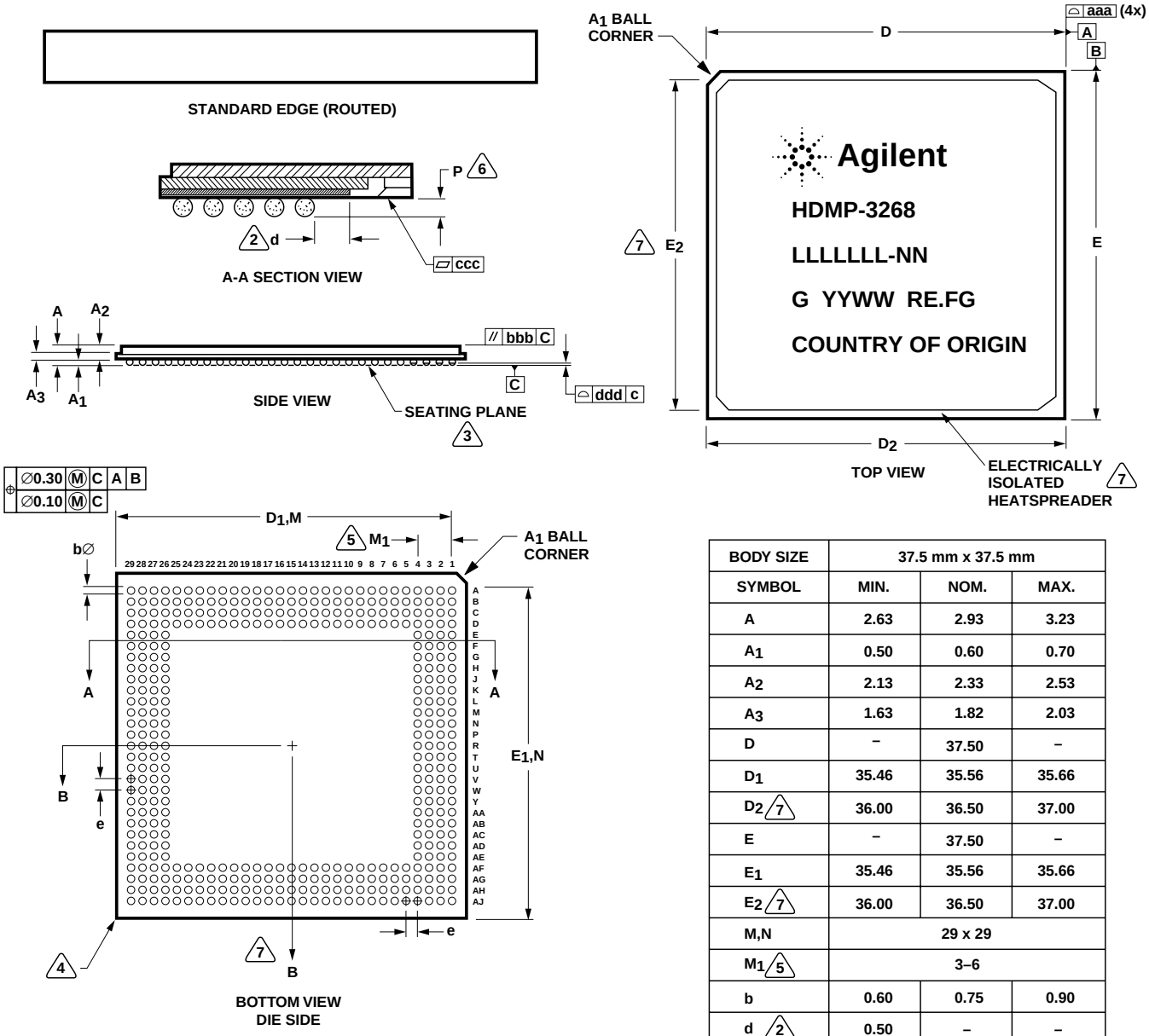
Table 13. HDMP-3268 Detailed Pin Assignment

A1	GND	B22	DOUT[5]+	D14	CH[4]	J3	DIN[59]+
A2	GND	B23	DOUT[6]-	D15	VDD	J4	DIN[59]-
A3	GND	B24	DOUT[8]+	D16	VDD	J26	DIN[8]-
A4	DOUT[58]-	B25	DOUT[9]-	D17	RW	J27	DIN[8]+
A5	GND	B26	DOUT[11]+	D18	TERM	J28	DIN[9]-
A6	DOUT[59]-	B27	DOUT[12]-	D19	DOUT[1]-	J29	DIN[9]+
A7	GND	B28	VCC_DOUT	D20	GND	K1	GND
A8	DOUT[62]-	B29	GND	D21	DOUT[4]-	K2	DIN[57]+
A9	GND	C1	DIN[67]+	D22	GND	K3	DIN[57]-
A10	DOUT[65]-	C2	DIN[67]-	D23	DOUT[7]-	K4	GND
A11	GND	C3	DOUT[55]+	D24	GND	K26	GND
A12	VREFI	C4	DOUT[54]-	D25	DOUT[10]-	K27	DIN[10]-
A13	CH[2]	C5	DOUT[56]+	D26	VCC_DOUT	K28	DIN[10]+
A14	CH[3]	C6	DOUT[57]-	D27	DIN[0]-	K29	GND
A15	DATA[0]	C7	DOUT[60]+	D28	DIN[0]+	L1	DIN[55]+
A16	DATA[3]	C8	DOUT[61]-	D29	DIN[2]+	L2	DIN[55]-
A17	DATA[6]	C9	DOUT[63]+	E1	DIN[64]+	L3	DIN[56]+
A18	CNTL	C10	DOUT[64]-	E2	DIN[64]-	L4	DIN[56]-
A19	DOUT[0]+	C11	DOUT[66]+	E3	DIN[65]+	L26	DIN[11]-
A20	GND	C12	DOUT[67]-	E4	DIN[65]-	L27	DIN[11]+
A21	DOUT[3]+	C13	CH[0]	E26	DIN[1]-	L28	DIN[12]-
A22	GND	C14	CH[5]	E27	DIN[1]+	L29	DIN[12]+
A23	DOUT[6]+	C15	DATA[2]	E28	DIN[3]-	M1	GND
A24	GND	C16	DATA[5]	E29	DIN[3]+	M2	DIN[54]+
A25	DOUT[9]+	C17	CS	F1	GND	M3	DIN[54]-
A26	GND	C18	USE	F2	DIN[63]+	M4	GND
A27	DOUT[12]+	C19	DOUT[1]+	F3	DIN[63]-	M26	GND
A28	GND	C20	DOUT[2]-	F4	GND	M27	DIN[13]-
A29	GND	C21	DOUT[4]+	F26	GND	M28	DIN[13]+
B1	GND	C22	DOUT[5]-	F27	DIN[4]-	M29	GND
B2	VCC_DOUT	C23	DOUT[7]+	F28	DIN[4]+	N1	DIN[52]+
B3	DOUT[55]-	C24	DOUT[8]-	F29	GND	N2	DIN[52]-
B4	DOUT[58]+	C25	DOUT[10]+	G1	DIN[61]+	N3	DIN[53]+
B5	DOUT[56]-	C26	DOUT[11]-	G2	DIN[61]-	N4	DIN[53]-
B6	DOUT[59]+	C27	DOUT[13]+	G3	DIN[62]+	N26	DIN[14]-
B7	DOUT[60]-	C28	DOUT[13]-	G4	DIN[62]-	N27	DIN[14]+
B8	DOUT[62]+	C29	DIN[2]-	G26	DIN[5]-	N28	DIN[15]-
B9	DOUT[63]-	D1	GND	G27	DIN[5]+	N29	DIN[15]+
B10	DOUT[65]+	D2	DIN[66]+	G28	DIN[6]-	P1	GND
B11	DOUT[66]-	D3	DIN[66]-	G29	DIN[6]+	P2	DIN[51]+
B12	VREF14	D4	DOUT[54]+	H1	VCC	P3	DIN[51]-
B13	CH[1]	D5	VCC_DOUT	H2	DIN[60]+	P4	GND
B14	CH[6]	D6	DOUT[57]+	H3	DIN[60]-	P26	VCC
B15	DATA[1]	D7	GND	H4	GND	P27	DIN[16]-
B16	DATA[4]	D8	DOUT[61]+	H26	GND	P28	DIN[16]+
B17	WSTB	D9	GND	H27	DIN[7]-	P29	GND
B18	SET	D10	DOUT[64]+	H28	DIN[7]+	R1	DIN[50]-
B19	DOUT[0]-	D11	GND	H29	VCC	R2	DIN[50]+
B20	DOUT[2]+	D12	DOUT[67]+	J1	DIN[58]+	R3	DIN[49]+
B21	DOUT[3]-	D13	VREFO	J2	DIN[58]-	R4	DIN[49]-

Table 13. HDMP-3268 Detailed Pin Assignment (continued)

R26	DIN[18]-	AA28	DIN[26]+	AF17	DOUT[30]-	AH9	DOUT[42]+
R27	DIN[18]+	AA29	DIN[26]-	AF18	GND	AH10	DOUT[41]-
R28	DIN[17]+	AB1	VCC	AF19	DOUT[27]-	AH11	DOUT[39]+
R29	DIN[17]-	AB2	DIN[39]-	AF20	GND	AH12	DOUT[38]-
T1	GND	AB3	DIN[39]+	AF21	DOUT[23]-	AH13	DOUT[36]+
T2	DIN[48]-	AB4	GND	AF22	GND	AH14	DOUT[35]-
T3	DIN[48]+	AB26	GND	AF23	DOUT[20]-	AH15	DOUT[34]-
T4	VCC	AB27	DIN[28]+	AF24	GND	AH16	DOUT[32]+
T26	GND	AB28	DIN[28]-	AF25	DOUT[17]-	AH17	DOUT[31]-
T27	DIN[19]+	AB29	VCC	AF26	GND	AH18	DOUT[29]+
T28	DIN[19]-	AC1	DIN[38]-	AF27	DOUT[14]+	AH19	DOUT[28]-
T29	GND	AC2	DIN[38]+	AF28	DOUT[14]-	AH20	DOUT[26]+
U1	DIN[47]-	AC3	DIN[37]-	AF29	GND	AH21	DOUT[25]-
U2	DIN[47]+	AC4	DIN[37]+	AG1	DOUT[52]+	AH22	DOUT[24]+
U3	DIN[46]-	AC26	DIN[30]+	AG2	DOUT[52]-	AH23	DOUT[22]-
U4	DIN[46]+	AC27	DIN[30]-	AG3	GND	AH24	DOUT[21]+
U26	DIN[21]+	AC28	DIN[29]+	AG4	DOUT[49]+	AH25	DOUT[19]-
U27	DIN[21]-	AC29	DIN[29]-	AG5	DOUT[50]-	AH26	DOUT[18]+
U28	DIN[20]+	AD1	GND	AG6	DOUT[46]+	AH27	DOUT[16]-
U29	DIN[20]-	AD2	DIN[36]-	AG7	DOUT[47]-	AH28	GND
V1	GND	AD3	DIN[36]+	AG8	DOUT[43]+	AH29	GND
V2	DIN[45]-	AD4	GND	AG9	DOUT[44]-	AJ1	GND
V3	DIN[45]+	AD26	GND	AG10	DOUT[41]+	AJ2	GND
V4	GND	AD27	DIN[31]+	AG11	DOUT[40]-	AJ3	DOUT[51]-
V26	GND	AD28	DIN[31]-	AG12	DOUT[38]+	AJ4	GND
V27	DIN[22]+	AD29	GND	AG13	DOUT[37]-	AJ5	DOUT[48]-
V28	DIN[22]-	AE1	DIN[35]-	AG14	DOUT[35]+	AJ6	GND
V29	GND	AE2	DIN[35]+	AG15	DOUT[33]-	AJ7	DOUT[45]-
W1	DIN[44]-	AE3	DIN[34]-	AG16	DOUT[32]-	AJ8	VCC_DOUT
W2	DIN[44]+	AE4	DIN[34]+	AG17	DOUT[30]+	AJ9	DOUT[42]-
W3	DIN[43]-	AE26	DIN[33]+	AG18	DOUT[29]-	AJ10	GND
W4	DIN[43]+	AE27	DIN[33]-	AG19	DOUT[27]+	AJ11	DOUT[39]-
W26	DIN[24]+	AE28	DIN[32]+	AG20	DOUT[26]-	AJ12	GND
W27	DIN[24]-	AE29	DIN[32]-	AG21	DOUT[23]+	AJ13	DOUT[36]-
W28	DIN[23]+	AF1	GND	AG22	DOUT[24]-	AJ14	GND
W29	DIN[23]-	AF2	DOUT[53]+	AG23	DOUT[20]+	AJ15	DOUT[34]+
Y1	GND	AF3	DOUT[53]-	AG24	DOUT[21]-	AJ16	GND
Y2	DIN[42]-	AF4	GND	AG25	DOUT[17]+	AJ17	DOUT[31]+
Y3	DIN[42]+	AF5	DOUT[50]+	AG26	DOUT[18]-	AJ18	GND
Y4	GND	AF6	GND	AG27	GND	AJ19	DOUT[28]+
Y26	GND	AF7	DOUT[47]+	AG28	DOUT[15]+	AJ20	GND
Y27	DIN[25]+	AF8	GND	AG29	DOUT[15]-	AJ21	DOUT[25]+
Y28	DIN[25]-	AF9	DOUT[44]+	AH1	GND	AJ22	VCC_DOUT
Y29	VCC	AF10	GND	AH2	GND	AJ23	DOUT[22]+
AA1	DIN[41]-	AF11	DOUT[40]+	AH3	DOUT[51]+	AJ24	GND
AA2	DIN[41]+	AF12	GND	AH4	DOUT[49]-	AJ25	DOUT[19]+
AA3	DIN[40]-	AF13	DOUT[37]+	AH5	DOUT[48]+	AJ26	GND
AA4	DIN[40]+	AF14	VCC_DOUT	AH6	DOUT[46]-	AJ27	DOUT[16]+
AA26	DIN[27]+	AF15	DOUT[33]+	AH7	DOUT[45]+	AJ28	GND
AA27	DIN[27]-	AF16	GND	AH8	DOUT[43]-	AJ29	GND

Package Dimensions



BODY SIZE	37.5 mm x 37.5 mm		
SYMBOL	MIN.	NOM.	MAX.
A	2.63	2.93	3.23
A_1	0.50	0.60	0.70
A_2	2.13	2.33	2.53
A_3	1.63	1.82	2.03
D	–	37.50	–
D_1	35.46	35.56	35.66
D_2 7	36.00	36.50	37.00
E	–	37.50	–
E_1	35.46	35.56	35.66
E_2 7	36.00	36.50	37.00
M,N	29 x 29		
M_1 5	3–6		
b	0.60	0.75	0.90
d 2	0.50	–	–
e	1.27		
aaa	–	–	0.20
bbb	–	–	0.25
ccc	–	–	0.20
ddd	–	–	0.20
P 6	0.20	–	–

NOTES: UNLESS OTHERWISE SPECIFIED

1 ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

2 DIMENSION "d" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

3 PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.

4 SHAPE AT CORNER.  SINGLE FORM

5 NUMBER OF ROWS IN FROM EDGE TO CENTER.

6 SEATING PLANE CLEARANCE: MINIMUM HEIGHT OF ENCAPSULANT ABOVE SEATING PLANE.

7 D_2 AND E_2 SPECIFY THE STANDARD ELECTRICALLY ISOLATED HEATSPREADER SIZE. SEE HEATSPREADER OPTIONS SHEET 1 FOR OPTIMAL SIZES.

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