Integrated Device Technology, Inc.

256KB AND 512KB SECONDARY CACHE MODULES FOR THE PowerPC™

IDT7MPV6253
IDT7MPV6255/56

FEATURES

- For CHRP based PowerPC™ systems.
- Asynchronous and pipelined burst SRAM options in the same module pinout
- Low-cost, low-profile card edge module with 178 leads
- Uses Burndy Computerbus™ connector, part number ELF182KSC-3Z50
- Operates with external PowerPC CPU speeds up to 66MHz
- Separate 5V (±5%) and 3.3V (+10/-5%) power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Presence Detect output pins allow the system to determine the particular cache configuration.

DESCRIPTION

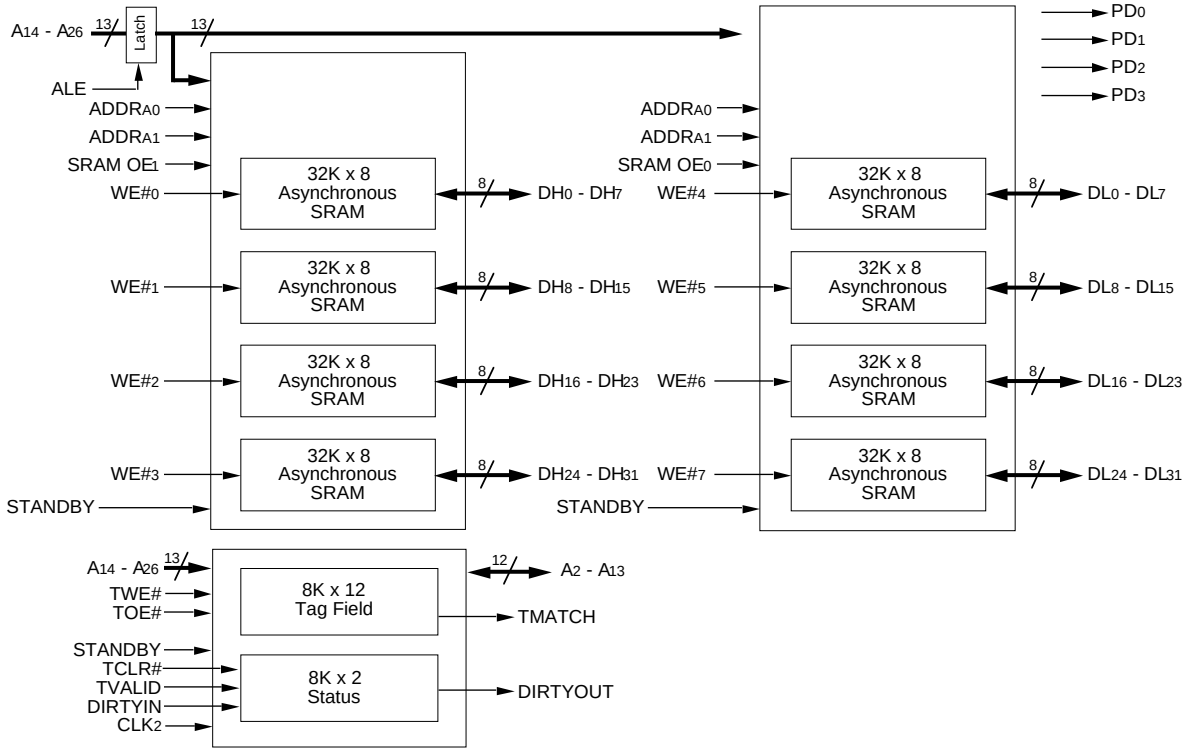
The IDT7MPV6253/55/56 modules belong to a family of secondary caches intended for use with PowerPC CPU-based systems. The IDT7MPV6253 uses IDT's 71V256 32K x 8 asynchronous static RAMs and the IDT7MPV6255/56 use IDT's 71V432 32K x 32 pipelined synchronous burst static RAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. In addition, each of the modules uses the IDT 71216 16K x 15 Cache-Tag static RAM and IDT FCT logic. Extremely high speeds are achieved using IDT's high-reliability, low cost CMOS technology.

The low profile card edge package allows 178 signal leads to be placed on a package 5.06" long, a maximum of 0.250" thick and a maximum of 1.08" tall. The module space savings versus discrete components allows the OEM to design additional functions onto the system or to shrink the size of the motherboard for reduced cost.

All inputs and outputs are LVTTL-compatible, and operate from separate 5V (±5%) and 3.3V (+10/-5%) power supplies. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM

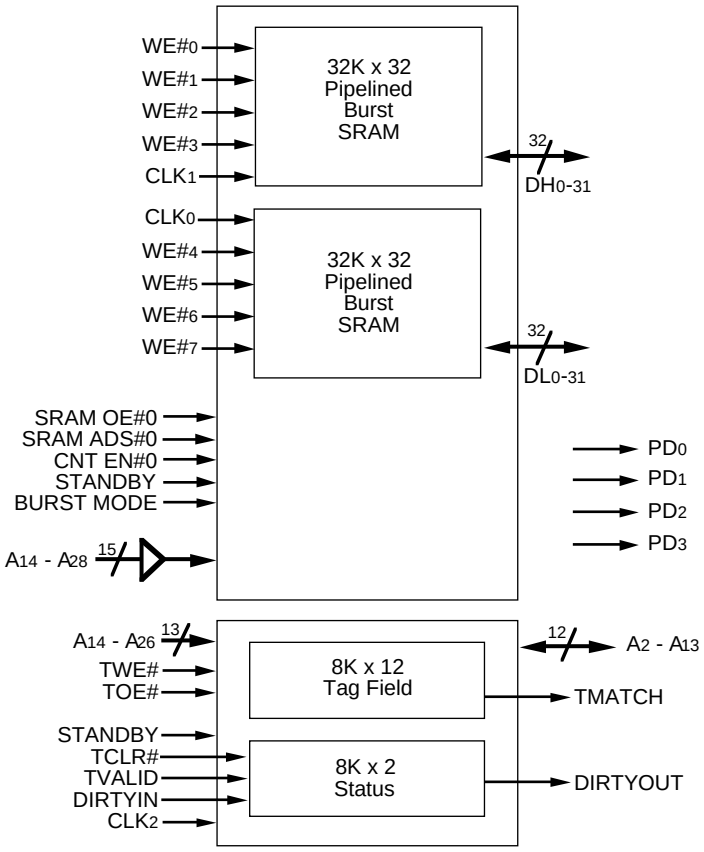
IDT7MPV6253 – 256KB ASYNCHRONOUS VERSION



drw 01

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6255 – 256KB PIPELINED BURST VERSION



drw 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.14	3.3	3.6	V
V_{CC5}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

tbl 01

NOTE:
1. V_{IL} = –1.0V for pulse width less than 5ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Power Plane	Ambient Temperature	GND	V_{CC}
V_{CC3}	0°C to +70°C	0V	3.3V +10/-5%
V_{CC5}	0°C to +70°C	0V	5.0V ± 5%

tbl 02

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

tbl 03

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

SRAM ACCESS TIMES

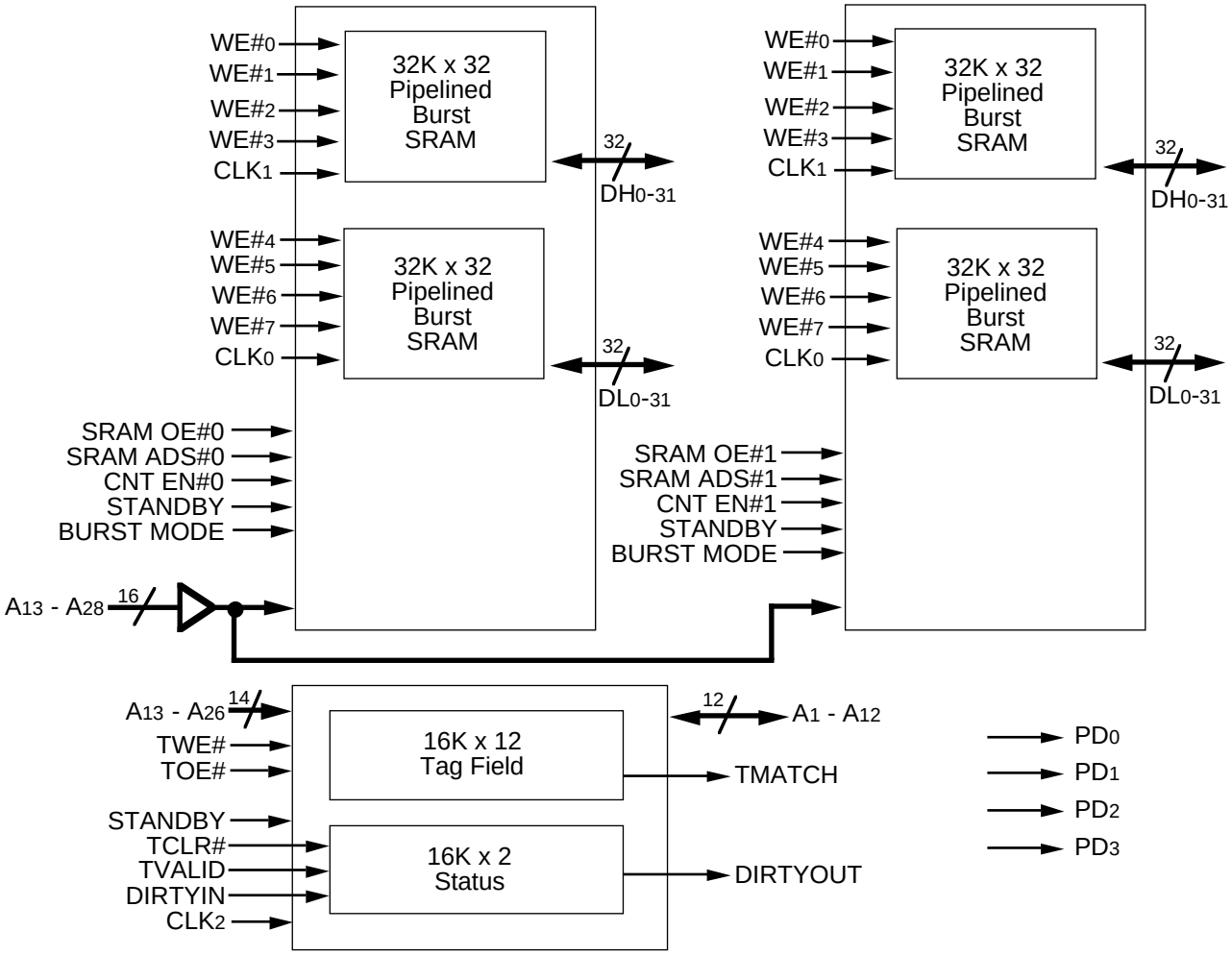
Module Speed	Asych	Burst(1)	Tag
66MHz	15ns	8.5ns	10ns

tbl 04

NOTE:
1. Burst SRAMs are measured by Clock to Data Out (t_{CD}).

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6256 – 512KB PIPELINED BURST VERSION



drw 03

CAPACITANCE (IDT7MPV6253)(1)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN1}	Input Capacitance (Address)	V_{IN} = 0V	15	pF
C_{IN2}	Input Capacitance ($ADDR_{0-1}$)	V_{IN} = 0V	25	pF
C_{IN3}	Input Capacitance (OE#)	V_{IN} = 0V	45	pF
C_{IN4}	Input Capacitance (WE#, TWE#)	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	10	pF

tbl 05

NOTES:
1. These parameters are guaranteed by design but not tested.

CAPACITANCE (IDT7MPV6255/56)(1)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN1}	Input Capacitance (Address)	V_{IN} = 0V	20	pF
C_{IN2}	Input Capacitance ($ADDR_{0-1}$)	V_{IN} = 0V	—	pF
C_{IN3}	Input Capacitance (OE#)	V_{IN} = 0V	15	pF
C_{IN4}	Input Capacitance (WE#, TWE#)	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	10/20	pF

tbl 06

NOTES:
1. These parameters are guaranteed by design but not tested.

PIN CONFIGURATION(1)

GND	90	1	GND
PD1	91	2	PD0
PD3	92	3	PD2
DH31	93	4	DH30
DH29	94	5	DH28
DH27	95	6	DH26
DH25	96	7	DH24
VCC3	97	8	VCC3
SRAM WE3	98	9	DP3 (1)
DH23	99	10	DH22
DH21	100	11	DH20
DH18	101	12	DH19
GND	102	13	GND
DH16	103	14	DH17
SRAM WE2	104	15	DP2 (1)
DH14	105	16	DH15
DH13	106	17	DH12
VCC5	107	18	VCC5
DH10	108	19	DH11
DH8	109	20	DH9
SRAM WE1	110	21	DP1 (1)
DH6	111	22	DH7
VCC3	112	23	VCC3
DH4	113	24	DH5
GND	114	25	DH3
CLK0	115	26	DH2
GND	116	27	DH0
DH1	117	28	DP0 (1)
SRAM WE0	118	29	GND
DL31	119	30	CLK1
DL30	120	31	GND
GND	121	32	DL28
DL29	122	33	DL26
DL27	123	34	DL24
DL25	124	35	DP7 (1)
VCC5	125	36	VCC5
SRAM WE7	126	37	DL22
DL23	127	38	DL20
DL21	128	39	DL18
DL19	129	40	DL16
GND	130	41	GND
DL17	131	42	DP6 (1)
SRAM WE6	132	43	DL14
DL15	133	44	DL12
DL13	134	45	DL11
GND	135	46	GND
DL10	136	47	DL9
DL8	137	48	DP5 (1)
SRAM WE5	138	49	DL7
DL6	139	50	DL4
VCC3	140	51	VCC3
DL5	141	52	DL3
DL2	142	53	DL1
GND	143	54	DL0
(1) CLK3	144	55	GND
GND	145	56	CLK2 (TAG)
(1) CLK4	146	57	GND
GND	147	58	DP4 (1)
SRAM WE4	148	59	SRAM OE0
(3,4) SRAM ALE	149	60	SRAM OE1 (3)
VCC3	150	61	VCC3
(3,4) ADDR1	151	62	ADDR0 (3,4)
(1) RSVD	152	63	RSVD (1)
(2) SRAM CNT EN0	153	64	SRAM ADS0 (2)
(2,3) SRAM CNT EN1	154	65	SRAM ADS1 (2,3)
A27	155	66	A28
A24	156	67	A26
A22	167	68	A25
A20	158	69	A23
GND	159	70	GND
A18	160	71	A21
A16	161	72	A19
A15	162	73	A17
A14	163	74	A13
VCC3	164	75	VCC3
A10	165	76	A12
A8	166	77	A11
A6	167	78	A9
GND	168	79	GND
A4	169	80	A7
A2	170	81	A5
(2,3) A1	171	82	A3
BURST MODE	172	83	A0 (1)
VCC5	173	84	VCC5
TAG VALID	174	85	TAG CLR
TAG WE	175	86	TAG MATCH
STANDBY	176	87	TAG OE
DIRTYOUT	177	88	DIRTYIN
GND	178	89	GND

LOW PROFILE CARD EDGE MODULE
TOP VIEW

drw 04

PIN NAMES

A0 – A28	Address Inputs
ADDR0 - ADDR1	Address Inputs (Asynchronous SRAMs only)
CLK0 - CLK4	Clock Inputs
DH0 - DH31	High Order Cache Data
DL0 - DL31	Low Order Cache Data
PD0 – PD3	Presence Detect Pins
SRAM ADS0 - SRAM ADS1	SRAM Address Strobe
SRAM ALE	SRAM Address Latch Enable
SRAM CNT EN0 - SRAM CNT EN1	SRAM Control Enable
SRAM OE0 - SRAM OE1	SRAM Output Enable
SRAM WE0 - SRAM WE1	SRAM Write Enable
BURST MODE	Burst Mode: 0=Linear, 1=Interleaved
TAG CLR	Tag Clear
TAG MATCH	Tag Match
TAG VALID	Tag Valid
TAG OE	Tag Output Enable
TAG WE	Tag Write Enable
DIRTYIN	Dirty Input Bit
DIRTYOUT	Dirty Output Bit
STANDBY	Stand By Mode
VCC3	3.3 Volt Power Supply
VCC5	5 Volt Power Supply
GND	Ground
NC	No Connect
RSVD	Reserved

tbl 07

PRESENCE DETECT TABLE

PD3	PD2	PD1	PD0	Module
NC	NC	NC	NC	No cache present
NC	GND	GND	GND	IDT7MPV6253
GND	GND	NC	NC	IDT7MPV6255
GND	NC	NC	NC	IDT7MPV6256

tbl 08

NOTES:
1. These pins are NC (No Connect) on 7MPV6253/55/56.
2. These pins are NC on 7MPV6253.
3. These pins are NC on 7MPV5255.
4. These pins are NC on 7MPV6256.

DC ELECTRICAL CHARACTERISTICS

(V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%, T_A = 0°C to 70°C)

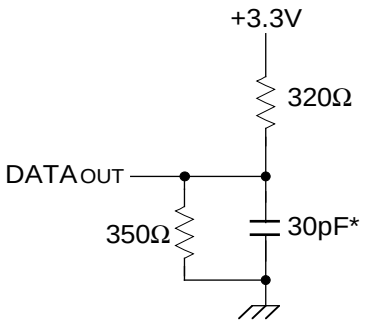
Symbol	Parameter	Test Condition	Min.	'53 Max.	'55 Max.	'56 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC5} = Max, V_{IN} = GND to V_{CC} V_{CC3} = Max	—	20	30	50	µA
$\|I_{LI}\|$	Input Leakage Current (Data and Control)	V_{CC5} = Max, V_{IN} = GND to V_{CC} V_{CC3} = Max	—	10	10	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC3}, V_{CC3} = Max.	—	10	10	20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC3} = Min.	—	0.4	0.4	0.4	V
V_{OH}	Output HighVoltage	I_{OH}= –4mA, V_{CC3} = Min.	2.4	—	—	—	V
I_{CC3}	Operating 3.3V Power Supply Current	V_{CC3} = Max., STANDBY ≤ V_{IL}, f = f_{MAX}, Outputs Open	—	1000	500	590	mA
I_{CC5}	Operating 5V Power Supply Current	V_{CC5} = Max., STANDBY ≤ V_{IL}, f = f_{MAX}, Outputs Open	—	290	290	290	mA
I_{SB3}	Standby 3.3V Power Supply Current	V_{CC3} = Max., STANDBY ≥ V_{IH}, f = f_{MAX}, Outputs Open	—	100	100	190	mA
I_{SB31}	Full Standby 3.3V Power Supply Current	V_{CC3} = Max., STANDBY ≥ V_{CC3} - 0.2V, f = 0, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC3} - 0.2V, Outputs Open	—	30	30	50	mA
I_{SB5}	Standby 5V Power Supply Current	V_{CC5} = Max., STANDBY ≥ V_{IH} f = f_{MAX}, Outputs Open	—	30	30	30	mA

tbl 09

AC TEST CONDITIONS – 3.3V POWER SUPPLY

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

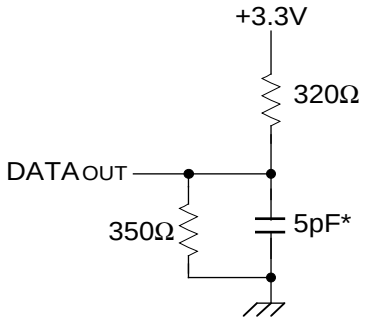
tbl 10



*including scope and jig capacitances

Figure 1. Output Load

drw 05

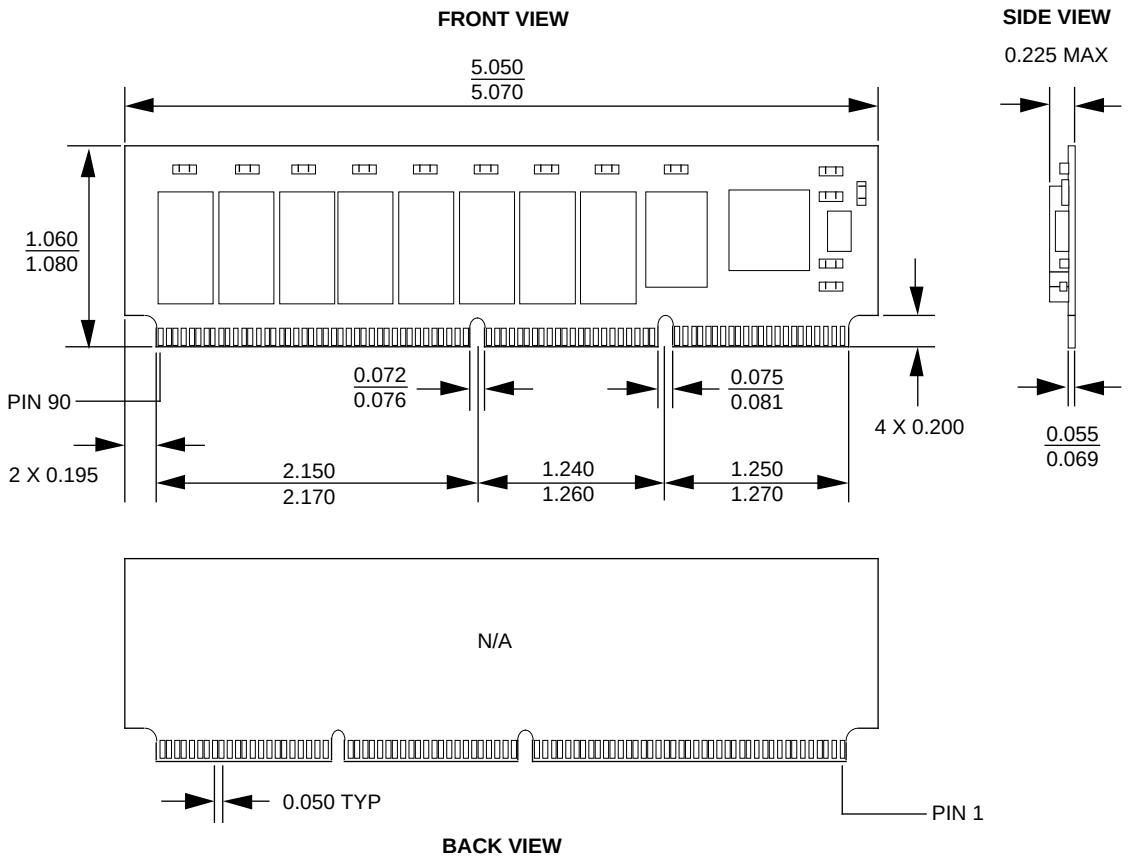


*including scope and jig capacitances

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

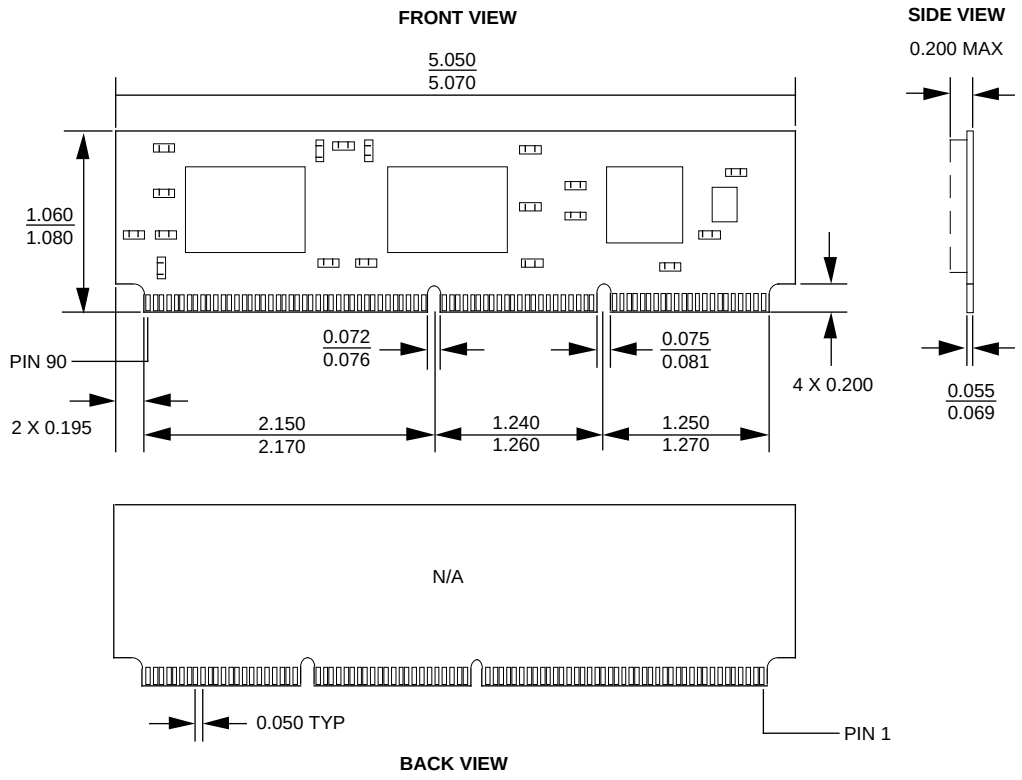
drw 06

PACKAGE DIMENSIONS - IDT7MPV6253



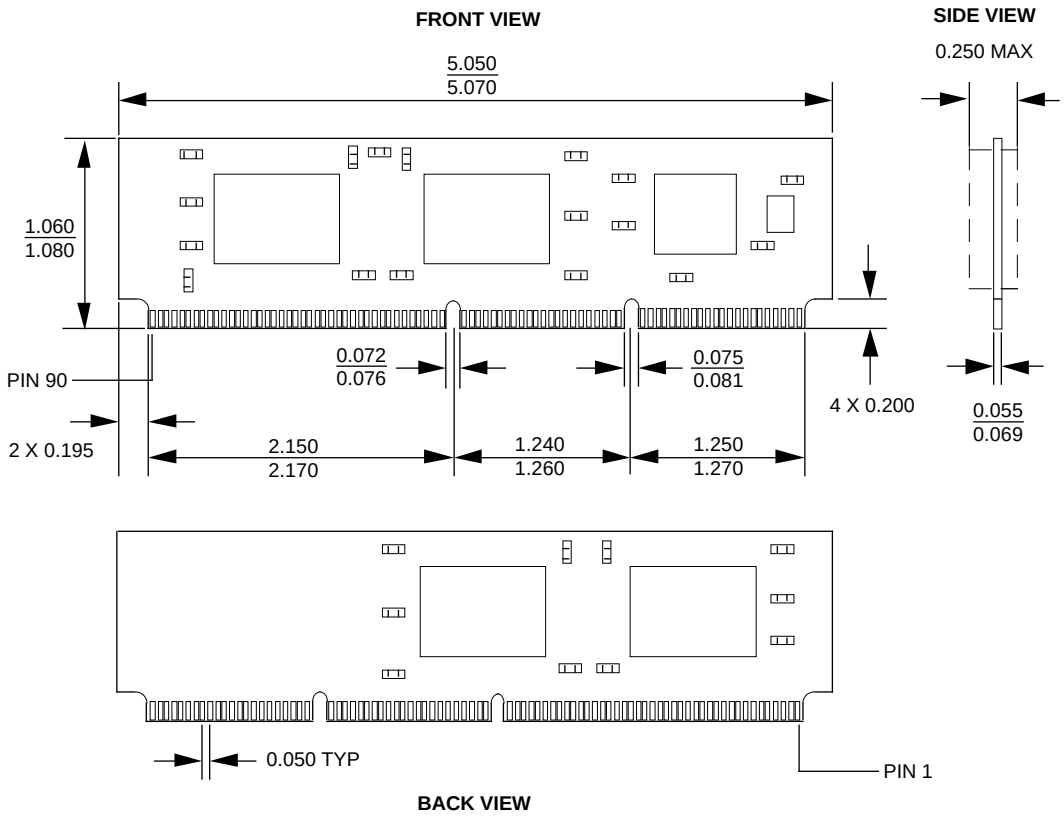
drw 07

IDT7MPV6255



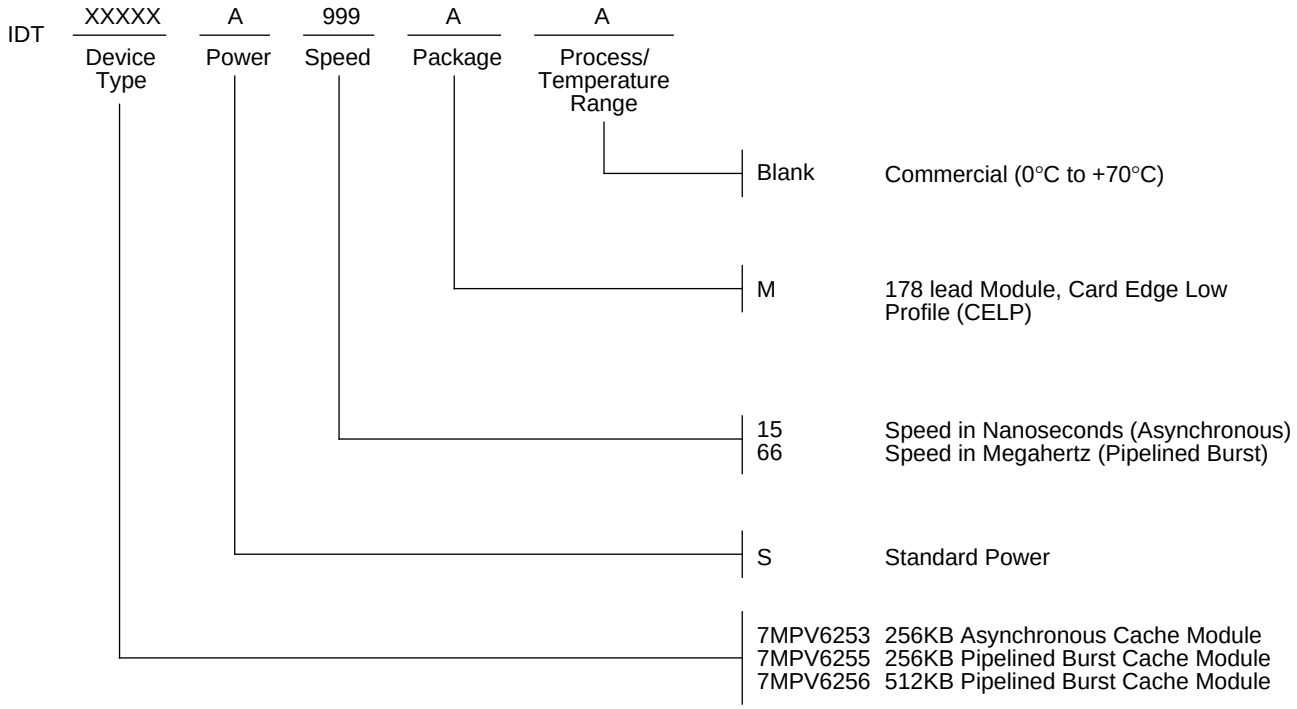
drw 08

PACKAGE DIMENSIONS - IDT7MPV6256



drw 09

ORDERING INFORMATION



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