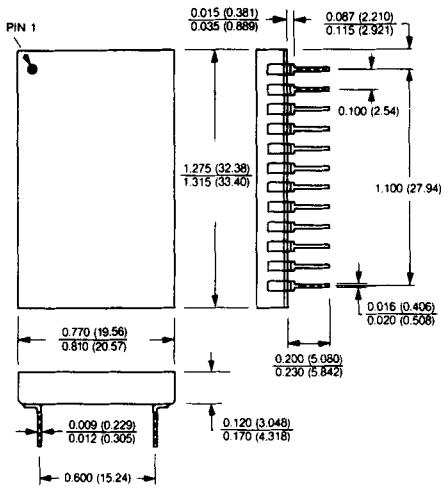
High-speed 8-bit A/D Converters

FEATURES

- High Conversion Speed
  900nsec MN5101
  1.5μsec MN5100
- Small 24-Pin DIP
- ±1/2LSB Linearity and No Missing Codes Over Temperature
- Parallel and Serial Outputs
- Adjustment-free No Gain or Offset Adjustments Necessary
- Fully Specified 0°C to +70°C (MN5100/5101) or −55°C to +125°C (MN5100/5101H or H/B)
- MIL-PRF-38534 Screening Optional.

24 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN5100 and MN5101 are very high-speed, 8-bit, successive approximation A/D converters. MN5100 guarantees a 1.5μsec conversion time, and MN5101 guarantees a 900nsec conversion time. Containing an internal reference and requiring only an external clock, these devices are much easier to use than other 8-bit A/D's in their speed class. Both devices are functionally laser trimmed and complement their speed performance with excellent linearity (±½ LSB max) and accuracy (±½ LSB max) specifications.These specifications are achieved without the need for external adjusting potentiometers and are guaranteed over the full specified temperature range. MN5100 and MN5101 are a simple solution to high-speed, low-resolution, digitizing requirements in single or multi-channel systems.

MN5100 and MN5101 are packaged in standard, 24-pin, double-wide, hermetically sealed, ceramic DIP's. Both devices are TTL compatible; have a low-drift, −6.3V internal reference; and offer 7 user-selectable input voltage ranges. Supply requirements are ±15V and +5V, and power consumption is 1550mW maximum.

Units are available and fully specified for 0°C to +70°C (MN5100 and MN5101) or −55°C to +125°C (MN5100H, H/B and MN5101H, H/B) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN5100H/B CH and MN5101H/B CH are fully screened to MIL-PRF-38534.

Part Number	Conversion Time	Specified Temperature Range
MN5100	1.5μsec	0°C to +70°C
MN5100H	1.5μsec	−55°C to +125°C
MN5100H	1.5μsec	−55°C to +125°C
MN5100H/B CH	1.5μsec	−55°C to +125°C
MN5101	900nsec	0°C to +70°C
MN5101H	900nsec	−55°C to +125°C
MN5101H/B	900nsec	−55°C to +125°C
MN5101H/B CH	900nsec	−55°C to +125°C

MN5100 MN5101 HIGH-SPEED, 8-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN5100, MN5101	0°C to +70°C
MN5100H, MN5100H/B	−55°C to +125°C (case)
MN5101H, MN5101H/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 16)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 13)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 6)	−0.5 to +7 Volts
Analog Inputs (Pins 11, 12)	±25 Volts
Digital Inputs (Pins 23, 24)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5100H/B CH

- Select MN5100 or MN5101 Model.
- Standard part is specified for 0°C to +70°C operation.
- Add "H" suffix for specified −55°C to +125°C (case) operation.
- Add "/B" to "H" devices for Environmental Stress Screening.
- Add "CH" to "H/B" devices for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Positive Unipolar Negative Bipolar		0 to +5, 0 to +10 0 to −5, 0 to −10 ±2.5, ±5, ±10		Volts Volts Volts
Input Impedance (Notes 2, 3): 5V FSR 10V FSR 20V FSR		1.5 3 6		kΩ kΩ kΩ
DIGITAL INPUTS (Start, Clock)				
Logic Levels All Inputs: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Start: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V) Clock: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			+80 −1.6 +40 −1.6	μA mA μA mA
TRANSFER CHARACTERISTICS				
Resolution		8		Bits
Linearity Error (Note 4): Initial (+25° C) Over Temperature (Note 5)		±¼ ±¼	±½ ±½	LSB LSB
Full Scale Absolute Accuracy Error (Notes 4, 6): Initial (+25° C) 0°C to +70°C −55°C to +125°C		 ±¼ ±½ ±1	 ±½ ±1 ±2	 LSB LSB LSB
Unipolar Offset Error (Notes 4, 7): Initial (+25°C) 0°C to +70°C −55°C to +125°C		 ±¼ ±½ ±1	 ±½ ±1 ±2	 LSB LSB LSB
Bipolar Zero Error (Notes 4, 8): Initial (+25°C) 0°C to +70°C −55°C to +125°C		 ±¼ ±½ ±1	 ±½ ±1 ±2	 LSB LSB LSB
DIGITAL OUTPUTS				
Output Coding (Note 9): Unipolar Ranges Bipolar Ranges		CSB COB		
Logic Levels All Outputs: Logic "1" (Isource ≤ 80μA) Logic "0" (Isink ≤ 3.2mA)	+2.4		 +0.4	Volts Volts
REFERENCE OUTPUT				
Internal Reference (Note 2): Voltage Accuracy Tempco External Current		−6.3 ±10 ±10	 200	Volts % ppm/°C μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 10): MN5100 MN5101			1.5 900	μsec nsec
External Clock Frequency (Note 2): MN5100 MN5101			5.33 8.88	MHz MHz
Clock Pulse Width (Note 2): High Low	20 50			nsec nsec
Setup Time Start Low to Clock (Note 2)	20			nsec

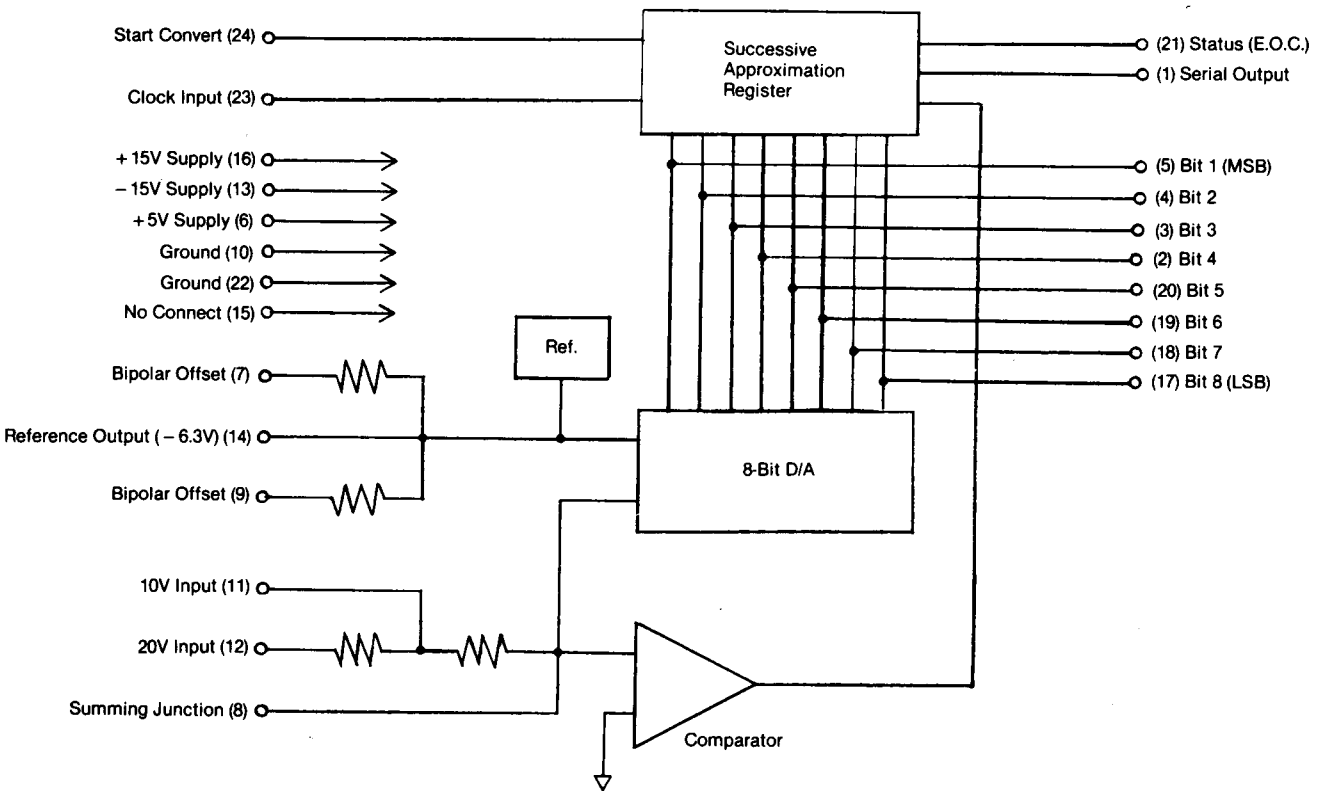
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15.00	+15.45	Volts
−15V Supply	−14.55	−15.00	−15.45	Volts
+5V Supply	+4.75	+5.00	+5.25	Volts
Power Supply Rejection (Notes 3, 11): +15V Supply		± 0.01		%FSR/%Supply
−15V Supply		± 0.03		%FSR/%Supply
+5V Supply		± 0.01		%FSR/%Supply
Current Drain: +15V Supply		+25	+35	mA
−15V Supply		−25	−35	mA
+5V Supply		+75	+100	mA
Power Consumption		1125	1550	mW

SPECIFICATION NOTES:

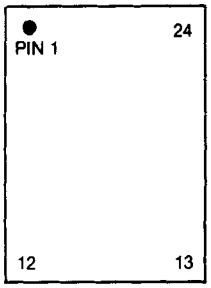
1. Listed specifications apply for all part numbers unless specifically indicated.
2. These parameters are listed for reference and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for ± 10V operation has a 20V FSR. A unit connected for 0 to + 10V, 0 to − 10V or ± 5V operation has a 10V FSR. A unit connected for 0 to + 5V, 0 to − 5V, or ± 2.5V operation has a 5V FSR.
4. 1 LSB for 8 bits in 20V FSR is 78mV.
   1 LSB for 8 bits in 10V FSR is 39mV.
   1 LSB for 8 bits in 5V FSR is 19.5mV.
5. Listed specifications apply over the 0°C to + 70°C temperature range for standard products, and over the − 55°C to + 125°C (case) range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale accuracy specifications apply at positive full scale for unipolar positive input ranges, at negative full scale for unipolar negative input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 for unipolar positive and bipolar input ranges. Additionally, it describes the accuracy of the 1111 1111 to 1111 1110 transition for unipolar negative and bipolar input ranges. The former transition ideally occurs at an input voltage 1 LSB below the nominal positive full scale voltage. The latter ideally occurs 1 LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 to 1111 1110 when operating MN5100/5101 on a unipolar positive range (0 to + 5V, 0 to + 10V) or from 0000 0000 to 0000 0001 when operating on a unipolar negative range (0 to − 5V or 0 to − 10V). The ideal value at which this transition should occur is + 1 LSB for unipolar positive ranges and − 1 LSB for unipolar negative ranges. See Digital Output Coding.
8. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating the MN5100/5101 on a bipolar range. The ideal value at which this transition should occur is 0 volts. See Digital Output Coding.
9. CSB = complementary straight binary. COB = complementary offset binary.
10. Conversion time is defined as the width of Status (E.O.C.).
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0000 to 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Serial Output	24	Start Convert
2	Bit 4	23	Clock Input
3	Bit 3	22	Ground
4	Bit 2	21	Status (E.O.C.)
5	Bit 1 (MSB)	20	Bit 5
6	+5V Supply (+Vdd)	19	Bit 6
7	Bipolar Offset	18	Bit 7
8	Summing Junction	17	Bit 8 (LSB)
9	Bipolar Offset	16	+15V Supply (+Vcc)
10	Ground	15	N.C.
11	10V Input	14	Reference Output (−6.3V)
12	20V Input	13	−15V Supply (−Vcc)

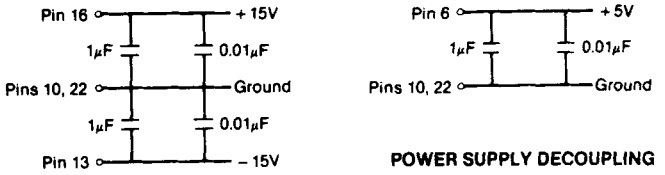
APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 24) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 21) is set to logic "1" (See Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the Status output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5100 Series converters. The units' two ground pins (pins 10 and 22) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 10 and 22 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converter. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

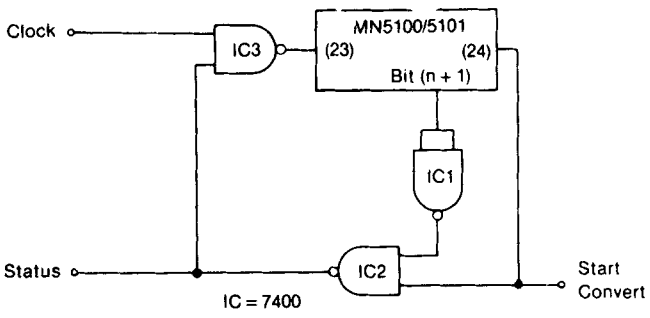


POWER SUPPLY DECOUPLING

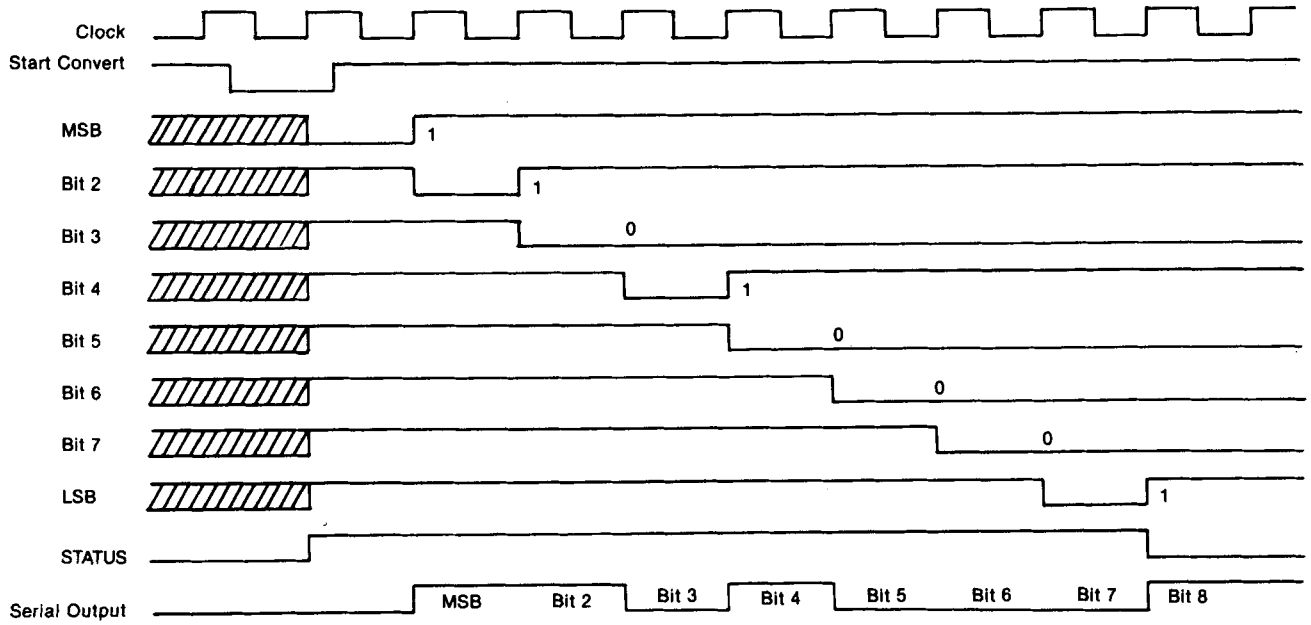
CONTINUOUS CONVERTING—The MN5100 Series A/D converters can be made to continuously convert by tying the Status output (pin 21) to the Start Convert input (pin 24). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output.

SHORT CYCLING—For applications requiring less than 8-bits resolution, the MN5100 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.

SHORT CYCLING SINGLE CONVERSION



TIMING DIAGRAM



TIMING DIAGRAM NOTES:

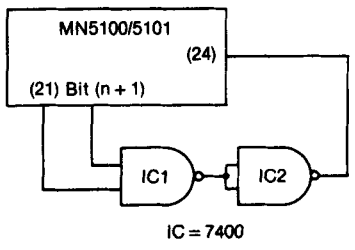
1. Operation shown is for the digital word 1101 0001 which corresponds to −8.164V on the 0 to −10V input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 20 nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the Start has returned high.
4. The delay between the resetting clock edge and Status actually rising to a "1" is 50nsec maximum.
5. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 50nsec (maximum) after the Status (E.O.C.) output has returned low. Parallel output data will remain valid and the Status output low until another conversion is initiated.
8. For continuous conversion, connect the Status output (pin 21) to the Start Convert input (pin 24). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

Assuming a conversion is already in progress, bit (n + 1) will go low as bit n is being set (see Timing Diagram). Since the Start Convert signal is high at this time, Status (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, Start Convert is brought low driving Status high and gating on the clock. The first rising clock edge the converter sees with Start Convert low will reset the converter bringing bit (n + 1) high again. Now Status will remain high as Start Convert is brought back high allowing the conversion to continue. Therefore, in this configuration, Status and Start Convert function normally, i.e., the same as Status and Start Convert for a converter not being short cycled.

SHORT CYCLING AND CONTINUOUS CONVERTING—A previous section described how continuous converting for 8-bits could be accomplished by simply tying the Status output back to the Start Convert input. To continuously convert at n bits, one simply has to tie the bit (n + 1) output back to the Start Convert input. The bit (n + 1) output acts like a Status when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be avoided by making the Start Convert input the AND function of bit (n + 1) and the Status output.

If one is already using the circuit described in the section labeled Short Cycling, one can short cycle and continuously convert by making the Start Convert input the AND function of Status (IC2) and Status (pin 21) outputs.

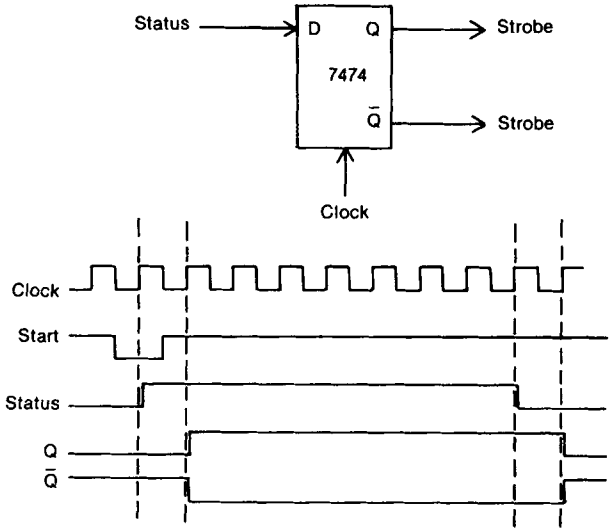
SHORT CYCLING CONTINUOUS CONVERTING



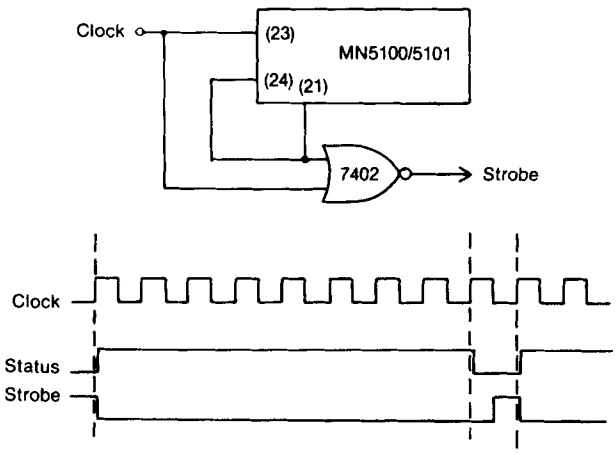
STATUS OUTPUT—The Status or End Of Conversion (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 50nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple

gate delays can be employed or the Status can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after Status changes.

LATCHING OUTPUT DATA



LATCHING DATA CONTINUOUS CONVERSIONS



If continuously converting, the Status (E.O.C.) output can be NORed with the converter clock, as shown above, to produce a positive strobe pulse ½ period wide, ½ period after the Status output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

INPUT RANGE SELECTION

Pin Connections	Analog Input Voltage Range						
	0 to −5V	0 to −10V	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect Input to Pin	11	11	11	11	11	11	12
Connect Pin 8 to Pin	12	Open	7, 9,12	7, 9	9,12	9	9
Connect Pin 7 to Pin	Ground	Ground	8, 9,12	8, 9	Ground	Ground	Ground
Connect Pin 9 to Pin	Ground	Ground	7, 8,12	7, 8	8,12	8	8
Input Impedance (kΩ)	1.5	3	1.5	3	1.5	3	6

DIGITAL OUTPUT CODING

Analog Input Voltage Range							Digital Outputs	
0 to −5V	0 to −10V	0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB	LSB
0.000 −0.019	0.000 −0.039	+5.000 +4.981	+10.000 +9.961	+2.500 +2.481	+5.000 +4.961	+10.000 +9.922	0000 0000	0000 000Ø
−2.481 −2.500 −2.519	−4.961 −5.000 −5.039	+2.519 +2.500 +2.481	+5.039 +5.000 +4.961	+0.019 0.000 −0.019	+0.039 0.000 −0.039	+0.078 0.000 −0.078	0111 ØØØØ 1000	111Ø ØØØØ 000Ø
−4.981 −5.000	−9.961 −10.000	+0.019 0.000	+0.039 0.000	−2.481 −2.500	−4.961 −5.000	−9.922 −10.000	1111 1111	111Ø 1111

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +5V, 0 to −5V or ±2.5V input ranges, 1 LSB for 8 bits = 19.5mV.
4. For 0 to +10V, 0 to −10Vor ±5V input ranges, 1 LSB for 8 bits = 39mV.
5. For ±10V input range, 1 LSB for 8 bits = 78mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5100 operating on its ±10V input range, the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.922 volts. Subsequently, any input voltage more positive than +9.922 volts will give a digital output of all "0's". The transition from digital output 1000 0000 to 0111 1111 will ideally occur at an input of 0.000 volts, and the 1111 1111 to 1111 1110 transition should occur at −9.922 volts. An input more negative than −9.922 volts will give all "1's".