EPSON

SLA40000 Series

High Density Gate Array

- Super-high-density/speed gate array
- Operates on 3.3 and 3.0V power source (level shifter is pre-installed)
- Raw of gates: 28 to 411k gates (sea of gates)

■ OVERVIEW

The SLA 40000 series are super-high-density/speed, Sea-of-gate type CMOS gate arrays adopting the 0.45É m process.
They consume less electricity, a feature of ASICs dedicated to 3.3V, while enabling high-speed-operation as well as 3V/5V full swing I/F in the level shifter.
There are 2- and 3-metal layer for each of 8 models from 28,260 to 411,257 gates, satisfying customer needs for a wide range of circuit size.
In addition, the series can be used with various I/F devices such as low noise output cells, PCI I/F revision 2.0, GTL I/F*, JTAG*, fail/safe output* and test control input*, and have diverse applications such as small information instrument and for image processing.
To develop high-speed/high-density circuits in a shorter period of time, the series enable diverse design techniques to be used during development such as high accuracy simulation of interconnection resistance and blunted waveform in addition to the conventional interconnection capacity components, and provide a new layout tool for reducing clock skew.

■ FEATURES

- Super-high density (adopting 0.45µm silicon gate CMOS with 2- and 3-metal layers)
- High-speed operation (operation delay of internal gate = 0.160ns at 3.3V, 2-input power NAND standard)
- Internal gate = 3.3 and 3.0V (2.0V single), I/O buffer = 5.0, 3.3 and 3.0V (2.0V single) (built-in level shifter)
- Low power consumption (0.80µW/MHz/BC when internal cell = 3.0V)
- Output drivability (I_{OL} = 100µ, 1, 3, 6, 12, 24 mA when PCI = 5.0V, I_{OL} = 100µ, 1, 2, 6, 12mA when PCI = 3.3V, I_{OL} = 50µ, 300µ, 600µ, 2, 4mA when 2.0V)
- RAM, PLL, IrDA*, and various function cells available
- Low noise output cell, PCI I/F, USB I/F*, LVDS*, JTAG

■ PRODUCT LINEUP

Master / Features		SLA4028	SLA4046	SLA4078	SLA4115	SLA4162	SLA4239	SLA4318	SLA4411
	3-layer Metal	SLA402T	SLA404T	SLA407T	SLA411T	SLA416T	SLA423T	SLA431T	SLA441T
Total BCs (Raw Gates)		28,260	46,864	78,600	115,388	162,864	239,468	318,308	411,257
Usable BCs	2-layer Metal	14,130	22,026	35,370	51,924	70,031	95,787	127,323	164,502
	3-layer Metal	24,868	39,834	62,880	86,541	122,148	167,627	222,815	287,879
Number of PADs		116	144	184	216	256	308	352	400
(In Case of Micro Pitch)		(128)	(164)	(212)	(256)	(304)	(368)	(424)	(480)
Propagation Delay	Internal Gates	tpd = 0.160ns (standard at 3.3V)							
	Input Gates	tpd = 0.400ns (standard at 5.0V) level shifter, tpd = 0.420ns (standard at 3.3V)							
	Output Buffers	tpd = 1.99ns (standard at 5.0V) level shifter, tpd = 1.89ns (standard at 3.3V) CL = 50pF							
I/O Level		CMOS, TTL, PCI, USB*, LVDS*							
Input Mode		LVTTL, TTL, CMOS, Pull-up/Pull-down, Schmitt, 2.0/3.0/3.3/5.0V Level interface (Level shifter)							
Output Mode		Normal, Open drain, 3-state, Bi-directional, 2.0/3.0/3.3/5.0V Level interface (Level shifter)							

* Under development

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