SDRAM

4M x 16 SDRAM

1M x 16bit x 4Banks Synchronous DRAM

FEATURES

- 3.3V power supply
- Four banks operation
- LVTTL compatible with multiplexed address
- All inputs are sampled at the positive going edge of system clock
- Burst Read Single-bit Write operation
- DQM for masking
- Auto refresh and self refresh
- 64ms refresh period (4K cycle)
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1 , 2 , 4 , 8 & full page)
  - Burst Type (Sequential & Interleave)
- Available package type in 54 pin TSOP(II)
- Operating temperature : 0 ~ +70 °C

ORDERING INFORMATION

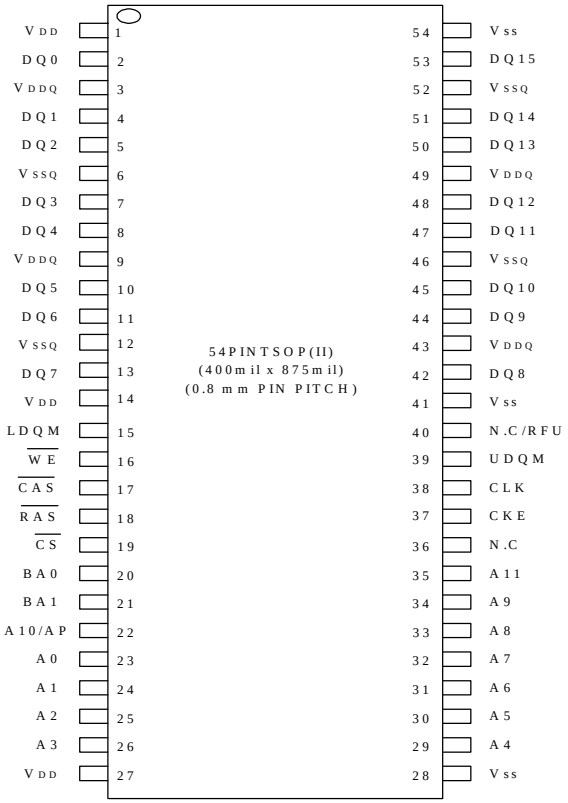
PART NO.	MAX FREQUENCY	PACKAGE
T436416A-6S	166 MHz	54 pin TSOP(II)
T436416A-7S	143 MHz	54 pin TSOP(II)
T436416A-7.5S	133 MHz	54 pin TSOP(II)
T436416A-8S	125 MHz	54 pin TSOP(II)
T436416A-10S	100 MHz	54 pin TSOP(II)
T436416A-6SG	166 MHz	54 pin TSOP(II) lead-free
T436416A-7SG	143 MHz	54 pin TSOP(II) lead-free
T436416A-7.5SG	133 MHz	54 pin TSOP(II) lead-free
T436416A-8SG	125 MHz	54 pin TSOP(II) lead-free
T436416A-10SG	100 MHz	54 pin TSOP(II) lead-free

GRNERAL DESCRIPTION

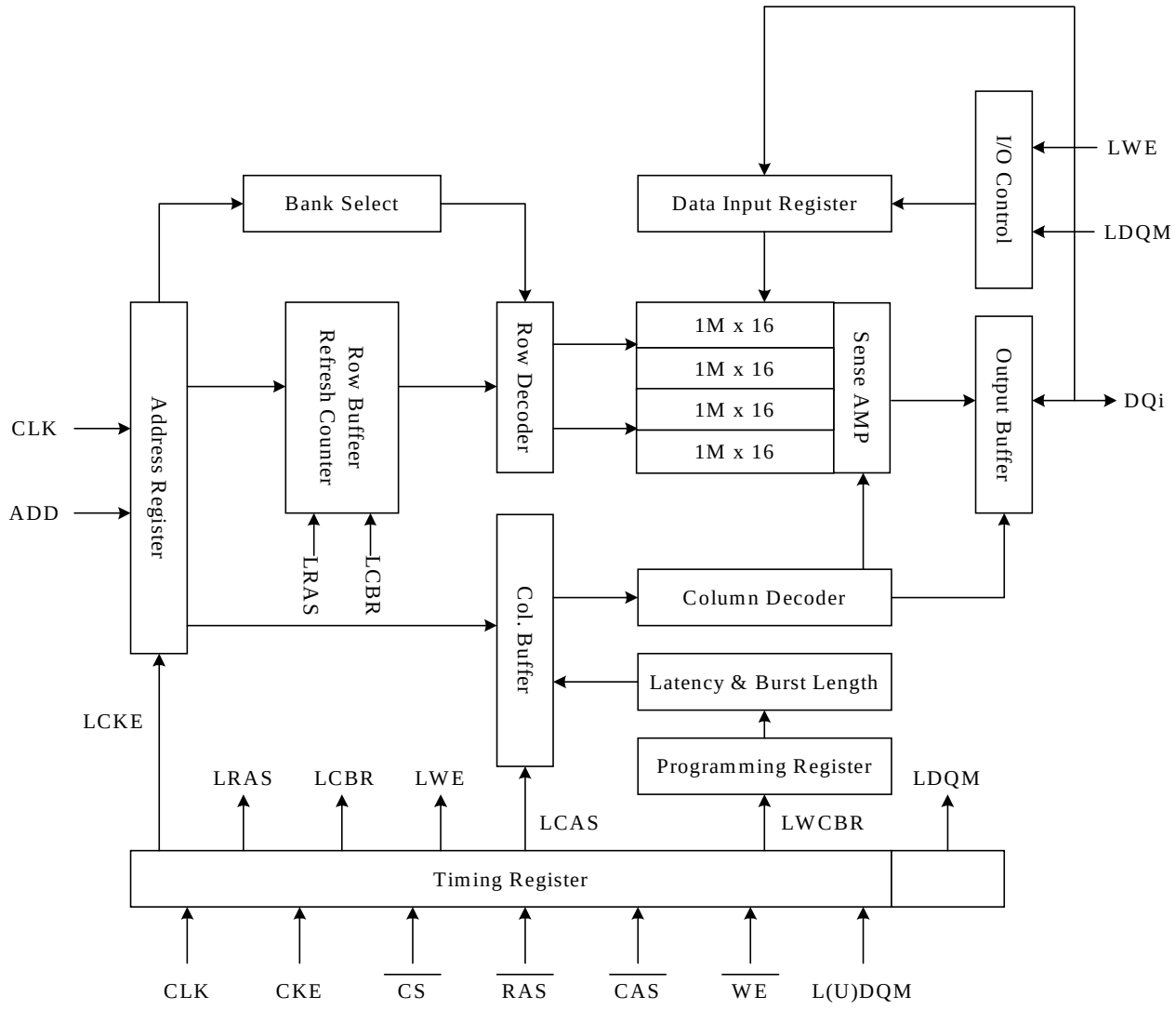
The T436416A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits , fabricated with high performance CMOS technology .

Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clockcycle . Range of operating frequencies , programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth , high performance memory system applications.

PIN ARRANGEMENT (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all input.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all input except CLK,CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11,column address : CA0 ~ CA7
BA0 ~ BA1	Bank Select Address	Selects bank to be activated during row address latch time. Select bank for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access .
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input/Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No Connection/Reserved for Future Use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative To Vss	V_{IN},V_{OUT}	-1.0 to 4.6	V
Supply Voltage Relative To Vss	V_{DD},V_{DDQ}	-1.0 to 4.6	V
Short circuit Output Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70°C, Voltage referenced to V_{SS}=0V)

Parameter	Symbol	Min.	Typ	Max.	Unit	Notes
Supply Voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{DD}+0.3V	V	1
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL}=2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width $\leq$ 10ns acceptable.

2. V_{IL} (min) = -1.0V AC for pulse width $\leq$ 10ns acceptable.

3. Any input $0V \leq V_{IN} \leq V_{DD}+0.3V$, all other pin are not under test = 0V.

4. Dout = disable, $0V \leq V_{OUT} \leq V_{DD}$.

CAPACITANCE

(T_A =25°C,V_{DD}=3.3V, f = 1MHz)

Pin	Symbol	Min	Max	Unit
CLOCK	C_{CLK}	2.5	4.0	pF
ADDRESS	C_{ADD}	2.5	5.0	pF
DQ0 ~ DQ15	C_{OUT}	4.0	6.5	pF
RAS,CAS,WE,CS,CKE,LDQM, UDQM	C_{IN}	2.5	5.0	pF

DC CHARACTERISTICS

T_A = 0 to 70°C , V_{IH}(min)/V_{IL}(max)=2.0V/0.8V

Parameter	Symbol	Speed version					Unit	Test Condition		Note
		-6	-7	-7.5	-8	-10				
Operating Current (One Bank Active)	I_{CC1}	140	120	115	110	100	mA	Burst Length = 1 $t_{RC} \geq t_{RC}$(min) ,$t_{CC} \geq t_{CC}$(min),I_{OL}= 0 mA		1,3
Precharge Standby Current in power-down mode	$I_{CC2}P$	2					mA	CKE ≤ V_{IL}(max),t_{CC}=15ns		3
	$I_{CC2}PS$	2						CKE ≤ V_{IL}(max),CLK ≤ V_{IL}(max), t_{CC} =∞		
Precharge Standby Current in non power-down mode	$I_{CC2}N$	30					mA	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min),t_{CC}=15ns Input signals are changed one time during 30ns		3
	$I_{CC2}NS$	2						CKE≥V_{IH}(min),CLK ≤ V_{IL}(min),t_{CC}=∞ Input signals are stable		
Active Standby Current in power-down mode	$I_{CC3}P$	10					mA	CKE ≤ V_{IL}(max),t_{CC}=15ns		3
	$I_{CC3}PS$	10						CKE ≤ V_{IL}(max),CLK ≤ V_{IL}(max),t_{CC}=∞		
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	40					mA	CKE≥V_{IH}(min), $\overline{CS}$ ≥V_{IH}(min),t_{CC}=15ns Input signals are changed one time during 30ns		3
	$I_{CC3}NS$	10						CKE≥V_{IH}(min),CLK ≤ V_{IL}(min),t_{CC}=∞ Input signals are stable		
Operating Current (Burst Mode)	I_{CC4}	150	130	125	120	110	mA	CAS Latency 3	I_{OL}=0 mA,Page Burst All Band Activated t_{CCD}= t_{CCD}(min)	1,3
		150	130	125	120	110		CAS Latency 2		
Refresh Current	I_{CC5}	150	130	125	120	110	mA	$t_{RC} \geq t_{RC}$(min)		2,3
Self refresh Current	I_{CC6}	1					mA	CKE ≤ 0.2V		

Note: 1. Measured with output open. Addresses are changed only one time during t_{CC}(min) .

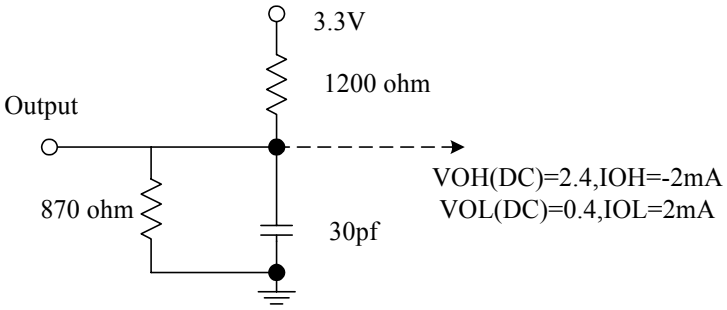
2. Refresh period is 64ms. Addresses are changed only one time during t_{CC}(min) .

3. t_{CC} : Clock cycle time.
   t_{RC} : Row cycle time.
   t_{CCD} : Column address to column address delay time.

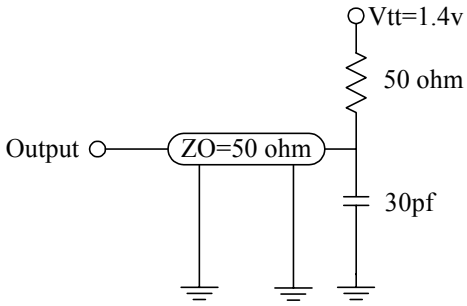
AC OPERATING CONDITIONS

(V_{DD}=3.3V ±0.3V ,T_A= 0 to 70°C)

Parameter	Value	Unit
Input levels (V_{IH}/V_{IL})	3.0 / 0	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t_r / t_f = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig.1) DC Output Load Circuit



(Fig.2)AC Output Load Circuit

OPERATING AC PARAMETER

(AC opterating conditions unless otherwise noted)

Parameter	Symbol	Speed Version					Unit	Note
		-6	-7	-7.5	-8	-10		
Row active to row active delay	t_{RRD}(min)	12	14	15	16	20	ns	1
RAS to CAS delay	t_{RCD}(min)	16	18	18	20	20	ns	1
Row precharge time	t_{RP}(min)	18	20	20	20	20	ns	1
Row active time	t_{RAS}(min)	42	42	45	48	50	ns	1
	t_{RAS}(max)	100K					ns	
Row cycle time	t_{RC}(min)	60	63	65	68	70	ns	1
Last data in to new col. Address delay	t_{CDL}(min)	1					CLK	2
Last data in to row precharge	t_{RDL}(min)	2					CLK	2
Last data in to burst stop	t_{BDL}(min)	1					CLK	2
Col. Address to col. Address delay	t_{CCD}(min)	1					CLK	3
Number of valid output data	CAS latency=3	1					ea	4
	CAS latency=2	1						

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
The earliest a precharge command can be issued after a Read command without the loss of data is CL + BL-2 clocks.

AC CHARACTERISTICS

(AC opterating conditions unless otherwise noted)

Parameter		Symbol	-6		-7		-7.5		-8		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency = 3	t_{CC}	6	1K	7	1K	7.5	1K	8	1K	10	1K	ns	1
	CAS Latency = 2		8		9		9		10		10			
CLK to valid Output delay	CAS Latency = 3	t_{SAC}	-	5.5	-	6		6	-	6	-	7	ns	1
	CAS Latency = 2		-	6	-	6		6	-	7	-	9	ns	
Output data hold time		t_{OH}	2		2.5		2.5		2.5		2.5		ns	2
CLK high pulse width		t_{CH}	2		2.5		2.5		3		3		ns	3
CLK low pulse width		t_{CL}	2		2.5		2.5		3		3		ns	3
Input setup time		t_{SS}	1.5		1.75		1.75		2		2.5		ns	3
Input hold time		t_{SH}	1		1			1	1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1			1	1		1		ns	2
CLK to output in Hi-Z	CAS Latency = 3	t_{SHZ}	-	5.5	-	6		6	-	6	-	7	ns	
	CAS Latency = 2		-	6	-	6		6	-	7	-	9	ns	

Note: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns,(tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns,transient time compensation should be considered,
   i.e.,[(tr+tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONAHIP TABLE

T436416A-6S (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		60ns	42ns	18ns	12ns	16ns	6ns	6ns	12ns
166MHz(6.0ns)	3	10	7	3	2	3	1	1	2
143MHz(7.0ns)	3	9	6	3	2	3	1	1	2
125MHz(8.0ns)	2	9	6	3	2	2	1	1	2
111MHz(9.0ns)	2	7	5	2	2	2	1	1	2
100MHz(10.0ns)	2	7	5	2	2	2	1	1	2

T436416A-7S (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		63ns	42ns	20ns	14ns	18ns	7ns	7ns	14ns
143MHz(7.0ns)	3	9	6	3	2	3	1	1	2
125MHz(8.0ns)	3	9	6	3	2	2	1	1	2
111MHz(9.0ns)	2	8	5	3	2	2	1	1	2
100MHz(10.0ns)	2	7	5	2	2	2	1	1	2
83MHz(12.0ns)	2	6	4	2	2	2	1	1	2

T436416A-7.5S (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		65ns	45ns	20ns	15ns	18ns	7.5ns	7.5ns	15ns
133MHz(7.5ns)	3	9	6	3	2	3	1	1	2
125MHz(8.0ns)	3	9	6	3	2	3	1	1	2
111MHz(9.0ns)	2	8	5	3	2	2	1	1	2
100MHz(10.0ns)	2	7	5	2	2	2	1	1	2
83MHz(12.0ns)	2	6	4	2	2	2	1	1	2

T436416A-8S (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		68ns	48ns	20ns	16ns	20ns	8ns	8ns	16ns
125MHz(8.0ns)	3	9	6	3	2	3	1	1	2
111MHz(9.0ns)	3	9	6	3	2	3	1	1	2
100MHz(10.0ns)	2	7	5	2	2	2	1	1	2
83MHz(12.0ns)	2	6	4	2	2	2	1	1	2
75MHz(13.0ns)	2	6	4	2	2	2	1	1	2

T436416A-10S (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	20ns
100MHz(10.0ns)	2	7	5	2	2	2	1	1	2
83MHz(12.0ns)	2	7	5	2	2	2	1	1	2
75MHz(13.0ns)	2	6	4	2	2	2	1	1	2
66MHz(15.0ns)	2	6	4	2	2	2	1	1	2
60MHz(16.7ns)	2	5	3	2	2	2	1	1	Note 1

Note : 1. $t_{RDL} \geq$ 16.7ns is recommended for T436416A

2. Clock count formula : clock $\geq \frac{\text{base value}}{\text{clock period}}$ (round off whole number).

MODE REGISTER

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	1								JEDEC Standard Test Set (refresh counter test)
x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
			1	0								Use in future
x	x	x	1	1	v	v	v	v	v	v	v	Vender Specific
0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

v = Valid
x = Don't care

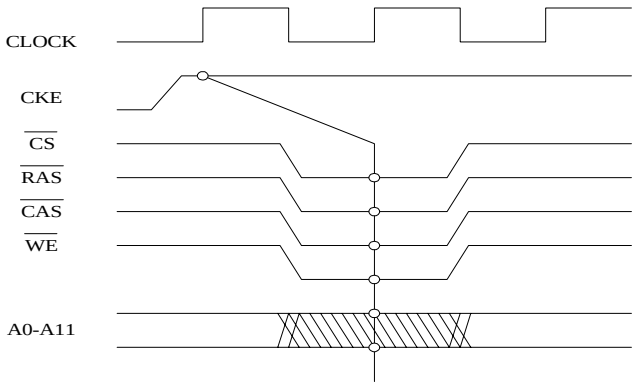
	Bit2-0	WT=0	WT=1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

	Bit6-4	CAS Latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Mode Register Write Timing



Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (Decimal)
0	0,1	0,1
1	1,0	1,0

(Burst of Four)

Starting Address (column address A1-A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (Decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

(Burst of Eight)

Starting Address (column address A2-A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (Decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 256 for 1Mx16 divice.

POWER UP SEQUENCE

1. Apply power and start clock, attempt to maintain CKE = ‘H’ , L(U)DQM = ‘H’ and the other pin are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue mode register set command to initalize the mode register.

   Cf.) Sequence of 4 & 5 is regardless of the order.

SIMPLIFIED TRUTH TABLE

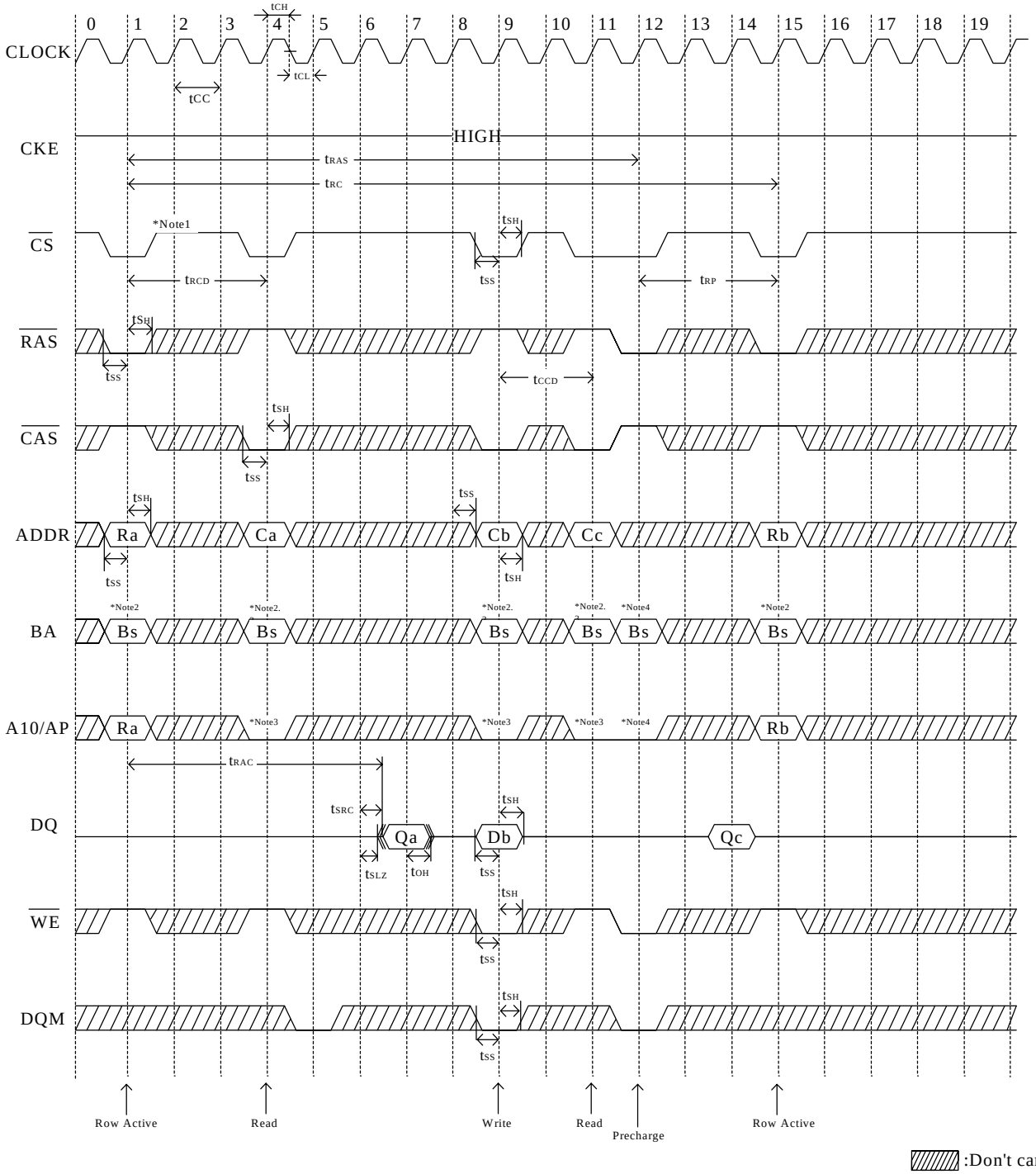
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA 0,1	A10/AP	A9~A0, A11	Note
Register	Mode Register Set		H	X	L	L	L	L	X	X			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					
Bank Active & Row Address			H	X	L	L	H	H	X	V	Row Address		
Read Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4,5
	Auto Precharge Enable										H		
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4,5
	Auto Precharge Enable										H		
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L		4
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
			H		L	H	H	H					

(V=Valid , X=Don't Care , H=Logic High , L=logic Low)

Notes :

1. OP Code : Operation Code. A0~A11 , BA0~BA1 : Program keys.(@MRS)
2. MRS can be issued only at both banks precharge state. A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM. The automatical precharge without row precharge command is meant by 'Auto'. Auto / self refresh can be issued only at both banks precharge state.
4. BA0~BA1 : Bank select address.
   If both BA0 and BA1 are 'Low' : at read , write , row active and precharge , bank A is selected.
   If both BA0 is 'Low' and BA1 is 'High' : at read , write , row active and precharge , bank B is selected.
   If both BA0 is 'High' and BA1 is 'Low' : at read , write , row active and precharge , bank C is selected.
   If both BA0 and BA1 are 'High' : at read , write , row active and precharge , bank D is selected
   If A10/AP is 'High' : at row precharge , BA0 and BA1 ignored and all banks are selected.
5. During burst read or write with auto precharge , new read/write command cannotbeissued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Single Bit READ-Write Cycle (Same Page) @CAS Latency=3,Burst Length=1



*note : 1. All input expect CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.

2. Bank active & read/write are controlled by BA0 – BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
1	0	Bnak B
0	1	Bank C
1	1	Bnak D

3. Enable and disable auto precharge function are controlled by A10/AP in read/wirte command.

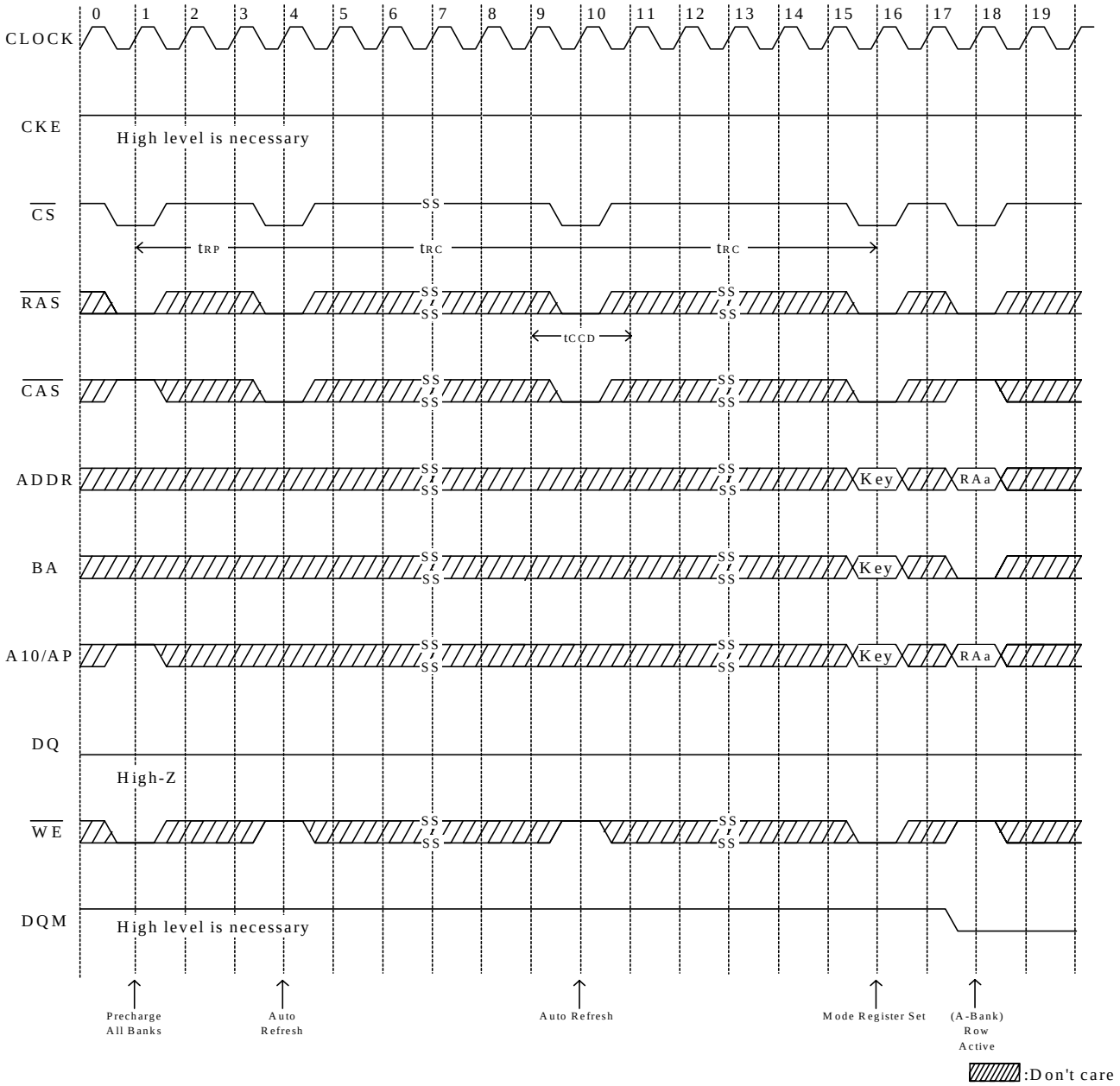
A10	Auto-Precharge
0	Disable (End of burst)
1	Enable (End of burst)

BA0	BA1	Operation
0	0	Enable read/write command for bank A .
1	0	Enable read/write command for bank B .
0	1	Enable read/write command for bank C .
1	1	Enable read/write command for bank D .

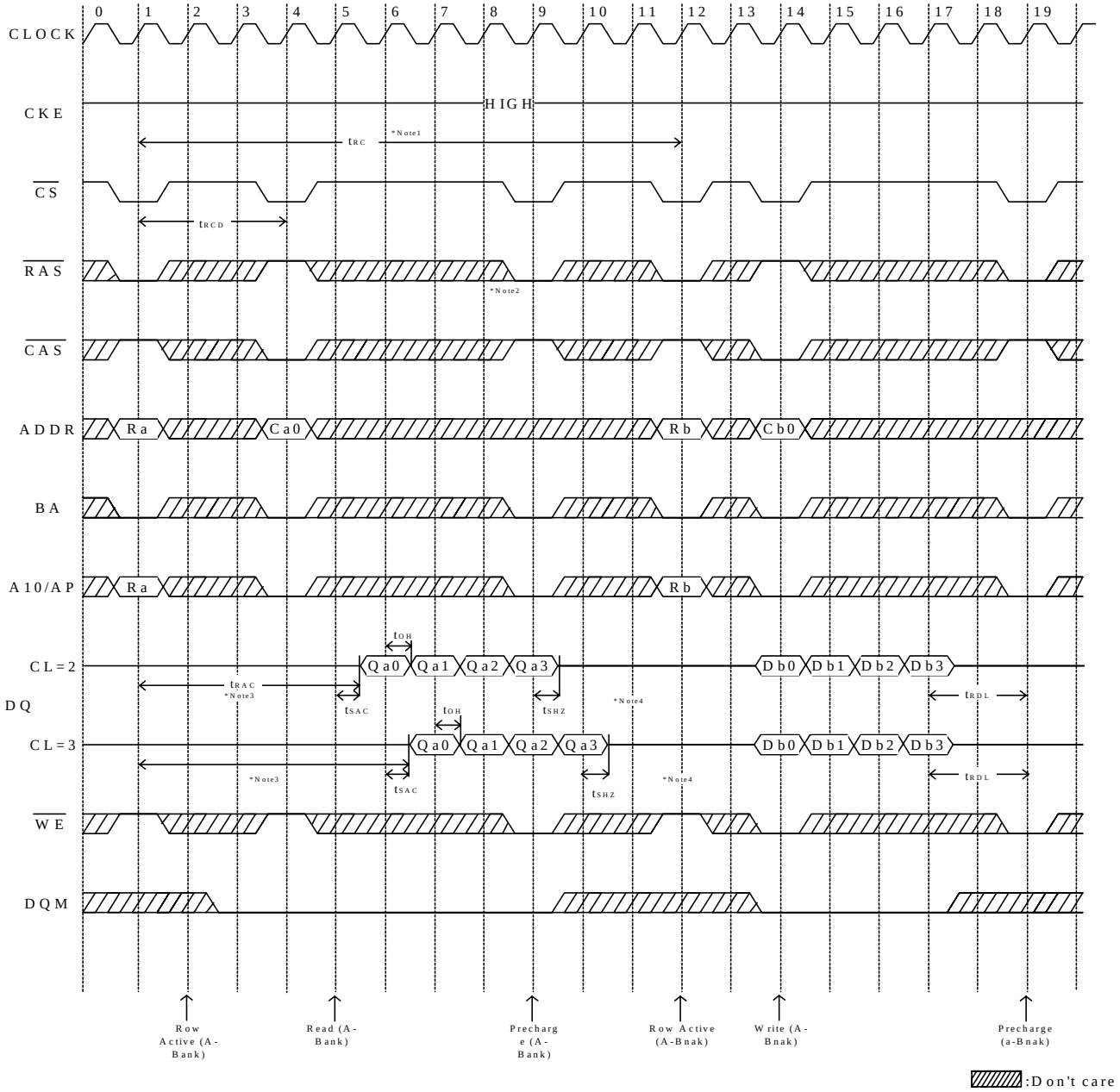
4. A10/AP and BA control bank precharge when precharge command is asserted.

A10/AP	BA0	BA1	precharge
0	0	0	Bank A
0	1	0	Bank B
0	0	1	Bank C
0	1	1	Bank D
1	X	X	All Bamks

Power Up Sequence



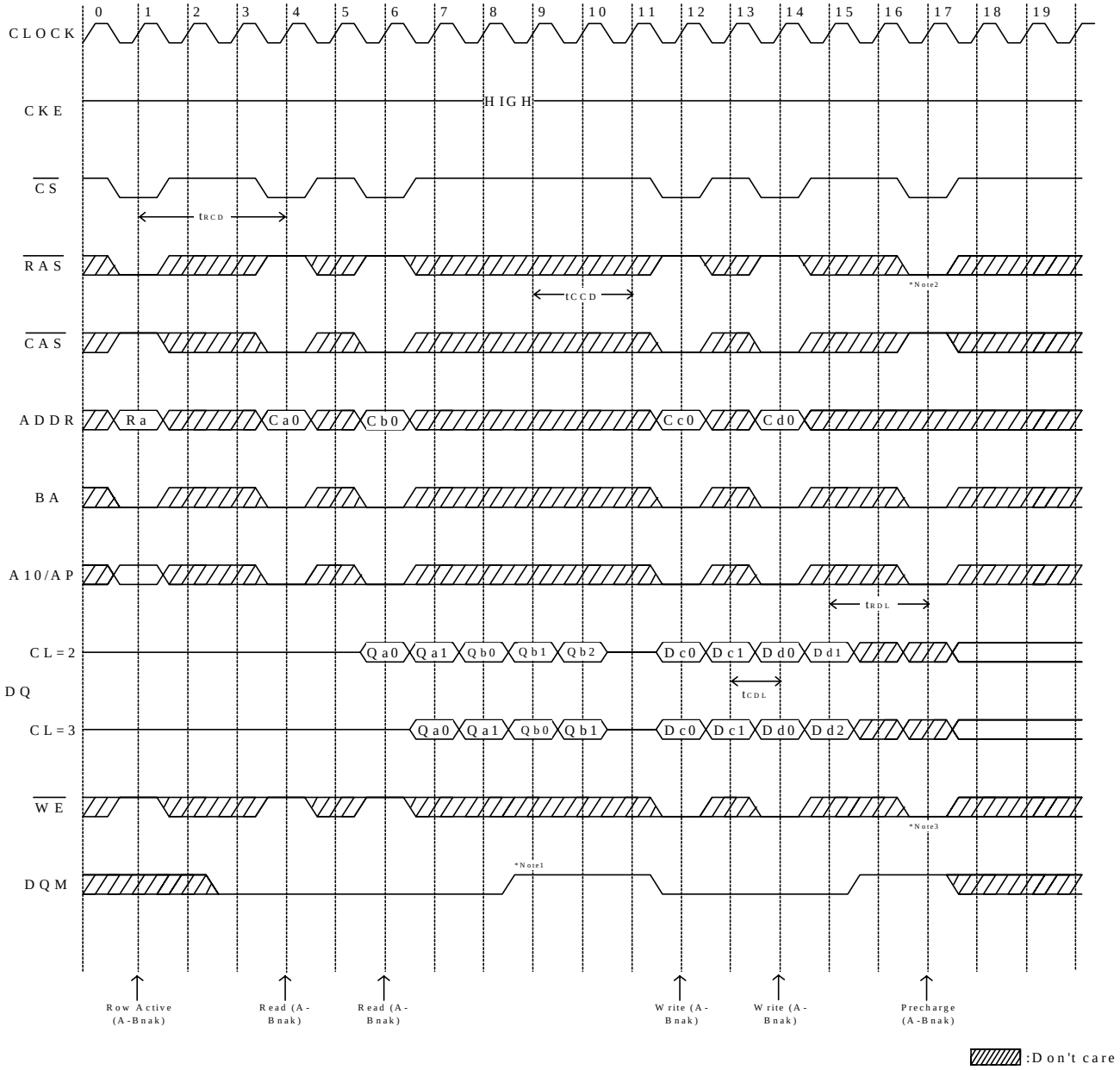
Read & Write Cycle at Same Bank @Burst Length = 4



*Note : 1. Minimum row cycle times is requiqed to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
3. Access time from Row active command. t_{CC}*(t_{RCD}+CAS latency-1)+t_{SAC}
4. Output will be Hi-Z after the end of burst.(1,2,4,8 bit burst)
   Burst can't end in Full Page Mode.

Page Read & Write Cycle at Same Bank @ Burst Length = 4

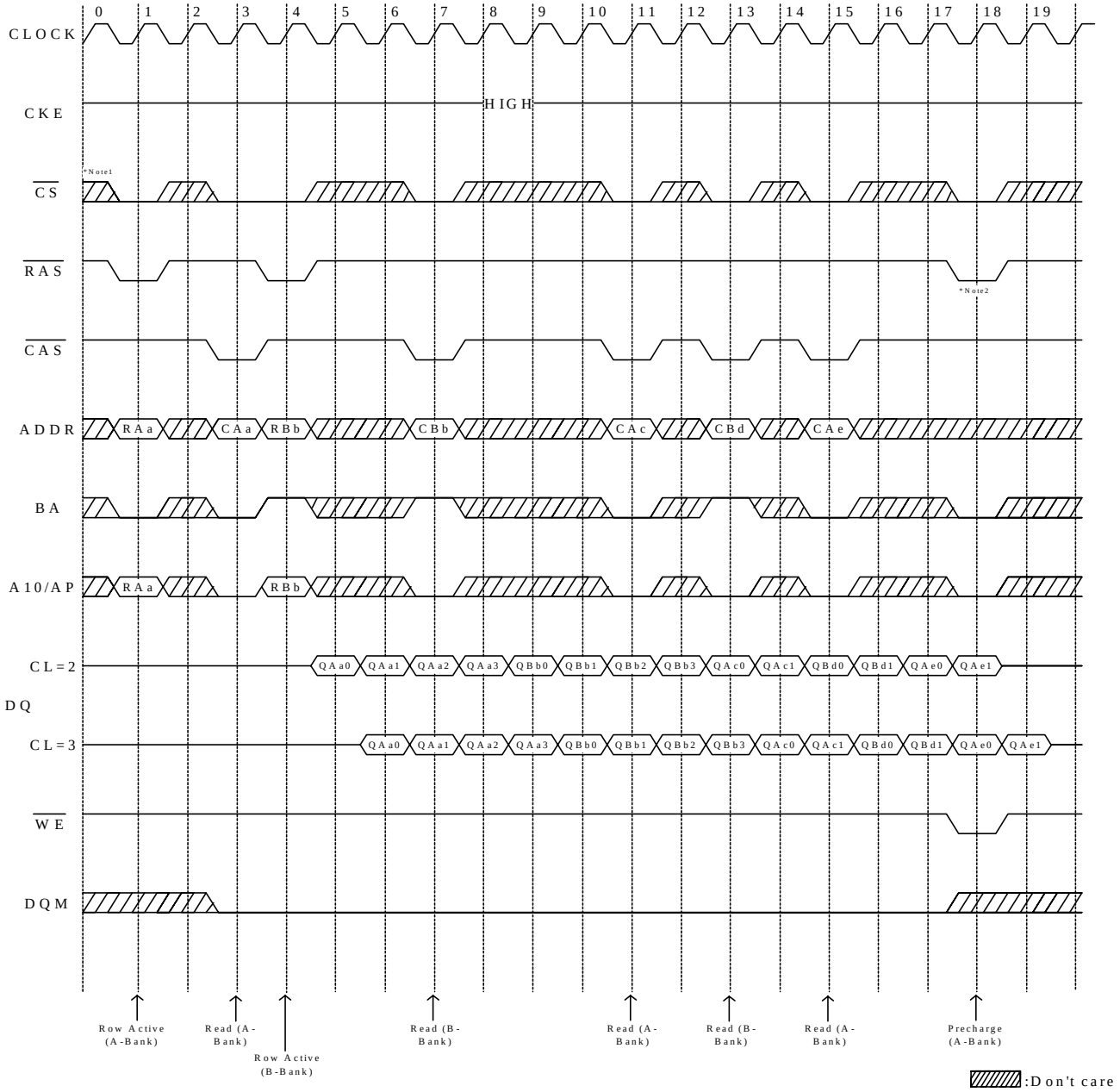


*Note : 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.

3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

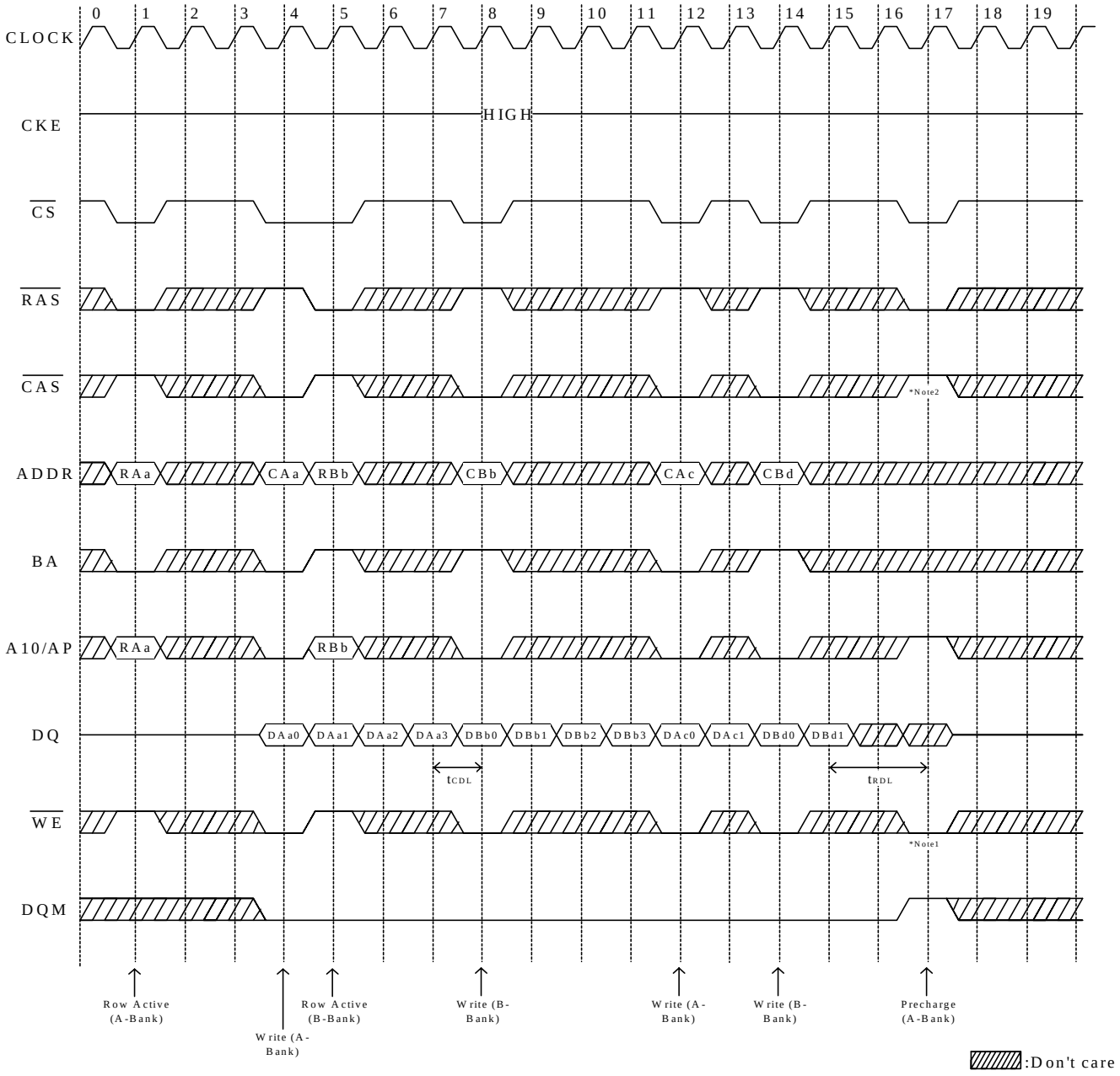
Page Read Cycle at Different Bank @ Burst Length = 4



*Note : 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.

2. To interrupt a burst resd by row precharge, both the read and the precharge banks must be the same.

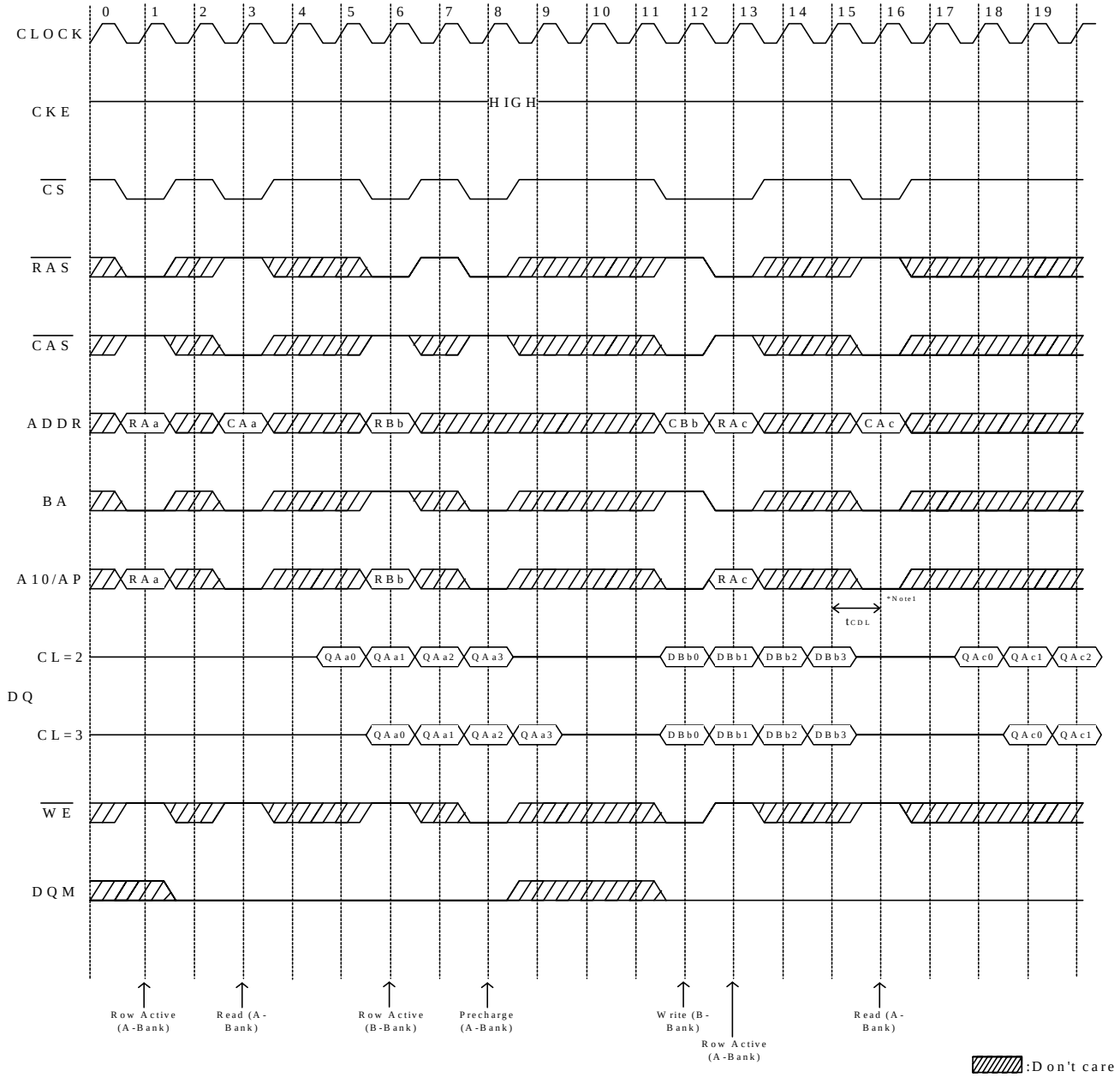
Page Write cycle at Different Bank @ Burst Length = 4



*Note : 1. To interrupt burst write by row precharge, DQM should be asserted to mask invalid input data.

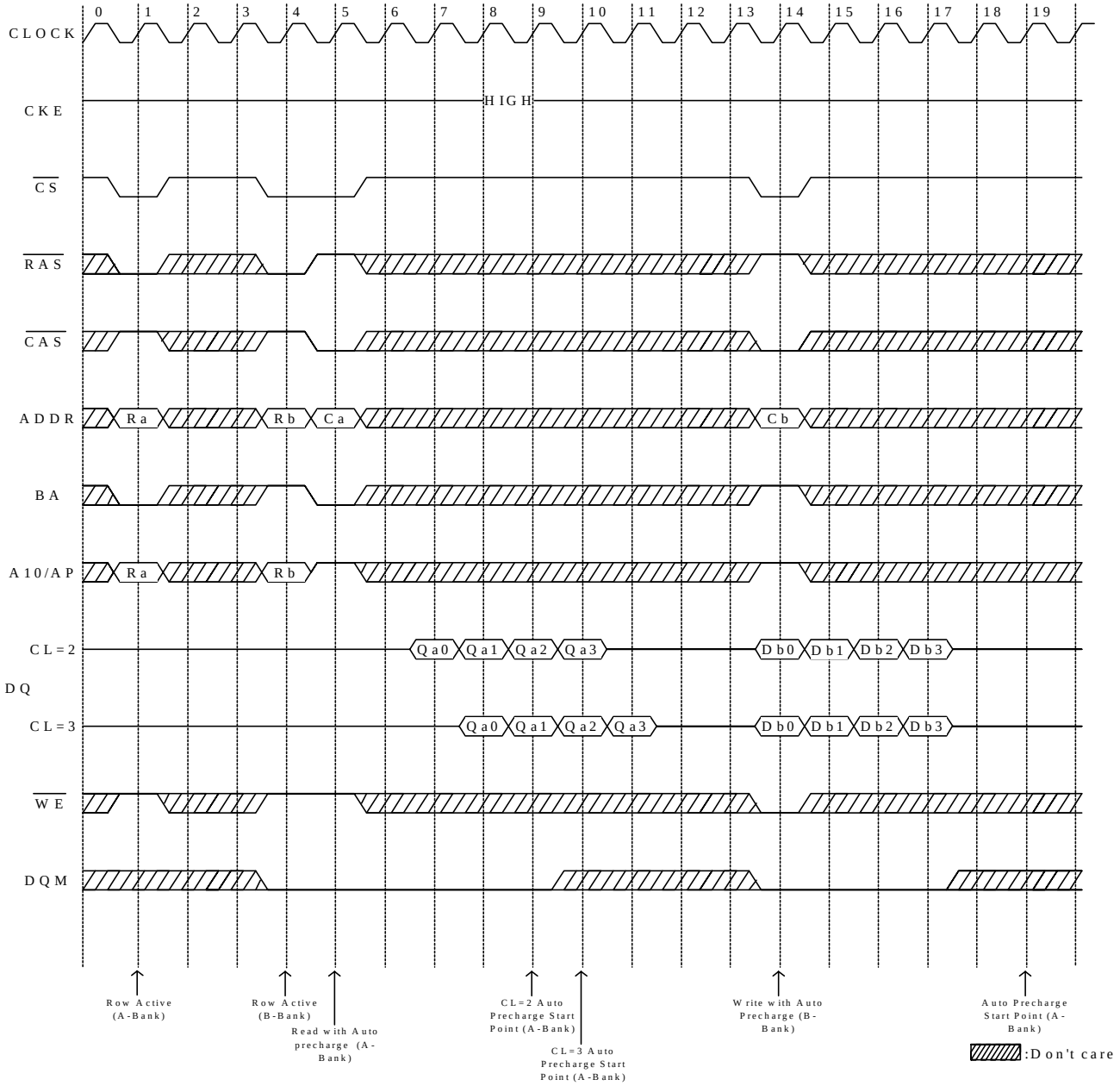
2. To interrupt burst write by row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @ Burst Length = 4



*Note : 1. t_{CDL} should be met to complete write.

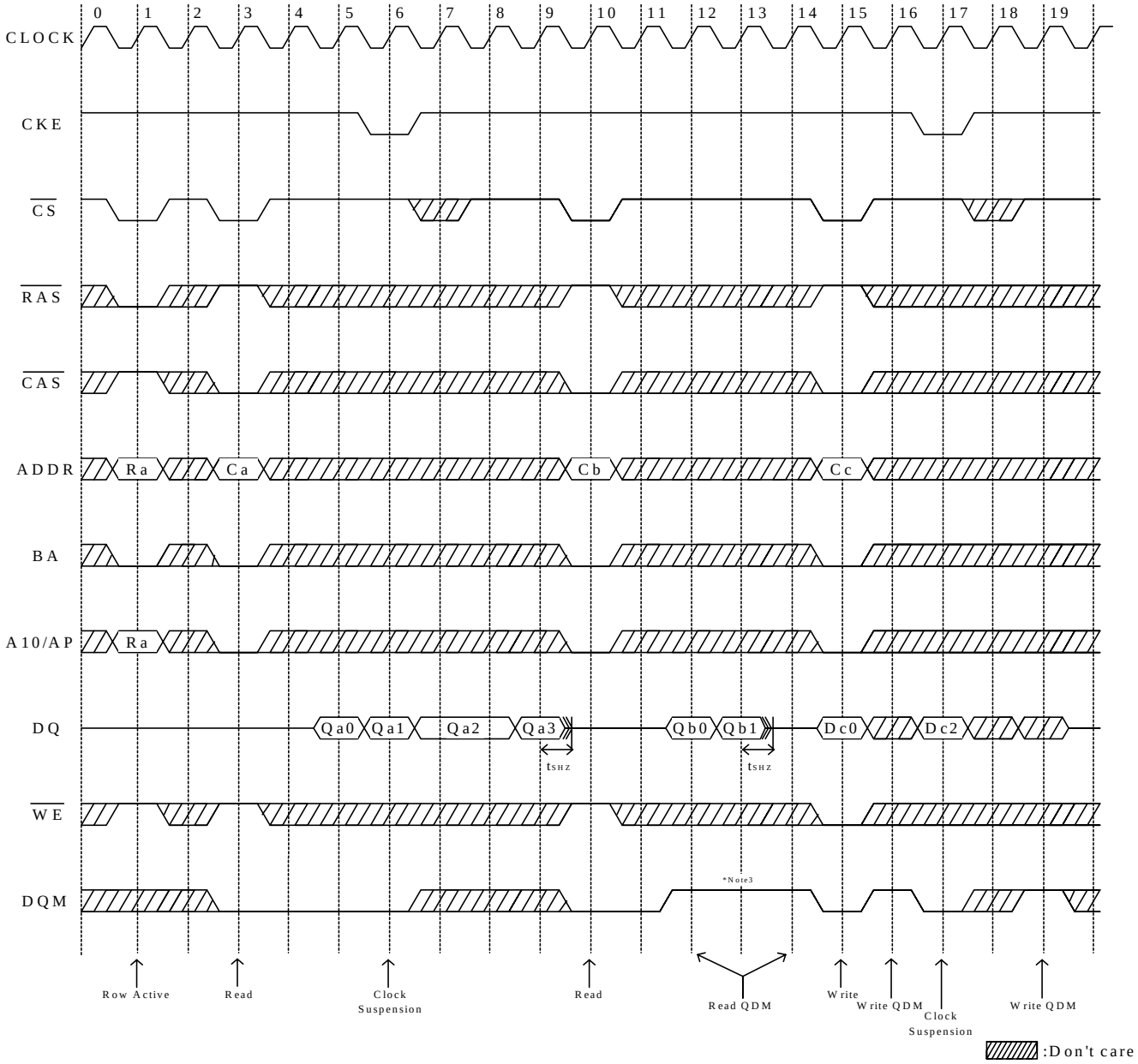
Read & Write Cycle with Auto Precharge @ Burst Length = 4



*Note : 1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.

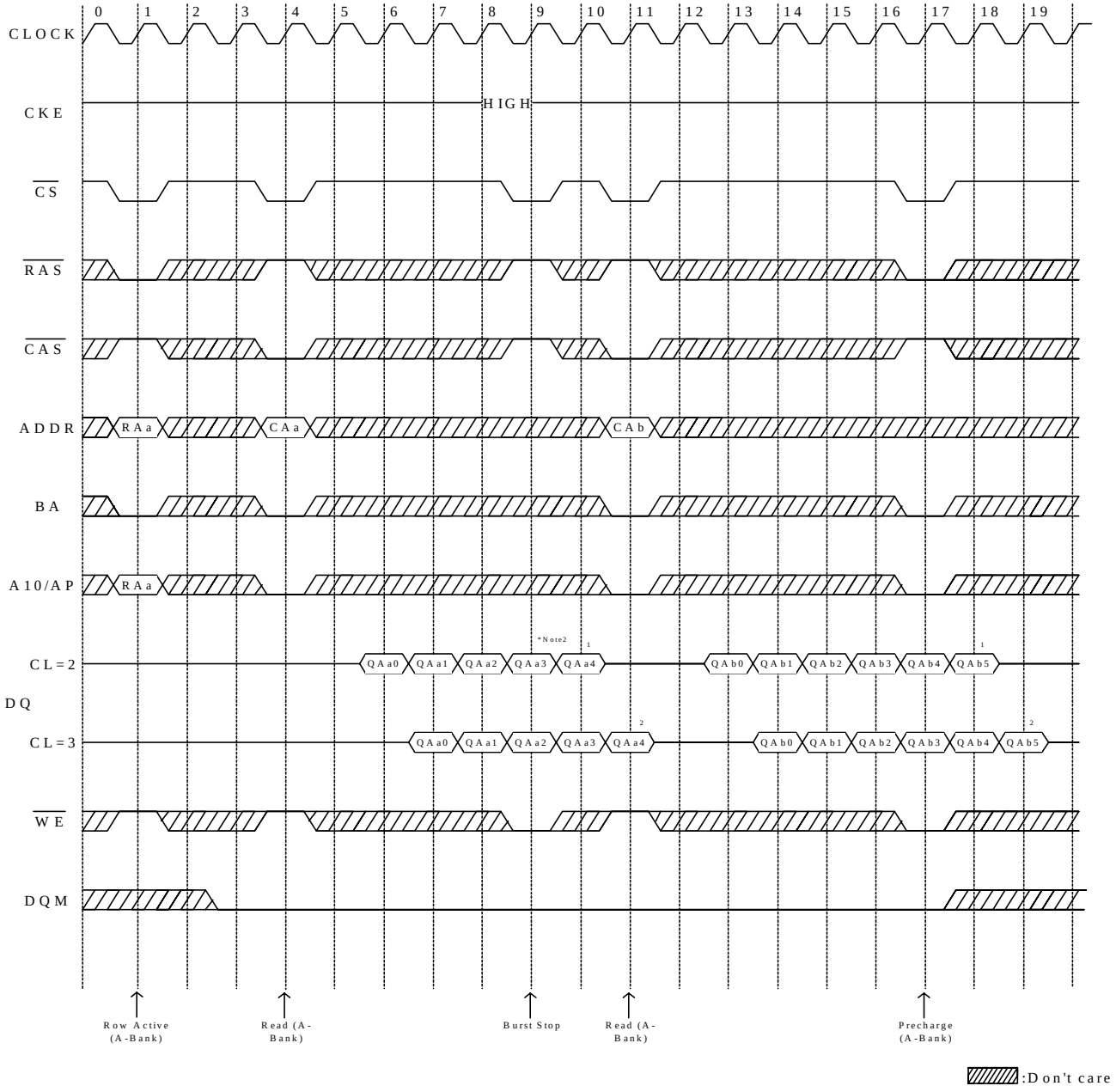
(In the case of Burst Length = 1 & 2 and BRSW mode)

Clock suspension & DQM Operation Cycle @ CAS Latency = 2 ,Burst Length = 4



*Note 1. DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Burst Length=Full Page

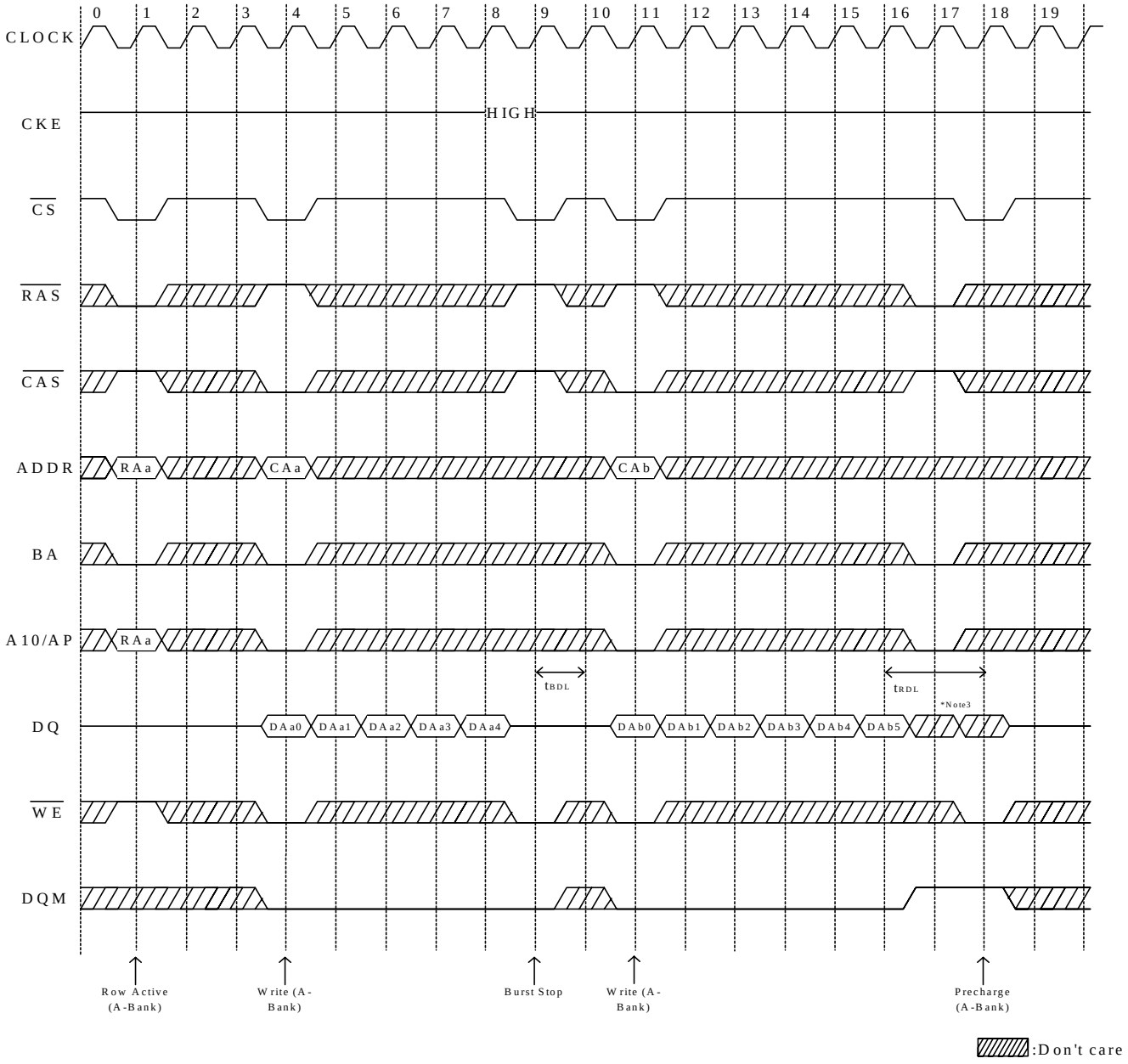


*Note : 1. Burst can't end in full page mode, so auto precharge can't issue.

2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
   Both cases are illustrated above timing diagram. See the lable 1,2 on them.
   But at burst write, burst stop and $\overline{RAS}$ interrupt should be compared carefully.
   Refer the timing diagram of 'Full Page write burst stop cycle'.

3. Burst stop is valid at every burst length.

Write Interrupted by Prechareg Command & Write Burst Stop Cycle @ Burst Length=Full Page

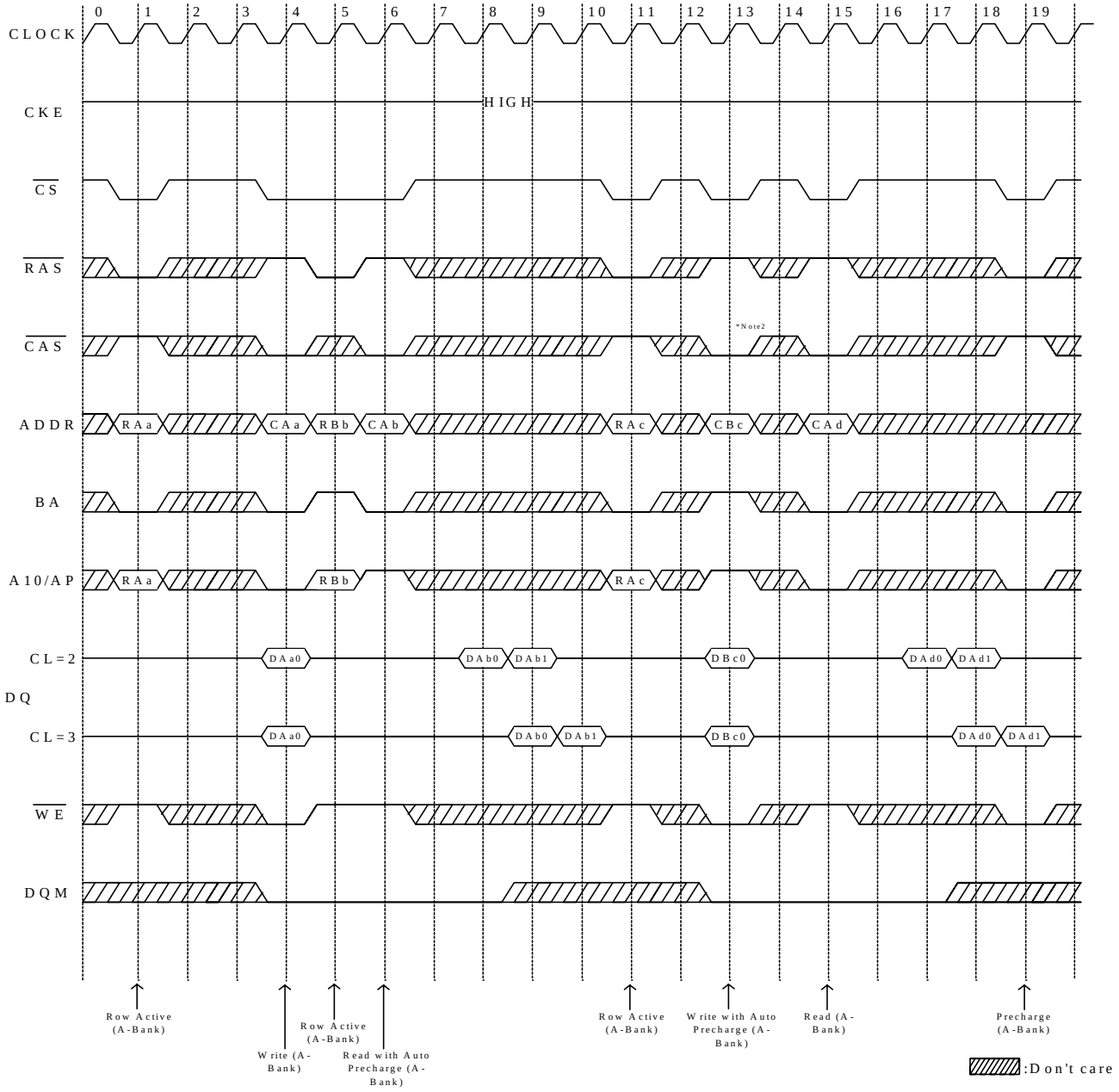


*Note : 1. Burst can't end in full page mode, so auto precharge can't issue.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell.
   It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   Input data after Row precharge cycle will be masked internally.

3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @ Burst Length = 2



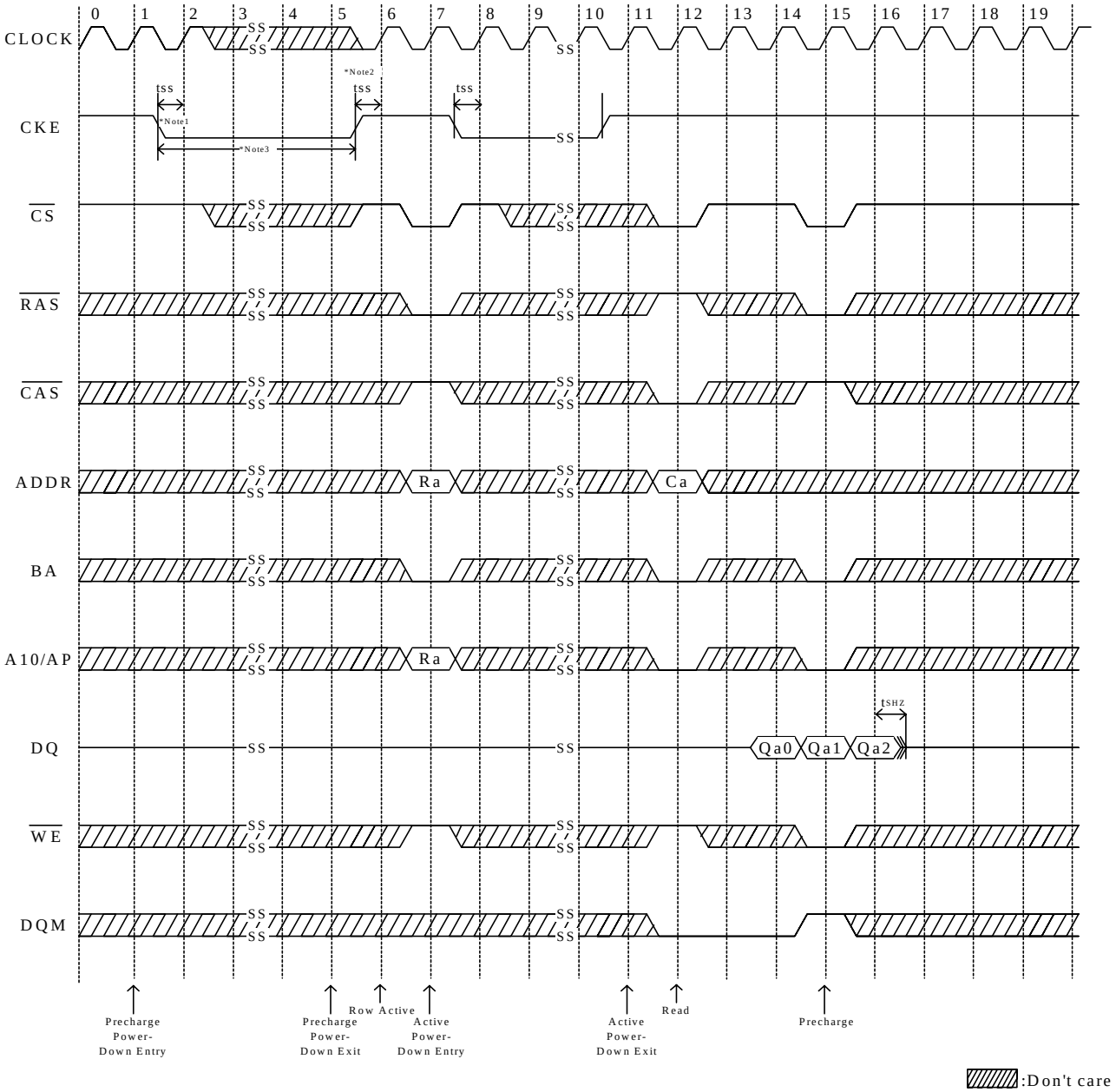
*Note : 1. BRSW modes is enabled by setting A9 'High' at MRS (Mode Register Set).

At the BRSW Mode, the burst length at write is fixed to '1' regardless of programmed burst length.

2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.

Auto precharge is executed at the next cycle of burst-end, so in the case of BRSW write command, the precharge command will be issued after two clock cycle.

Active/ Precharge Power Down Mode @ CAS latency = 2, Butsr length = 4

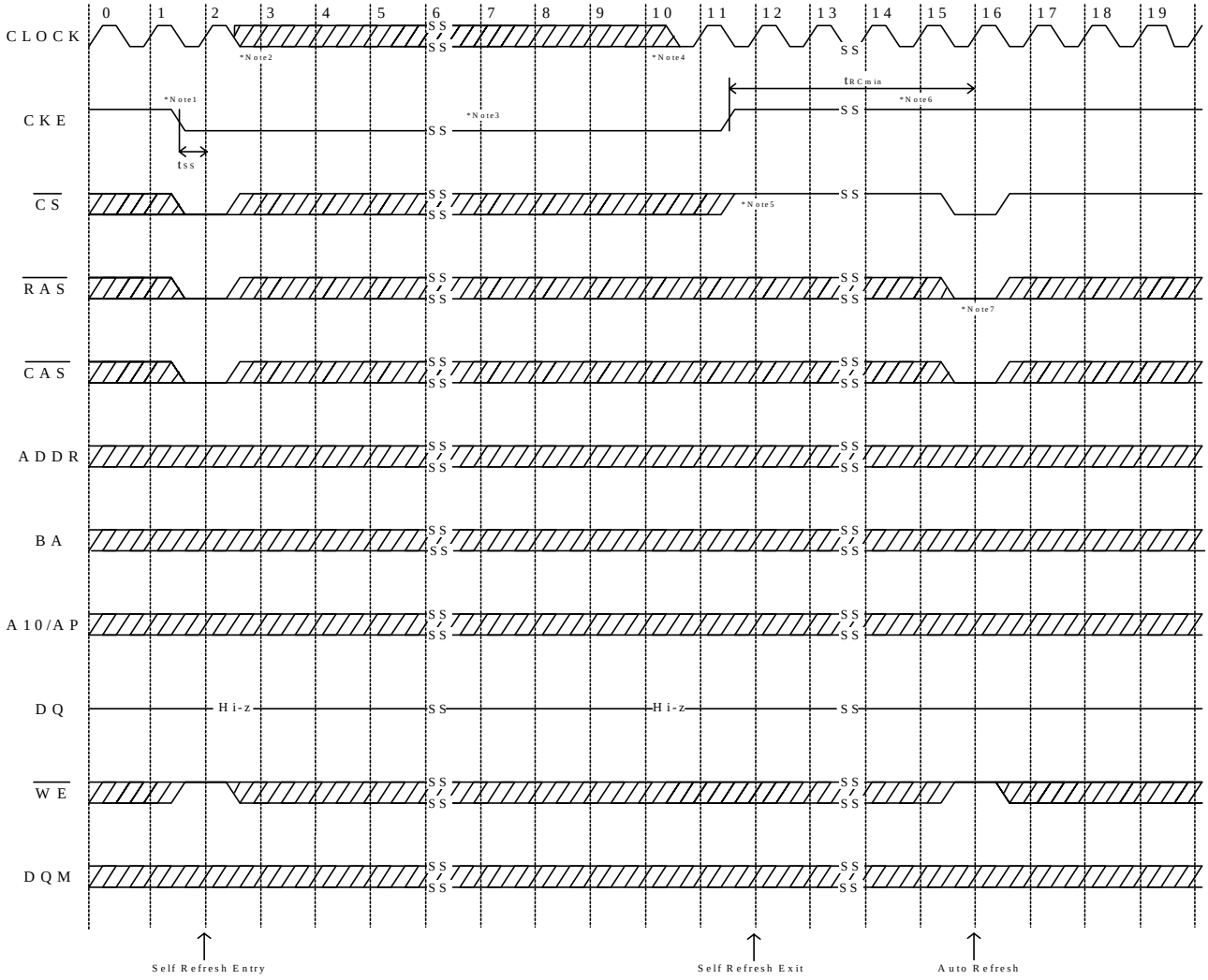


*Note : 1. Both banks should be in idle state prior to entering precharge power down mode.

2. CKE should be set high at least 1CLK+tSS prior to Row active command.

3. Can not violate minimum refresh specification.(64ms)

Self Refresh Entry & Exit Cycle



*Note : TO ENTER SELF REFRESH MODE

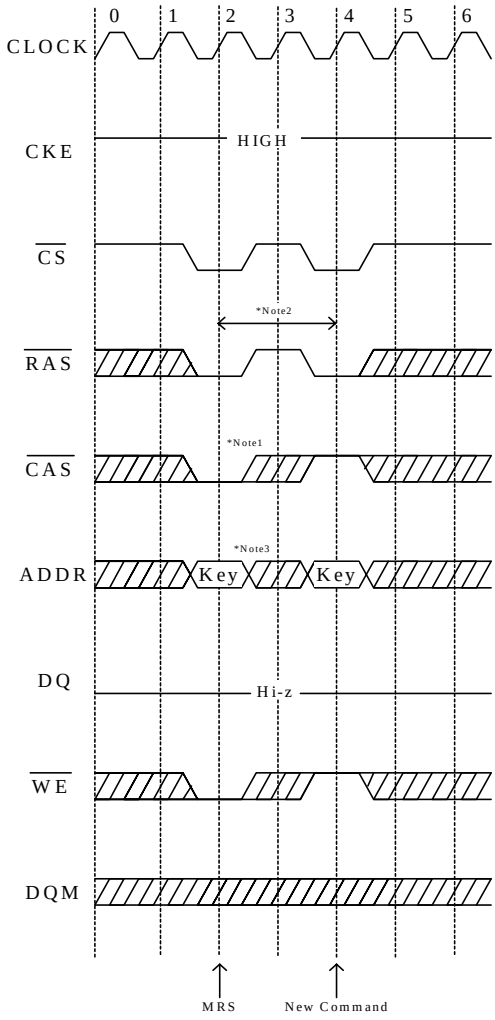
1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs inculding the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays 'Low'.

Cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

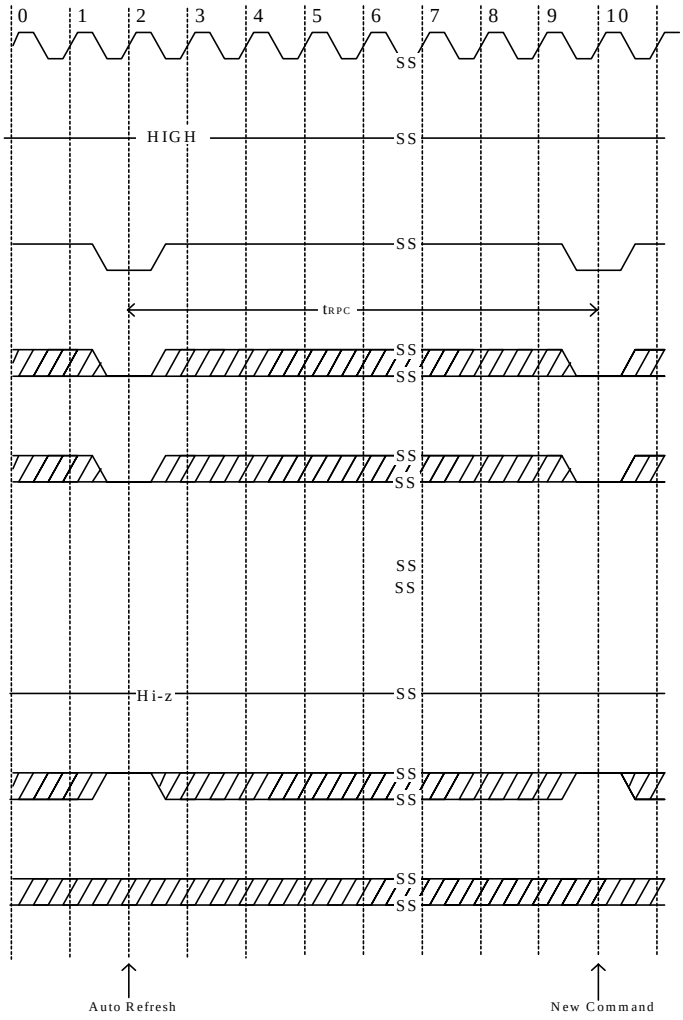
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum tRC is required after CKE going high to complete self refresh exit.
7. 2K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



:Don't care

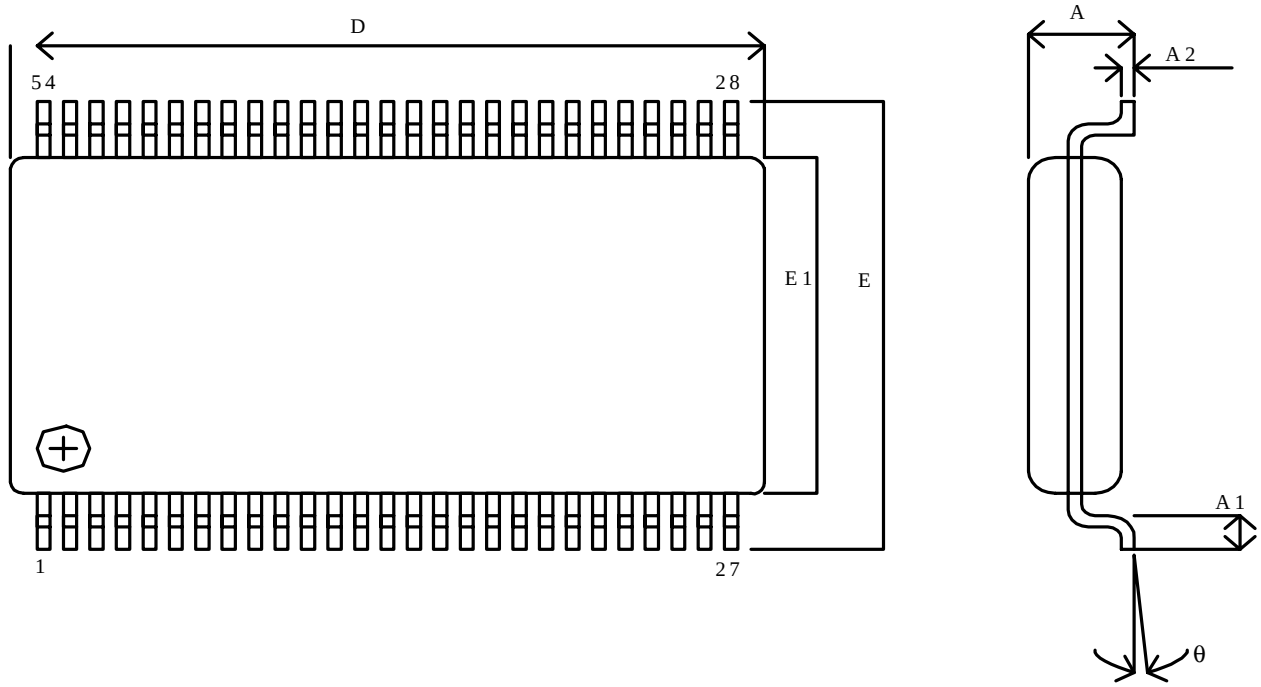
*Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

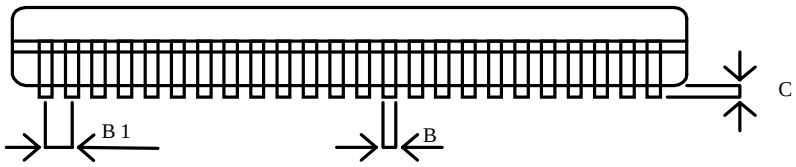
MODE REGISTER SET CYCLE

*Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.

2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

PACKAGE DIMENSIONS
54 LEAD TSOP-II (400 mil)





Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.2	-	-	0.047
A1	0.4	0.5	0.6	0.016	0.020	0.024
A2	-	0.15	-		0.006	
B	0.24	0.32	0.40	0.009	0.012	0.016
B1	-	0.8	-		0.0315	
C	0.05	0.10	0.15	0.002	0.004	0.006
D	22.12	22.22	22.62	0.871	0.875	0.905
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.06	10.16	10.26	0.396	0.400	0.404
θ	0	-	8	0	-	8