

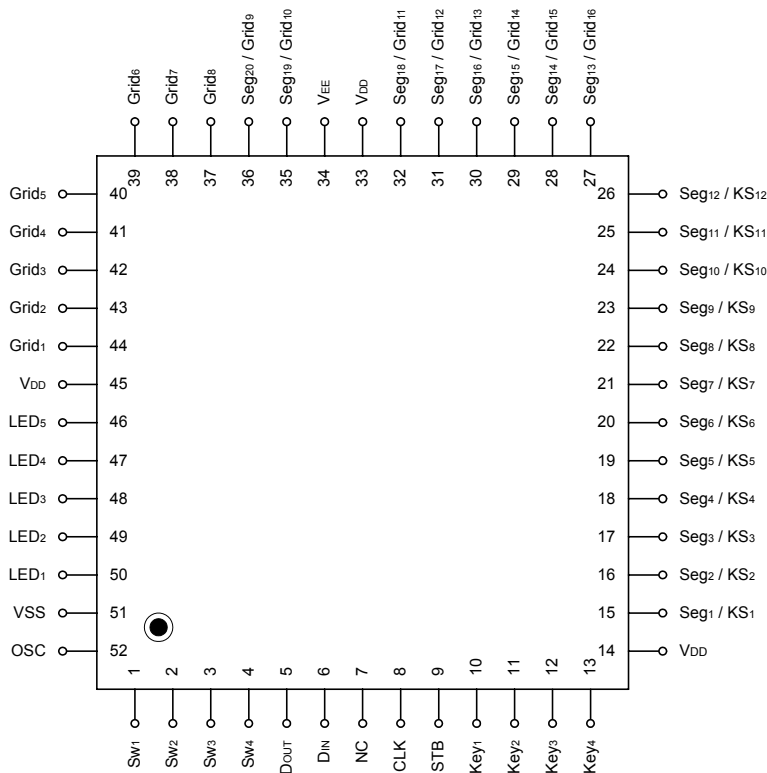
■ Features

- 4-pin serial interface
- Key scanning (12x4 matrices)
- Programming display modes (16-digit & 12-segment to 8-digit & 20-segment)
- Programming dimming step
- High-voltage output (V_{DD} -35V max)
- 5 channels LED ports
- 4-pin general-purpose input port
- Built-in oscillator
- No external resistor necessary for driver outputs

■ General Description

The AD6311 is a VFD (Vacuum Fluorescent Display) controller/driver that is driven on a 1/8- to 1/16 duty factor (include key scan). It consists of 12 segment/key scan output lines, 8 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the AD6311 through a four-line serial interface.

■ Pin Assignments

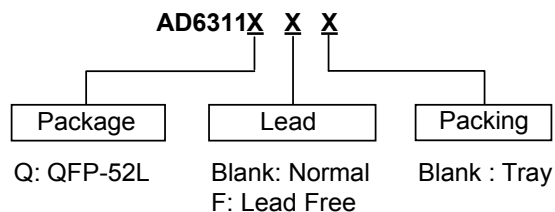


Use all the power pins.

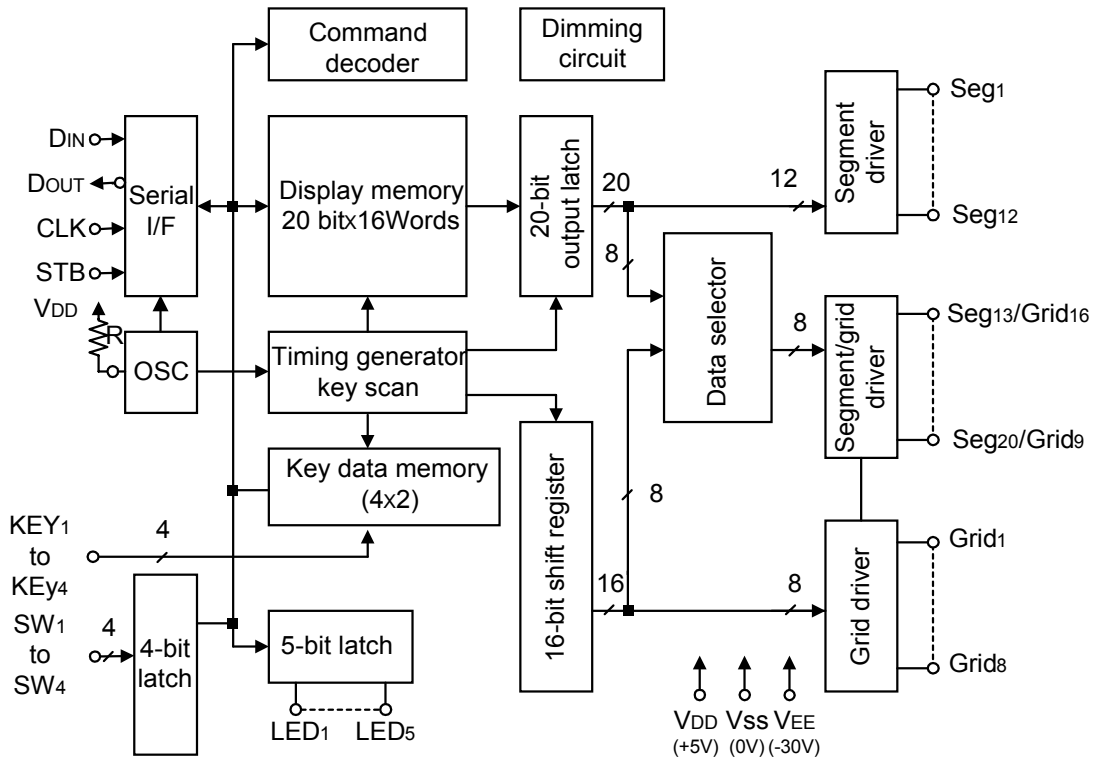
■ Pin Descriptions

Symbol	Name	No.	Description
D _{IN}	Data input	6	Input serial data at rising edge of shift clock, starting from the low order bit.
D _{OUT}	Data output	5	Output serial data at the falling edge of the shift clock, starting from low order bit. This is N-ch open-drain output pin.
STB	Strobe	9	Initializes serial interface at the rising or falling edge of the AD6311. It then waits for reception of a command. Data input after STB falling is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.
CLK	Clock input	8	Reads serial data at the rising edge, and outputs data at the falling edge.
OSC	Oscillator pin	52	Connect resistor in between this pin and V _{DD} to set up the oscillation frequency.
Seg ₁ /KS ₁ to Seg ₁₂ /KS ₁₂	High-voltage output	15 to 26	Multi-function pins, Segment output pins (Dual function as key scan source)
Grid ₁ to Grid ₈	High-voltage output (Grid)	37 to 44	Grid output pins
Seg ₁₃ /Grid ₁₆ to Seg ₂₀ /Grid ₉	High-voltage output (Segment/grid)	27 to 32 35, 36	These pins are selectable for segment or grid driving.
LED ₁ to LED ₅	LED output	46 to 50	CMOS output
KEY ₁ to KEY ₄	Key data input	10 to 13	Data input to these pins is latched at the end of the display cycle.
V _{DD}	Logic power	14, 33, 45	Logic power supply
V _{SS}	Logic ground	51	Connect this pin to system GND.
V _{EE}	Pull-down level	34	Driver power supply
SW ₁ to SW ₄	Switch input	1 to 4	These pins constitute a 4-bit general-purpose input port.
NC	NC	7	No connection

■ Ordering Information



■ Block Diagram





■ Absolute Maximum Ratings $(T_A=25^{\circ}\text{C}, V_{SS}=0\text{V})$

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD}	-0.5 to +7.0	V
Driver supply voltage	V_{EE}	$V_{DD} + 0.5$ to $V_{DD} - 40$	V
Logic input voltage	V_{I1}	-0.5 to $V_{DD} + 0.5$	V
VFD driver output voltage	V_{O2}	$V_{EE} - 0.5$ to $V_{DD} + 0.5$	V
LED driver output current	I_{O1}	+15	mA
VFD driver output current	I_{O2}	-40(grid) -15 (segment)	mA
Operating ambient temperature	T_{OPT}	-25 to +85	$^{\circ}\text{C}$
Storage temperature	T_{STG}	-50 to +125	$^{\circ}\text{C}$

■ Operating Conditions $(T_A=0$ to $+70^{\circ}\text{C}, V_{SS}=0\text{V})$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{DD}		4.5	5	5.5	V
High-level input voltage	V_{IH}		$0.7 \cdot V_{DD}$		V_{DD}	V
Low-level input voltage	V_{IL}		0		$0.3 \cdot V_{DD}$	V
Driver supply voltage	V_{EE}		0		$V_{DD} - 35$	V

■ DC Characteristics $(T_a=0$ to $70^{\circ}\text{C}, V_{DD}=4.5$ to $5.5\text{V}, V_{SS}=0\text{V}, V_{EE}=V_{DD}-35\text{V})$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH1}	LED ₁ -LED ₅ , $I_{OH1}=-1\text{mA}$	$0.9V_{DD}$			V
Low-level output voltage	V_{OL1}	LED ₁ -LED ₅ , $I_{OL1}=12\text{mA}$			1	V
Low-level output voltage	V_{OL2}	$D_{OUT}, I_{OL2}=2\text{mA}$			0.4	V
High-level output current	I_{OH21}	$V_O=V_{DD}-2\text{V}$, Seg ₁ to Seg ₁₂	-3			mA
High-level output current	I_{OH22}	$V_O=V_{DD}-2\text{V}$, Grid ₁ to Grid ₈ , Seg ₁₃ /Grid ₁₆ to Seg ₂₀ /Grid ₉	-15			mA
Driver leakage current	I_{OLEAK}	$V_O=V_{DD}-35\text{V}$, driver off			-10	μA
Output pull-down resistor	R_L	Driver output	50	100	150	$\text{k}\Omega$
High-level input voltage	V_{IH}		$0.7V_{DD}$			V
Low-level input voltage	V_{IL}				$0.3V_{DD}$	V

■ AC Characteristics $(T_a=0$ to $+70^{\circ}\text{C}, V_{DD}=4.5$ to $5.5\text{V})$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	$R=51\text{ k}\Omega$	350	500	650	kHz
Maximum clock frequency	f_{max}	Duty=50%			1	MHz
Clock pulse width	PW_{CLK}		500			ns
Strobe pulse width	PW_{STB}		1			μs
Data setup time	t_{SETUP}		100			ns
Data hold time	t_{HOLD}		100			ns
Clock-strobe time	$t_{CLK-STB}$	CLK \uparrow \rightarrow STB \uparrow	1			μs
Wait time	t_{WAIT}	CLK \uparrow \rightarrow CLK \downarrow (Note)	1			μs

Note: Refer to page 8.

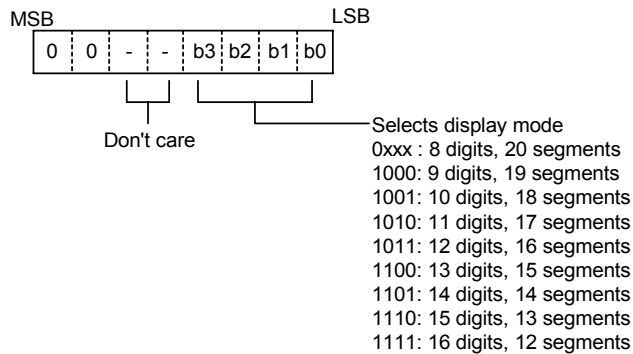
■ Function Description

1.0 Command

A command sets the display mode and status of the VFD driver. The first 1 byte input to the AD6311 through the Din pin after the STB pin has fallen is regarded as a command. If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

1.1 Display mode setting command

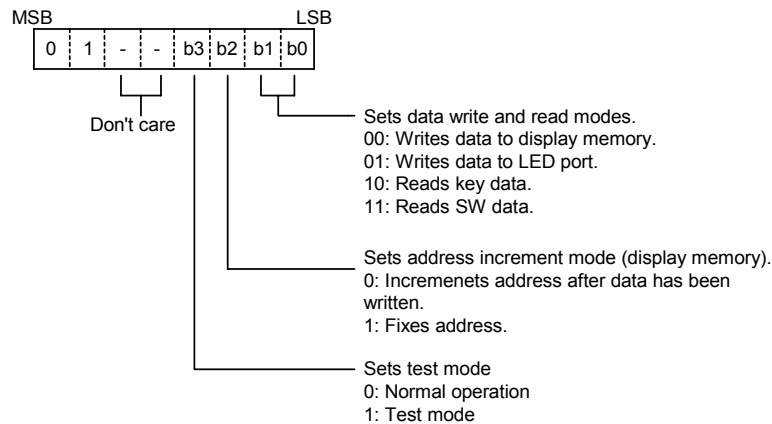
This command initializes the AD6311 and selects the number of segments and number of grids (8 grid & 20 segments to 16 grid & 12 segments). When this command is executed, display is forcibly turned off, and key scanning is also stopped. To resume display, a display ON command must be executed. If the same mode is selected, however, nothing is performed.



On power application, the 16-digit, 12-segment mode is selected.

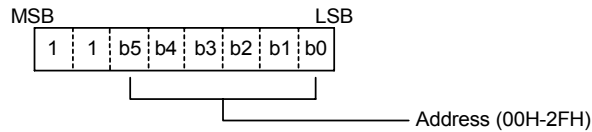
1.2 Data setting command

This command sets data write and data read modes. On power application, the normal operation mode and address increment mode are set.

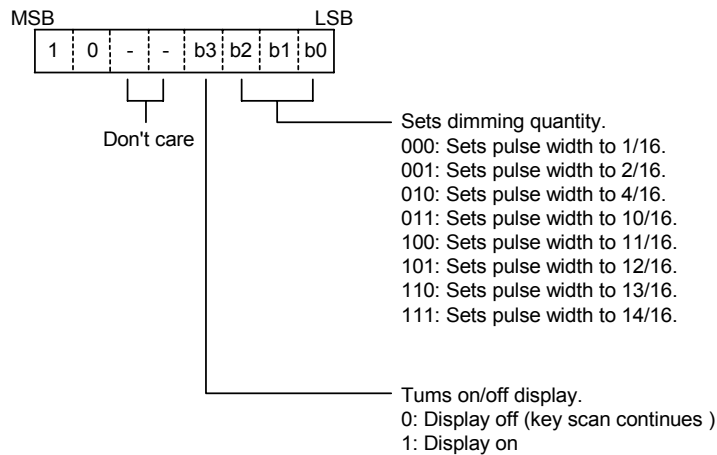


1.3 Address setting command

This command sets an address of the display memory. If address 30H or higher is set, the data is ignored, until a correct address is set. On power application, the address is set to 00H.



1.4 Display control command



On power application, the 1/16-pulse width is set, the display is turned off and key scanning is stopped.

2.0 Display RAM Address and Display Mode

The display RAM stores the data transmitted from an external device to the AD6311 through the serial interface, and is assigned addresses as follows, in units of 8 bits:

Seg ₁	Seg ₄	Seg ₈	Seg ₁₂	Seg ₁₆	Seg ₂₀	
00 H _L	:00 H _U	01 H _L	:01 H _U	02 H _L		GRID ₁
03 H _L	:03 H _U	04 H _L	:04 H _U	05 H _L		GRID ₂
06 H _L	:06 H _U	07 H _L	:07 H _U	08 H _L		GRID ₃
09 H _L	:09 H _U	0 A H _L	:0 A H _U	0 B H _L		GRID ₄
0 C H _L	:0 C H _U	0 D H _L	:0 D H _U	0 E H _L		GRID ₅
0 F H _L	:0 F H _U	10 H _L	:10 H _U	11 H _L		GRID ₆
12 H _L	:12 H _U	13 H _L	:13 H _U	14 H _L		GRID ₇
15 H _L	:15 H _U	16 H _L	:16 H _U	17 H _L		GRID ₈
18 H _L	:18 H _U	19 H _L	:19 H _U	1 A H _L		GRID ₉
1 B H _L	:1 B H _U	1 C H _L	:1 C H _U	1 D H _L		GRID ₁₀
1 E H _L	:1 E H _U	1 F H _L	:1 F H _U	20 H _L		GRID ₁₁
21 H _L	:21 H _U	22 H _L	:22 H _U	23 H _L		GRID ₁₂
24 H _L	:24 H _U	25 H _L	:25 H _U	26 H _L		GRID ₁₃
27 H _L	:27 H _U	28 H _L	:28 H _U	29 H _L		GRID ₁₄
2 A H _L	:2 A H _U	2 B H _L	:2 B H _U	2 C H _L		GRID ₁₅
2 D H _L	:2 D H _U	2 E H _L	:2 E H _U	2 F H _L		GRID ₁₆
b0	b3 b4	b7				
XX H _L	XXX H _U					

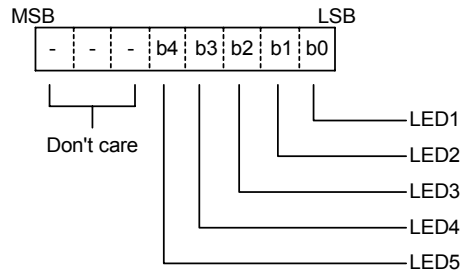
1/8- to 1/16 Duty VFD Controller/Driver

Lower 4 bits Higher 4 bits

Only the lower 4 bits of the addresses assigned to Seg₁₇ through Seg₂₀ are valid, and the higher 4 bits are ignored.

3.0 LED Port

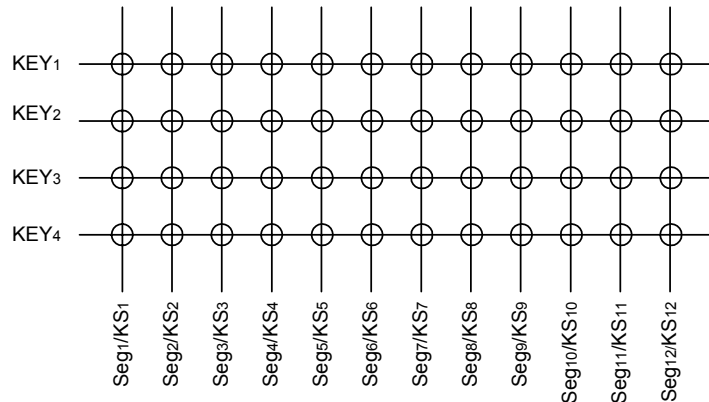
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights; when the bit is 1, the LED goes off. The data of bits 6 through 8 is ignored.



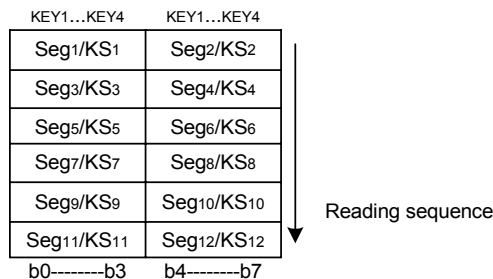
On power application, all the LEDs remain dark.

4.0 Key Matrix and Key-Input data Storage RAM

The key matrix is of 12x4 configuration, as shown below.

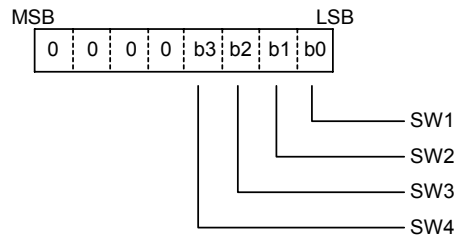


The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit. When the most significant bit of data (Seg₁₂ b₇) has been read, the least significant bit of the next data (Seg₁ b₀) is read.



5.0 SW Data

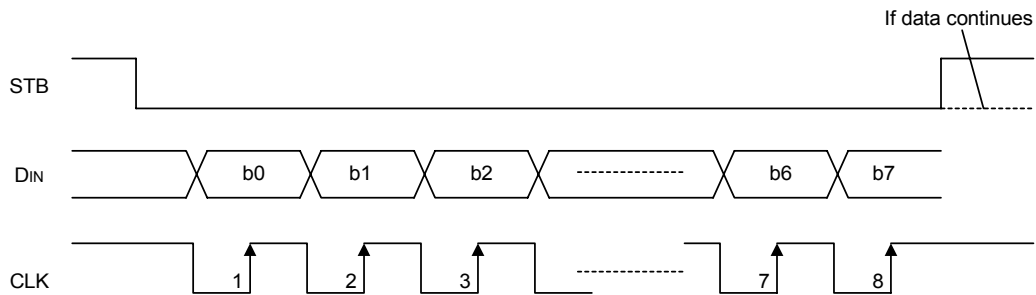
The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



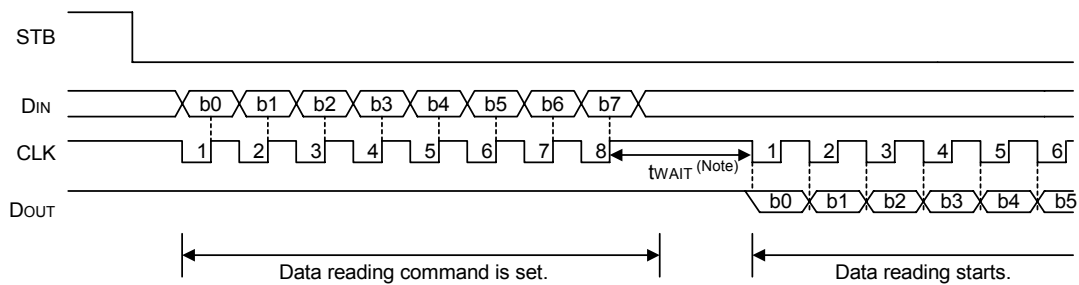
■ Timing Diagram

(1) Serial Communication Format

Reception (command/write data)



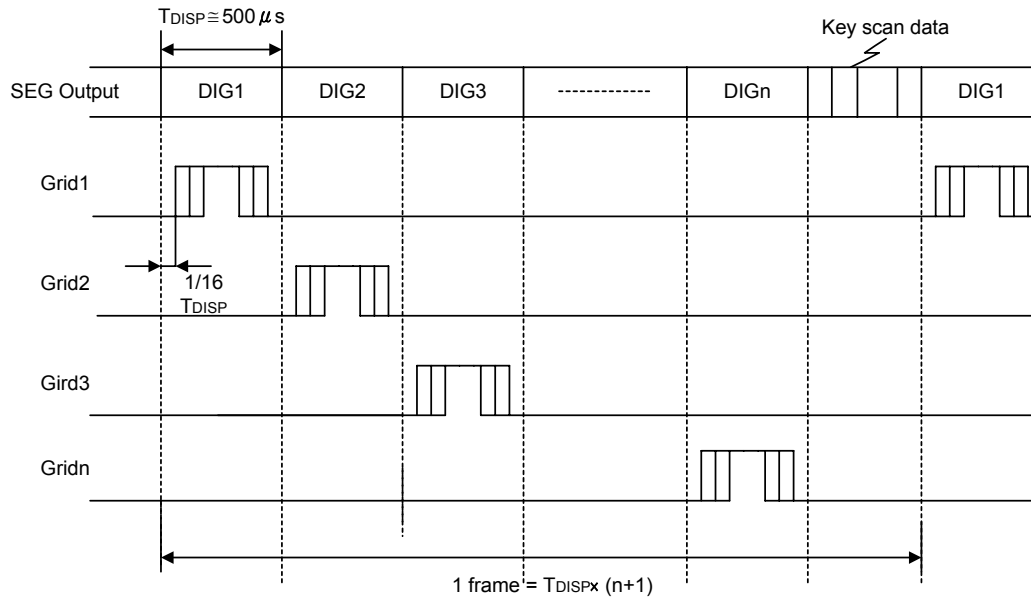
Transmission (read data)



Because the D_{OUT} pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1kΩ to 10 kΩ).

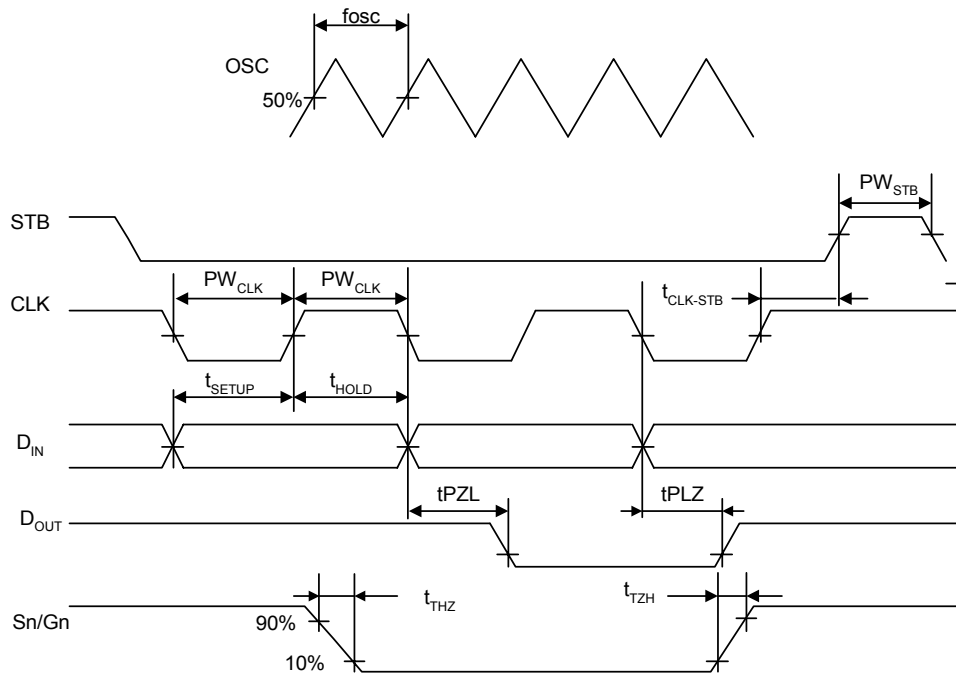
Note : When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

(2) Key Scanning and Display Timing



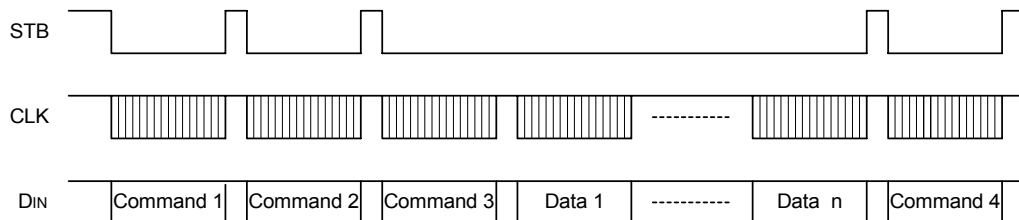
One cycle of key scanning consists of two frames, and data of 12x 4 matrices is stored in RAM.

AC characteristic waveform



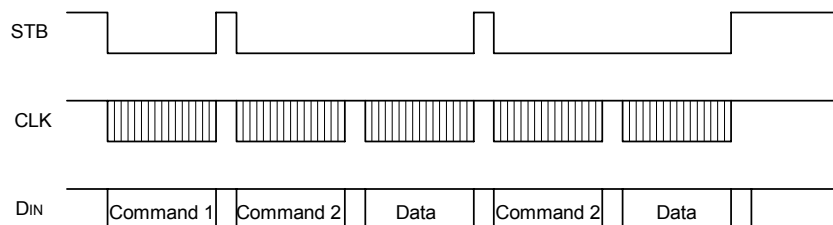
Applications

Updating display memory by incrementing address



Command 1: sets display mode
 Command 2: sets data(write data to display memory)
 Command 3: sets address
 Data 1 to n: transfers display data (48 bytes max.)
 Command 4: controls display

Updating specific display memory

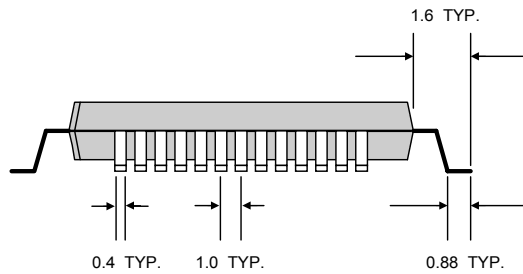
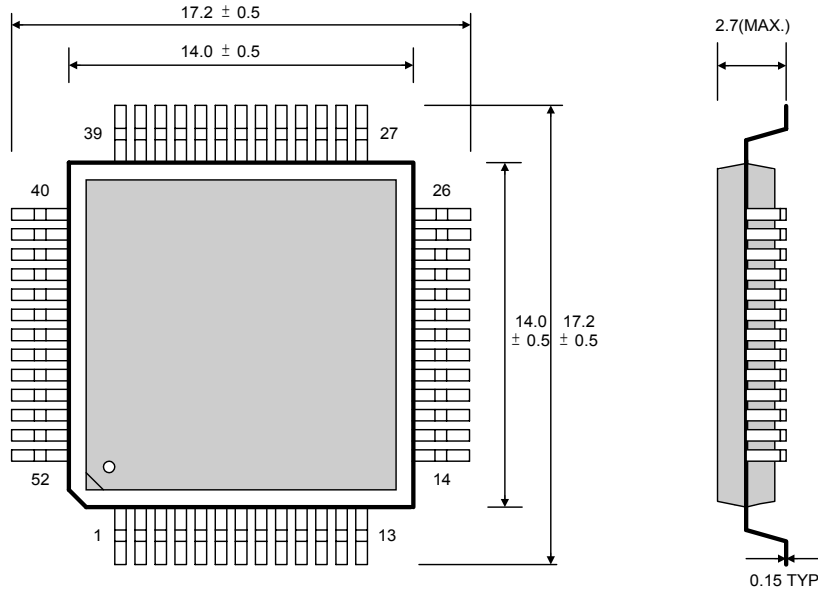


Command 1: sets data
 Command 2: sets address
 Data: display data

■ Package Information

52 pins QFP dimension

Unit: mm



■ Marking Information

