SONY

CXA7002R

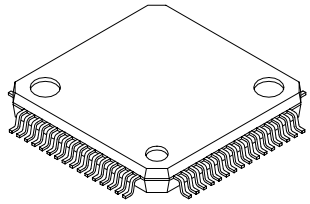
I²C Bus Compatible Audio Video (AV) Switch & Electronic Volume Control

Description

The Sony CXA7002R is an Audio/Video switch designed primarily for application in Digital Set Top Boxes. It provides video and audio routing from the digital encoder source to the TV and VCR scart (peri-television) connectors. In addition, the TV audio output has a programmable volume control. The chip is programmed by means of an I²C interface and can operate from a single or dual power supply.

Target specifications: Canal+, BSkyB, TPS, NorDig, and ECCA Euro-Box

64 pin LQFP (Plastic)



Features

Supply

- Single: 0V, +5V, +12V
- Dual: 0V, –5V, +5V and +12V
  (Low number of external parts required)

Video

- 2 scart switching (VCR, TV)
- VCR input supports RGB mode
- Integrated 75Ω drivers for direct video connection
- Y/C mixer with trap for RF modulators
- Switchable clamps on inputs
- Low pass filters on six inputs
- Controllable gain on encoder inputs
- Adjustable gain on RGB outputs
- Video output shutdown for low power modes
- Fast blanking switch
- Slow blanking switch for TV and VCR output
- SVHS switch on VCR output
- Y/C auxiliary input

Audio

- Four stereo audio inputs
- Volume control (–56dB to +6dB in 2dB steps)
- Additional +6dB gain on audio DAC inputs
- Audio overlay facility
- Volume bypass for TV and Phono outputs
- Mono switching on TV, VCR outputs
- Switchable audio limiter function
- Switchable Mono output for RF modulators
- Audio output disable for standby mode

I²C and Logic

- Fast mode compatible I²C bus
- Function monitor with loop through
- Interrupt output for function monitor and sync detect
- Logic output pin
- Sync detector for Y/CVBS inputs

Applications

- Digital Set Top Box
- Integrated digital television

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C) **unless stated**

• Supply voltage	V_{CC}	14	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.1	W
(when mounted on the board)			

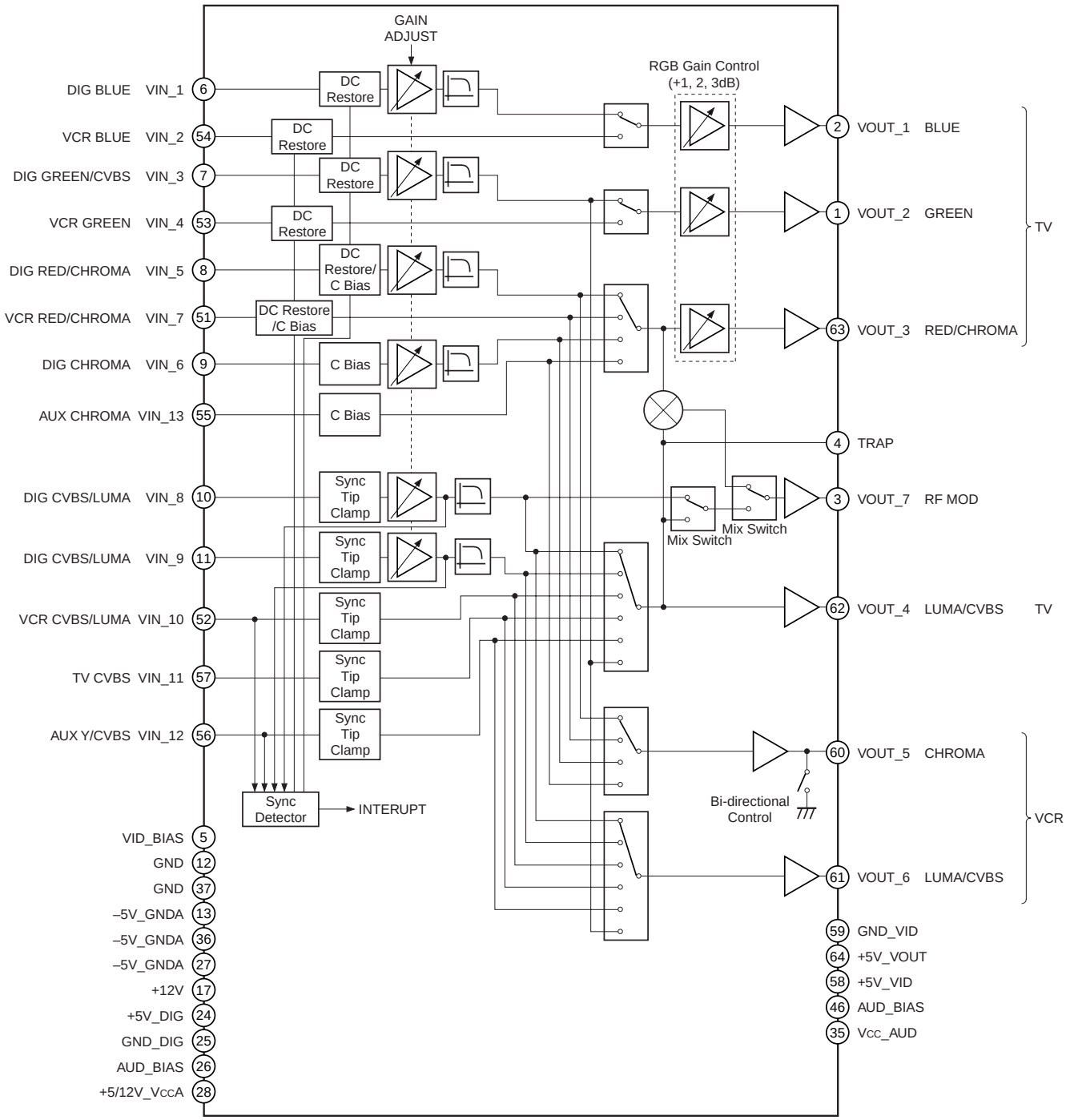
Operating Conditions

• Single supply		12 ± 0.6	V
		5 ± 0.25	V
• Dual supply		–5 ± 0.25	V
		5 ± 0.25	V
		12 ± 0.6	V
• Operating temperature	Topr	–20 to +75	°C
• Maximum ESD voltage		±2	kV
(Human Body Model)			

E02750A41

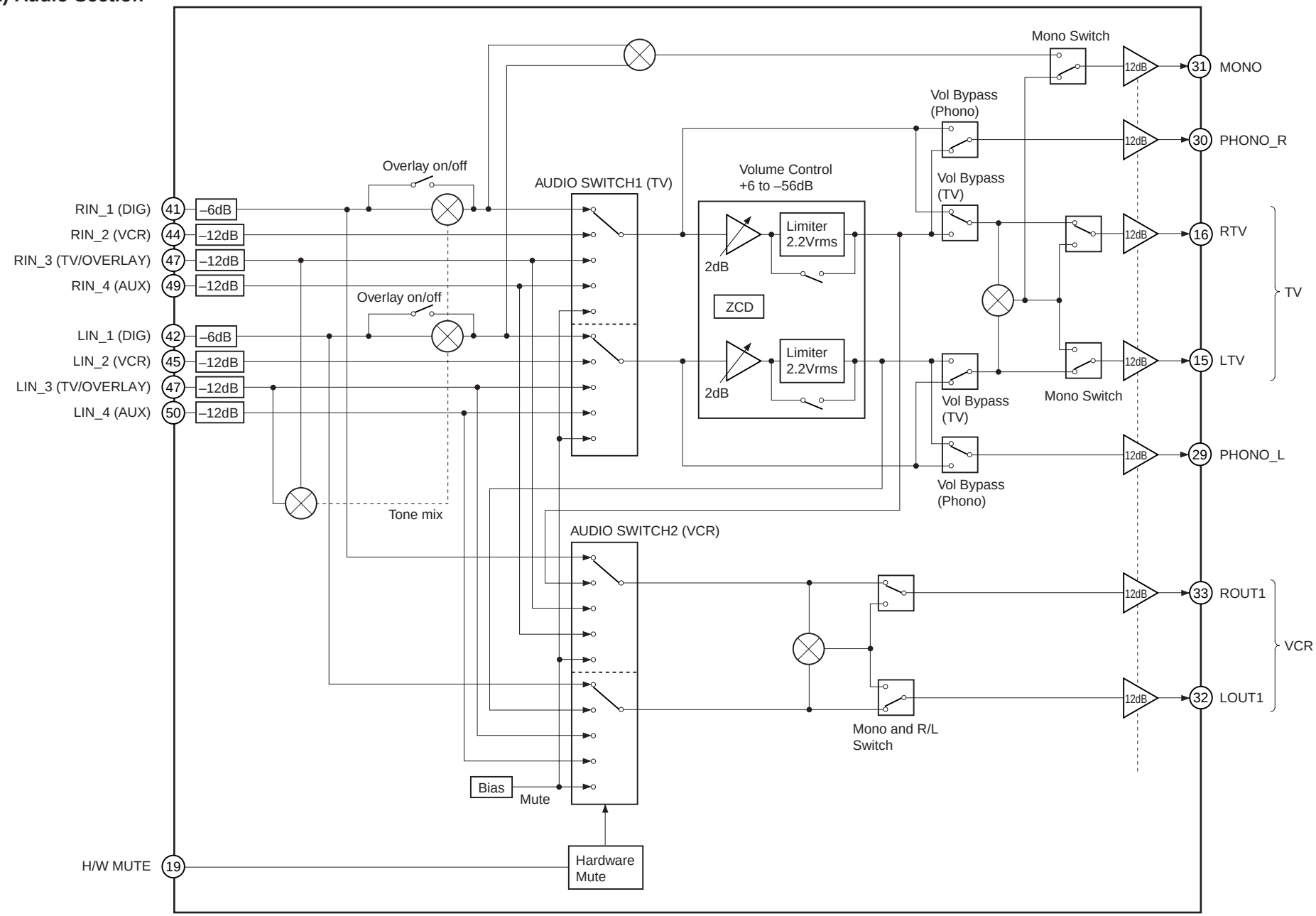
Block Diagram

(1) Video Section

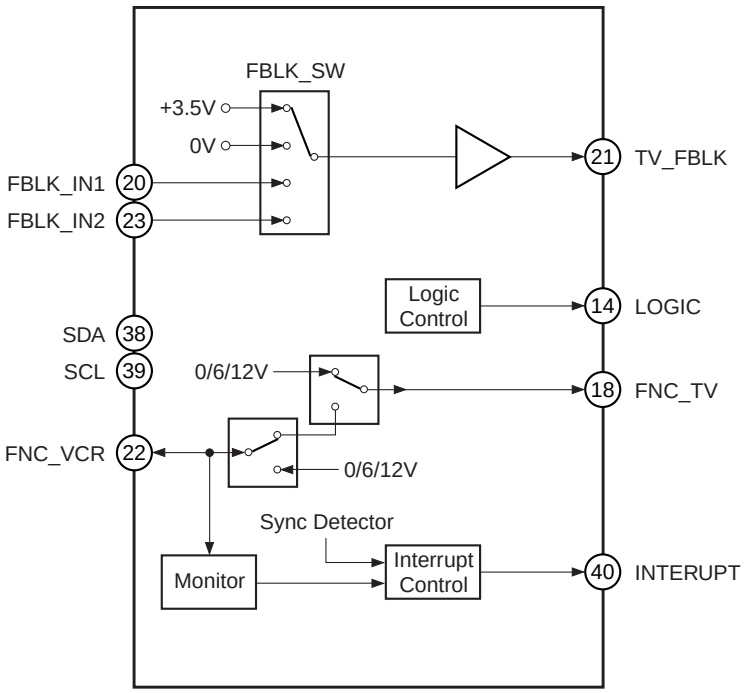


Note) All video outputs contain 75Ω drivers.

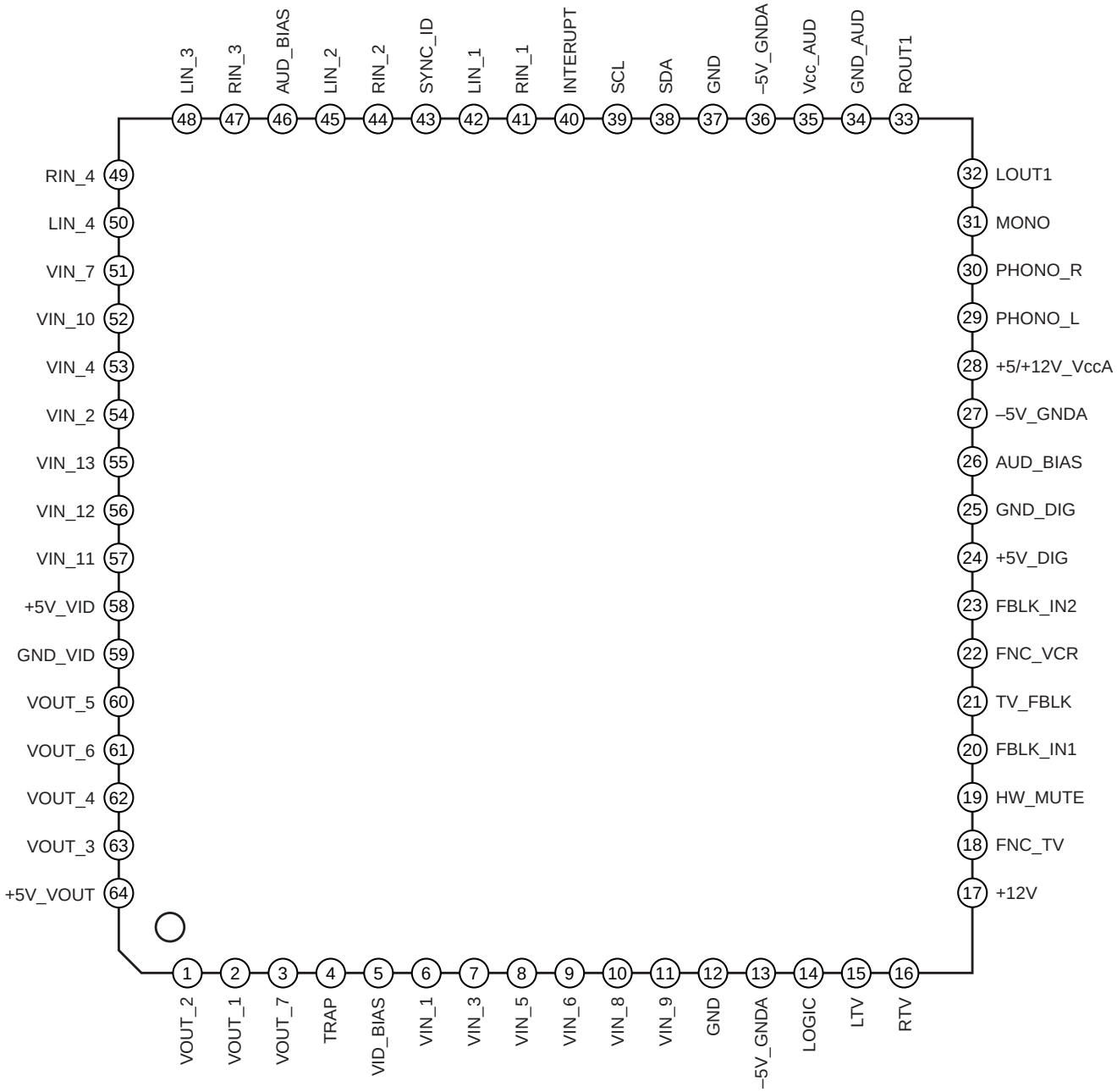
(2) Audio Section



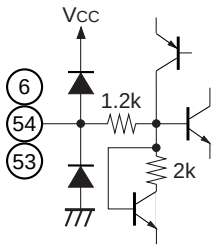
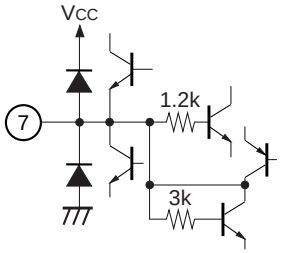
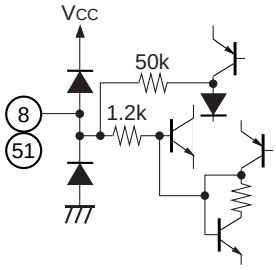
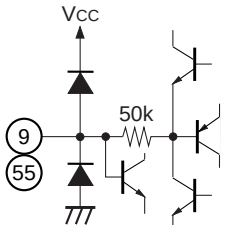
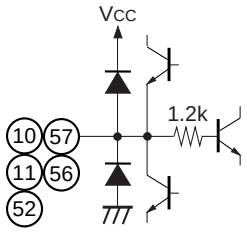
(3) Digital Section

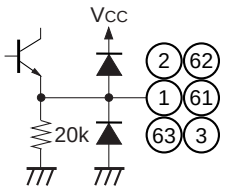
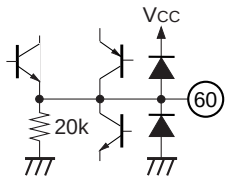
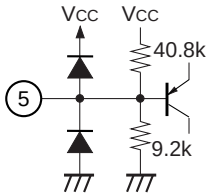
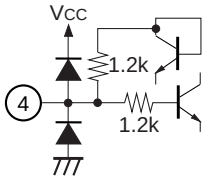
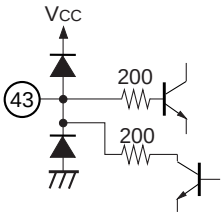
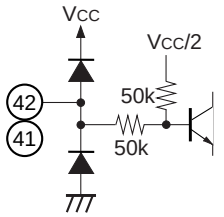
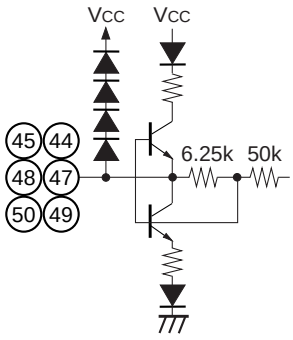


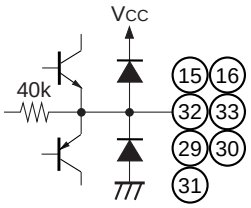
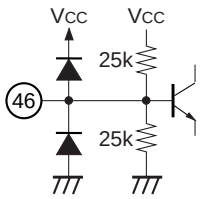
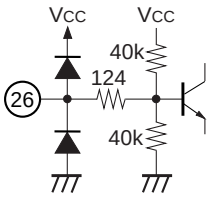
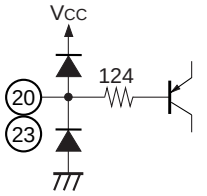
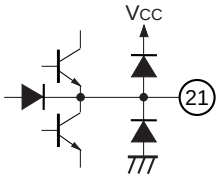
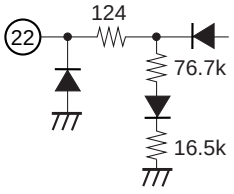
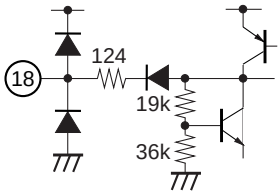
Pin Configuration

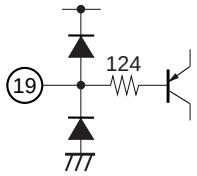
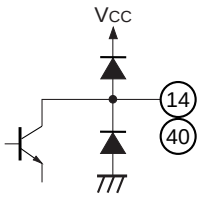
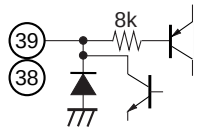


Pin Description

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
6 54 53	VIN_1 VIN_2 VIN_4	2.5		RGB signal inputs
7	VIN_3	2.5 2.4		RGB signal input or CVBS signal input
8 51	VIN_5 VIN_7	2.5 3.1		RGB signal inputs or Chrominance signal inputs
9 55	VIN_6 VIN_13	3.1		Chrominance signal inputs
10 11 52 57 56	VIN_8 VIN_9 VIN_10 VIN_11 VIN_12	2.4		CVBS/Luminance signal inputs

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
2 1 63 62 61 3	VOUT_1 VOUT_2 VOUT_3 VOUT_4 VOUT_6 VOUT_7	0.6		RGB/CVBS signal outputs
60	VOUT_5	1.8		Chrominance signal output
5	VID_BIAS	0.9		Internal reference bias for video circuits. A capacitor is connected from this pin to GND. Typically 100nF
4	TRAP	2.4		Connects trap circuit for subcarrier
43	SYNC_ID	2.5		Sync detect circuit time constant, resistor and capacitor connection pin
42 41	LIN_1 RIN_1	2.5		Audio signal inputs
45 44 48 47 50 49	LIN_2 RIN_2 LIN_3 RIN_3 LIN_4 RIN_4	2.5		Audio signal inputs

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description	
15 16 32 33 29 30 31	LTV RTV LOUT1 ROUT1 PHONO_L PHONO_R MONO	6.0 (Single) 0.0 (Dual)		Audio signal outputs	
46	AUD_BIAS	2.5V (Single/ Dual)		Internal reference bias for audio circuit	Capacitor connected to GND. (Typically 22µF)
26	AUD_BIAS	6.0 (Single)		Internal reference bias for audio circuit	Capacitor connected to GND. (Typically 22µF)
		0.0 (Dual)			Connected directly to GND.
20 23	FBLK_IN1 FBLK_IN2	—		Fast blanking signal inputs	
21	TV_FBLK	—		Fast blanking signal output	
22	FNC_VCR	—		SCART function pin 8 input/output to VCR	
18	FNC_TV	—		SCART function pin 8 output to TV	

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
19	HW_MUTE	—		Mutes audio outputs when pin voltage is below 2V. This pin is normally connected to +5V.
14	LOGIC (Vcc = +12V)	—		Open connector logic outputs Typically connect to +5V through 10kΩ resistor.
40	INTERUPT (Vcc = +5V)	—		
39	SCL	—		I^2C bus clock line
38	SDA			I^2C bus data line
24	+5V_DIG	5.0		Digital supply
64	+5V_VOUT			Video output supply
58	+5V_VID			Video supply
35	Vcc_AUD			Audio supply
17	+12V	12.0		Digital supply
13 17 36	–5V_GNDA	–5.0 (Dual) 0.0 (Single)		Audio supply/ground
28	+5V/12V_VccA	5.0 (Dual) 12.0 (Single)		Audio supply
12 37	GND	0.0		
25	GND_DIG	0.0		Digital ground
34	GND_AUD	0.0		Audio Ground
59	GND_VID	0.0		Video ground

Electrical Characteristics

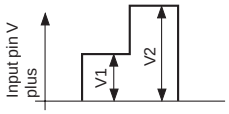
Nominal conditions (Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (Single ended supply)	Icc1	+12 supply, no signal, no load	—	30	55	mA
	Icc2	+5 supply, no signal, no load	—	60	85	mA
Current consumption (Dual supply)	Icc3	+12 supply, no signal, no load	—	10	30	mA
	Icc4	+5 supply, no signal, no load	—	80	110	mA
	Icc5	–5 supply, no signal, no load	–50	–20	—	mA

(1) Video System

Nominal conditions single supply (Ta = 25°C, +5V/12V_VccA = +12V, –5V_GNDA = 0V, +5V_VID = +5V, +5V_VOUT = +5V, +5V_DIG = +5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sync tip clamp voltage at input	Vclmp1	Vin3, Vin8, Vin9, Vin10, Vin11, Vin12 inputs. (Vin3 set to CVBS mode) (Fig. 1)	—	2.4	—	V
Chroma bias input voltage	Cbias1	Vin5, Vin7 inputs. Clamps set to Chroma bias mode. (Fig. 1)	—	3.1	—	V
	Cbias2	Vin6, Vin13 inputs. (Fig. 1)	—	2.45	—	V
RGB dc restore input voltage	RGB1	Vin1, Vin2, Vin3, Vin4, Vin5, Vin7 inputs. (Vin3 & Vin5 set to RGB mode) (Fig. 1)	—	2.5	—	V
Sync tip clamp voltage at output	Vclmp2	Vout4, Vout6 outputs (Fig. 1)	—	0.3	—	V
Chroma bias output voltage	Cbias3	Vout3, Vout5 outputs (Fig. 1)	—	1.8	—	V
RGB dc restore output voltage	RGB2	Vout1, Vout2, Vout3 outputs (Fig. 1)	—	0.6	—	V
Gain (Vout1 to 7)	GVv	f = 200kHz, 0.3Vp-p input, RGB Gain = 0dB, Input Gain = 0dB (Fig. 2)	5.5	6.0	6.5	dB
Gain (Vout1, 2, 3)	GV_{RGB1}	f = 200kHz, 0.3Vp-p input, RGB Gain = +1dB, Input Gain = 0dB (Fig. 2)	6.5	7.0	7.5	dB
	GV_{RGB2}	f = 200kHz, 0.3Vp-p input, RGB Gain = +2dB, Input Gain = 0dB (Fig. 2)	7.5	8.0	8.5	dB
	GV_{RGB3}	f = 200kHz, 0.3Vp-p input, RGB Gain = +3dB, Input Gain = 0dB (Fig. 2)	8.5	9.0	9.5	dB
Video input gain Vin 1, 3, 5, 6, 8, 9	$G_{i/p1}$	f = 200kHz, 0.3Vp-p input, Video gain = +1dB (Fig. 2)	6.5	7.0	7.5	dB
	$G_{i/p1}$	f = 200kHz, 0.3Vp-p input, Video gain = +3dB (Fig. 2)	8.5	9.0	9.5	dB
	$G_{i/p1}$	f = 200kHz, 0.3Vp-p input, Video gain = +6dB (Fig. 2)	11.5	12.0	12.5	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bandwidth (Vout1 to 6)	f_{V3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB. Filter Bypassed. (Fig. 2)	15	30	—	MHz
Bandwidth (Vout7) Mixer on – No trap components	f_{V3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB. (Fig. 2)	8	30	—	MHz
Input dynamic range	V_{DRVI}	200kHz input applied to any video (Fig. 2)	1.4	—	—	Vp-p
Output dynamic range	V_{DRVO}	200kHz input applied to any video (Fig. 2)	2.8	—	—	Vp-p
Cross talk	Vctv	f = 4.43MHz, 1Vp-p input (Fig. 2)	—	–65	—	dB
Fast blanking to RGB delay	Del_{FB}	Falling edge delay from RGB to fast blank signal. Measured at 20% level. (Fig. 2)			50	ns
Vout5 impedance when switched to ground	Z_{Vout5}	2V applied to Vout5 with series 75Ω resistor. Measured voltage at pin and calculate Zout. (Fig. 2)	—	1	—	Ω
S/N ratio	S/N_V	Ratio of 0.7Vp-p white video signal to "black line" noise. Weighted using CCIR 567. HPF@5kHz, LPF@5MHz. (Fig. 2)	—	74	—	dB
Non-linearity	Lin	 V1 = Pin voltage + 0.5V, V2 = Pin voltage + 1V At output, non-linearity = $\left(\frac{V2}{V1 \times 2} - 1\right) \times 100$ (Fig. 2)	–4	0	4	%
Differential gain	DG	1.7Vp-p 5-step modulated staircase. (Chroma & Burst are 150mVp-p, 4.43MHz) (Fig. 2)	–3	0	3	%
Differential phase	DP	As above. (Fig. 2)	–3	0	3	deg
Filter specification						
Attenuation @27MHz	Attn	Measured 27MHz signal relative to signal at 1MHz. (Fig. 2)	—	–47	–24	dB

Audio System

Unless otherwise stated: input coupling capacitor 1µF; output coupling capacitor of 10µF; load of 10kΩ.

Nominal conditions single supply (Ta = 25°C, +5V/12V_V_{CC}A = +12V, –5V_GNDA = 0V, +5V_VID = +5V, +5V_VOUT = +5V, +5V_DIG = +5V, GND_VID = 0V)

Nominal conditions dual supply (Ta = 25°C, +5V/12V_V_{CC}A = +5V, –5V_GNDA = –5V, +5V_VID = +5V, +5V_VOUT = +5V, +5V_DIG = +5V, GND_VID = 0V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin voltage (Single/Dual supply)		V_{APIN1}	No signal, no load (Fig. 3)	2.25	2.5	2.75	V
Output pin voltage (Single supply)		V_{APIN2}	No signal, no load (Fig. 3)	5.75	6	6.25	V
Output pin voltage (Dual supply)		V_{APIN2}	No signal, no load (Fig. 3)	–0.25	0	0.25	V
Output pin voltage when disabled (Single/Dual supply)		V_{APIN3}	No signal, no load (Fig. 3)	–0.25	0	0.25	V
Gain							
Input	Output						
Rin1 or Lin1	TV or Phono	GV_{A1}	f = 10kHz, 0.3Vp-p input (Fig. 4)	5.7	6.2	6.7	dB
Rin1 or Lin1	VCR	GV_{A2}	f = 10kHz, 0.3Vp-p input (Fig. 4)	5.7	6.2	6.7	dB
Rin1 + Lin1	TV (mono mix)	GV_{A3}	f = 10kHz, 0.3Vp-p stereo input, TV volume set to 0dB, TV mono switch on (Fig. 4)	5.7	6.2	6.7	dB
Rin1 + Lin1	MONO	GV_{A4}	f = 10kHz, 0.3Vp-p stereo input, TV volume set to 0dB **(Note 1)** (Fig. 4)	5.7	6.2	6.7	dB
Rin2, 3, 4 or Lin2, 3, 4	TV, VCR, Phono	GV_{A5}	f = 10kHz, 0.3Vp-p input, TV volume set to 0dB (Fig. 4)	–0.3	0.2	0.7	dB
Rin1 + Lin1	VCR (mono mix)	GV_{A6}	f = 10kHz, 0.3Vp-p stereo input, VCR mono switch on (Fig. 4)	5.7	6.2	6.7	dB
Rin2 + Lin2 Rin3 + Lin3 Rin4 + Lin4	MONO	GV_{A7}	f = 10kHz, 0.3Vp-p stereo input, TV volume set to 0dB **(Note 1)** (Fig. 4)	–0.3	0.2	0.7	dB
Rin2 + Lin2 Rin3 + Lin3 Rin4 + Lin4	VCR (mono mix)	GV_{A9}	f = 10kHz, 0.3Vp-p input, VCR mono switch on (Fig. 4)	–0.3	0.2	0.7	dB
Rin3	RTV, ROUT1, Phono_R	GV_{A10}	f = 10kHz, 0.3Vp-p, Lin3 has no signal Audio overlay enabled. (Fig. 4)	–12.5	–11.75	–11.25	dB
Lin3	LTV, LOUT1, Phono_L	GV_{A11}	f = 10kHz, 0.3Vp-p input Audio overlay enabled. (Fig. 4)	–12.5	–11.75	–11.25	dB

Note 1) Mono switch set to mix RTV & LTV after volume control.

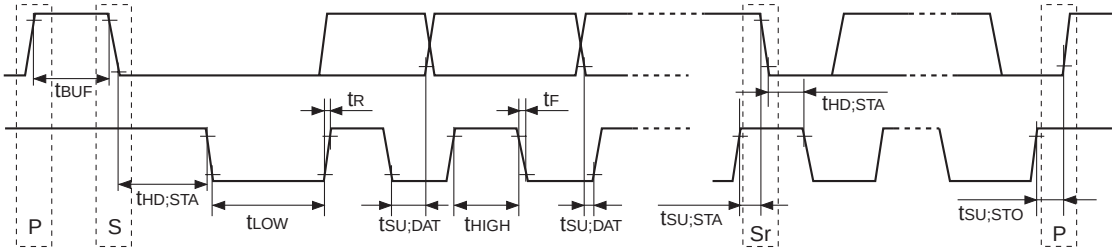
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Audio frequency response	F_{AF}	0.3Vp-p input. Output/Input gain at 30kHz with 10kHz serving as 0dB (Fig. 4)	–0.3	0	0.3	dB
Distortion	THD	f = 1kHz, 0.5Vrms, unweighted response; LPF @400Hz, HPF @80kHz (Fig. 4)	—	0.005	0.1	%
Input dynamic range Rin2, 3, 4/Lin2, 3, 4	Vd_{A1}	f = 1kHz, RIN1/LIN1 input amplifier set to –6dB. Dual supply mode used. (Fig. 4)	2.5	2.9	—	Vrms
Input dynamic range Rin1/Lin1	Vd_{A1}	f = 1kHz (Fig. 4)	1.25	1.45	—	Vrms
Cross talk (Channel separation)	Vct_A	f = 10kHz, 1Vrms input on one input, measure on any audio output (Fig. 4)	—	–90	—	dB
Input impedance Rin1, 2, 3, 4/Lin1, 2, 3, 4	Zin1	(Excluding any external series resistor) (Fig. 4)	—	100	—	dB
S/N ratio	S/N_A	f = 1kHz, 1Vrms input (0dB volume). (20Hz to 20kHz) BPF + A weighting filter (Fig. 4)	80	—	—	dB
Electronic Volume Control						
Volume attenuation step	A_{EVC}	f = 10Hz, 0.5Vp-p. Set by I^2C (Fig. 4)	1.6	2	2.4	dB
Audio limiter level	Alimit	f = 1kHz, 2.5Vrms input. Measure TV pk-pk output with limiter switched on. (Fig. 4)	—	2.2	—	Vrms
Mute TV I/P Mute or VCR I/P MUTE	Amute	f = 1kHz, 1Vrms input (Fig. 4)	—	–85	—	dB

Digital Characteristics

(1) I²C Interface

The I²C interface is compliant with Philips I²C Fast Mode specification (data April 1995). The interface is also capable of interfacing to +3.3V or +5V logic levels.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.3	—	5.5	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA, 3mA current supplied	0	—	0.4	V
		With SDA, 6mA current supplied	0	—	0.6	
Hysteresis of schmitt trigger input	V_{HYST}	$V_{IH} - V_{IL}$	—	0.5	—	V
Spike suppression	t_{SP}		—	—	50	ns
Fall time for SDA line	t_F	400pF bus load	—	—	300	ns
SCL clock frequency	t_{SCL}	I²C bus line requirement	0	—	400	kHz
Bus free time between a stop and start	t_{BUF}	I²C bus line requirement	1.3	—	—	µs
Hold time (repeated start condition)	$t_{HD;STA}$	I²C bus line requirement	0.6	—	—	µs
Low period of SCL clock	t_{LOW}	I²C bus line requirement	1.3	—	—	µs
High period of SCL clock	t_{HIGH}	I²C bus line requirement	0.6	—	—	µs
Setup time for a repeated start condition	$t_{SU;SDA}$	I²C bus line requirement	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	I²C bus line requirement	0	—	0.9	µs
Data setup time	$t_{SU;DAT}$	I²C bus line requirement	100	—	—	µs
Setup time for stop condition	$t_{SU;STO}$	I²C bus line requirement	0.6	—	—	µs



(2) Slow Blanking

Load = 10kΩ, supply +12V = +12V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input threshold low level	V_{TH1}		—	3	—	V
Input threshold high level	V_{TH2}		—	8.1	—	V
Output low level (Int TV mode)	V_{OUT1}	Load = 10kΩ	—	0.3	0.8	V
Output level (Ext 16:9 mode)	V_{OUT2}	Load = 10kΩ	4.8	5.5	6.5	V
Output level (Ext 4:3 mode)	V_{OUT3}	Load = 10kΩ	10	11	—	V

(3) Fast Blanking

Output load = 150Ω, supply +5V_VOUT = +5V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input threshold	V_{TH3}	Measured on fast blanking input 1, 2	—	0.7	—	V
Input current	I_{IN1}	+2V applied to input	—	2	—	µA
Output low level	V_{OUT4}	Load = 150Ω			0.2	V
Output high level	V_{OUT5}	Load = 150Ω	3	—	—	V

(4) logic and interrupt output

These outputs are open collector type and normally connected to +5V through a 10kΩ resistor.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output low voltage	DIG_{VOUTL}	I_{OL} = 1mA	—	—	0.4	V

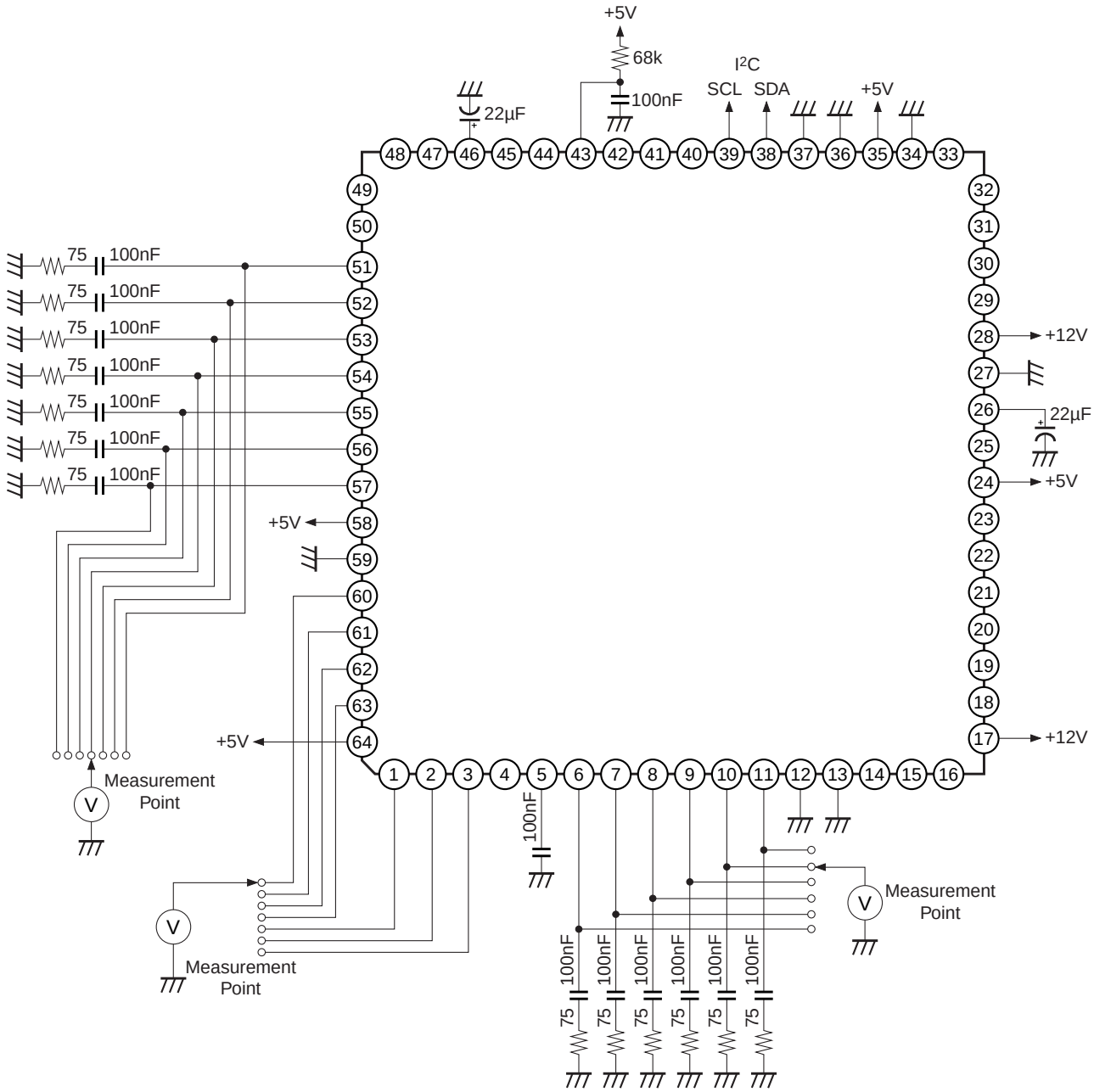


Fig. 1. Video System (DC Tests)

DC measured from Pins 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 51, 52, 53, 54, 55, 56, 57, 60, 61, 62, 63

Notes) 1. All supplies de-coupled close to the supply pins, 17, 24, 28, 58, 64 with 10nF and 10µF capacitors.
2. All video outputs are unloaded during tests.

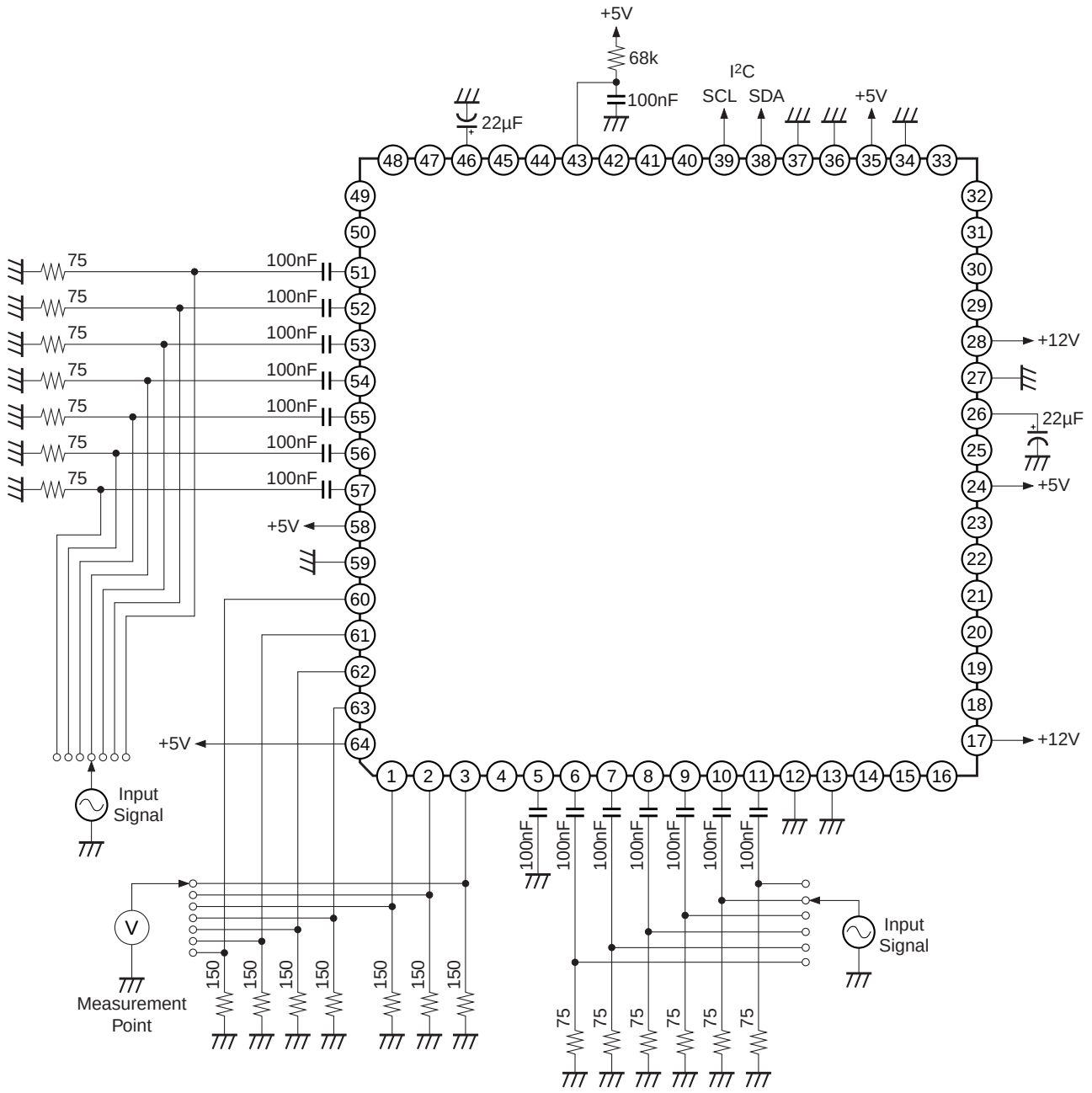


Fig. 2. Video System
(Gain, Dynamic Range, Bandwidth, Differential Gain, Differential Phase, Crosstalk, Linearity)

Signal applied to Pins 51, 52, 53, 54, 55, 56, 57, 6, 7, 8, 9, 10, 11
Output signal measured from Pins 60, 61, 62, 63, 64, 1, 2, 3

Notes) 1. All supplies de-coupled close to the supply pins, 17, 24, 28, 58, 64 with 10nF and 10µF capacitors.
2. For video crosstalk tests all video inputs are terminated with 37.5Ω.

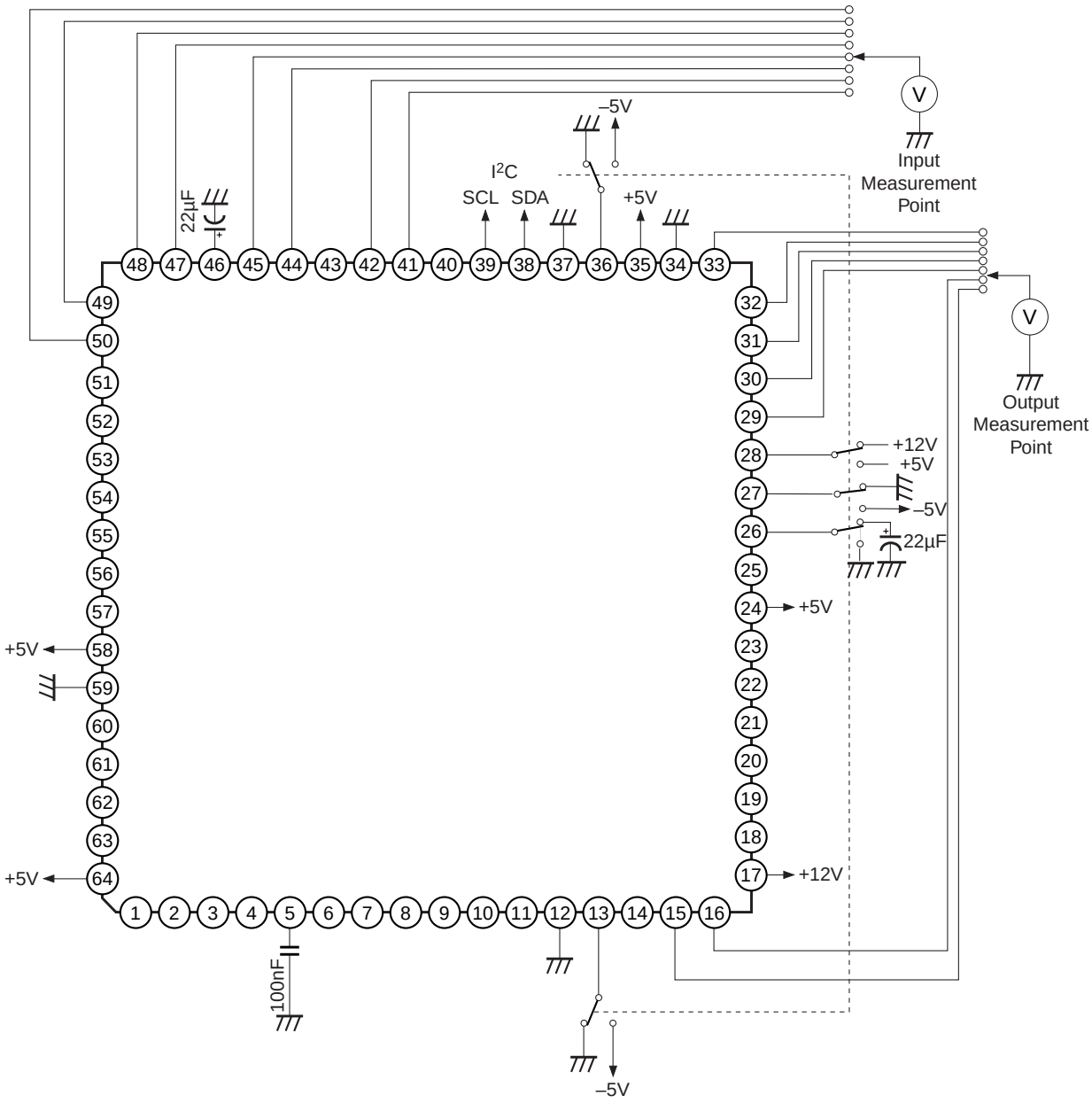


Fig. 3. Audio System (DC Tests)

DC measured from Pins 29, 30, 31, 32, 41, 42, 44, 45, 47, 48, 49, 50

Notes) 1. Single audio supply configuration shown. Operate switches for dual supply configuration.
2. All supplies de-coupled close to the supply pins, 17, 24, 28, 58, 64 with 10nF and 10µF capacitors.

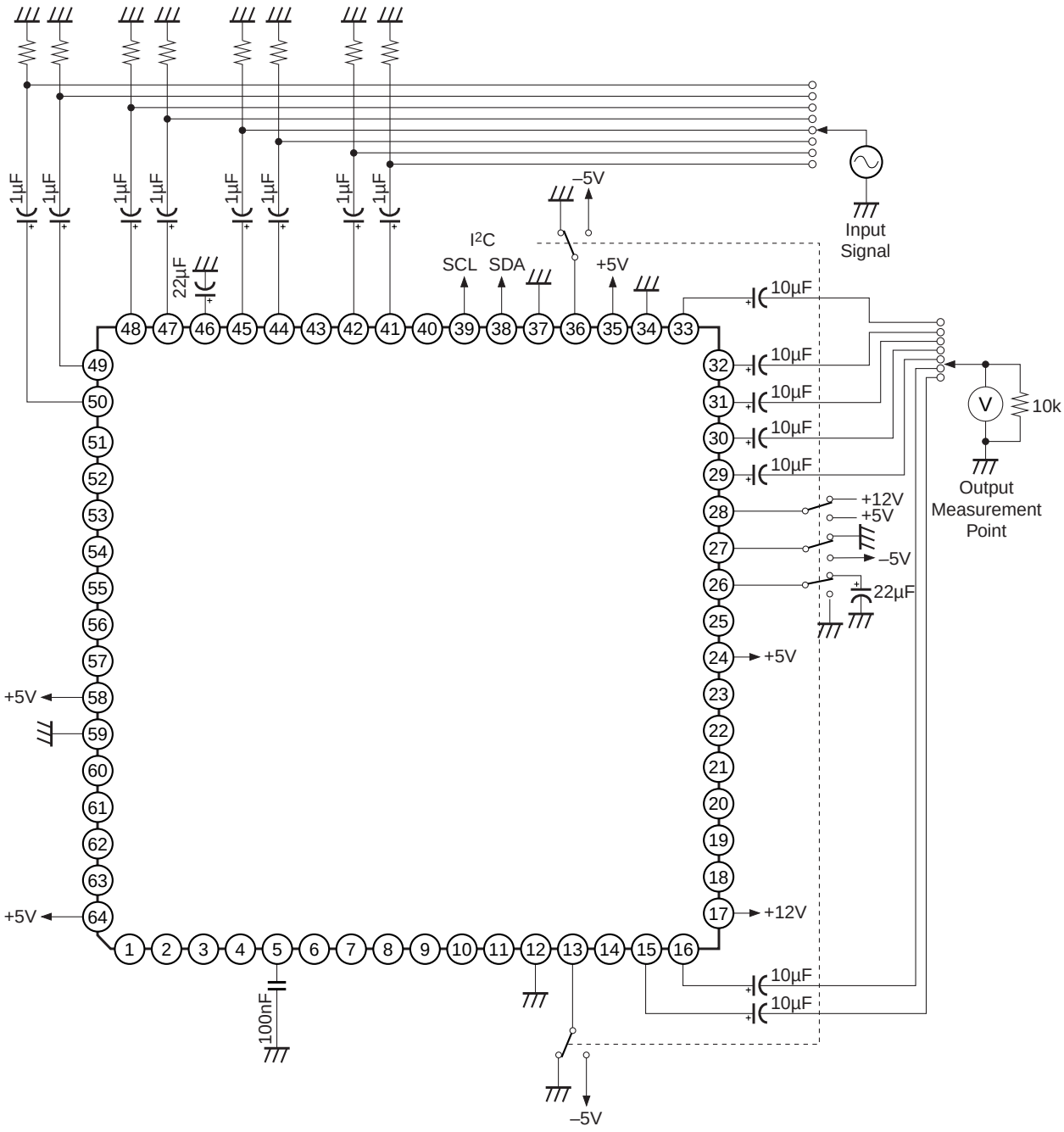


Fig. 4. Audio System

(Gain, Bandwidth, Signal to Noise, Electronic Volume, Zero Cross Detection, Dynamic Range, Crosstalk)

Signal applied to Pins 41, 42, 44, 45, 47, 48, 49, 50
Output signal measured from Pins 29, 30, 31, 32, 33

Notes) 1. Single audio supply configuration shown. Operate switches for dual supply configuration.
2. All supplies de-coupled close to the supply pins, 17, 24, 58, 64 with 10nF and 10µF capacitors.

I²C Control Data Format

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	DATAn	A	P

S: Start condition A: Acknowledge P: Stop condition

Address = 90H

I²C Data Structure (write mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	0	0 = Write
Data1	AUDIO LIMITER	VCR MONO SWITCH	VOLUME CONTROL					TV AUD MUTE
Data2	MONO SWITCH	TV MONO SWITCH	TV VOL BYPASS	VCR AUDIO SELECT		TV AUDIO SELECT		PHONO BYPASS
Data3	TV AUD MUTE	TV INPUT MUTE	ZCD	AUDIO DISABLE	LOGIC LEVEL	0	VCR INPUT MUTE	OVERLAY ENABLE
Data4	VIDEO INPUT GAIN		FNC VCR		FNC TV		FAST BLANK	
Data5	VCR VIDEO SWITCH			RGB GAIN		TV VIDEO SWITCH		
Data6	FILTER CONTROL	SYNC SEL		VIN5 CLAMP	VIN7 CLAMP	VIN3 CLAMP	MIXER CONTROL	
Data7	VOUT5_0 V	ENABLE VOUT7	ENABLE VOUT6	ENABLE VOUT5	ENABLE VOUT4	ENABLE VOUT3	ENABLE VOUT2	ENABLE VOUT1

I²C Data Structure (read mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	0	1 = Read
Data	NOT USED	NOT USED	ZERO CROSS STATUS	P.O.D.	NOT USED	SYNC DETECT	FNC_VCR	

Note) ZCD = Zero Cross Detect
P.O.D. = Power on Detect

I²C Video Control

TV Video Control [Data 5 Bits 0, 1, 2]

Switch setting	Vout1 Blue	Vout2 Green	Vout3 Red/Chroma	Vout4 CVBS/Y	Comment
0 xxxxx000	Encoder Blue VIN1	Encoder Green VIN3	Encoder Red VIN5	Encoder CVBS VIN8	Digital encoder RGB or CVBS
1 xxxxx001	Bias	Bias	Encoder Chroma VIN6	Encoder Luma VIN9	Digital encoder Y/C
2 xxxxx010	VCR Blue VIN2	VCR Green VIN4	VCR Chroma/Red VIN7	VCR CVBS/Y VIN10	VCR Y/C or RGB
3 xxxxx011	Bias	Bias	Bias	TV CVBS VIN11	TV
4 xxxxx100	Bias	Bias	Encoder Chroma VIN5	Encoder Luma VIN3	Digital encoder Y/C
5 xxxxx101	Encoder blue VIN1	Encoder Green VIN3	Encoder Red VIN5	Aux CVBS VIN12	Encoder RGB and AUX CVBS
6 xxxxx110	Bias	Bias	Aux Chroma VIN13	Aux CVBS/Y VIN12	Aux Y/C or CVBS
7 xxxxx111	Bias	Bias	Bias	Bias	Video Mute

After power on all TV outputs are off (high impedance) and muted.

TV RGB Gain Control [Data 5 Bits 3, 4]

I²C setting "RGB GAIN"	Extra gain/dB
0 xxx00xxx	0
1 xxx01xxx	+1
2 xxx10xxx	+2
3 xxx11xxx	+3

The power on default is 0dB.

VCR Video Control [Data 5 Bits 5, 6, 7]

Switch setting	Vout5 Chroma	Vout6 CVBS/Y	Comment
0 000xxxxx	Encoder Chroma VIN5	Encoder CVBS/Y VIN8	Digital encoder Y/C
1 001xxxxx	Encoder Chroma VIN6	Encoder Luma VIN9	Digital encoder Y/C
2 010xxxxx	VCR Chroma VIN7	VCR CVBS/Y VIN10	VCR Y/C
3 011xxxxx	Bias	TV CVBS VIN11	TV CVBS
4 100xxxxx	Encoder Chroma VIN5	Encoder Luma VIN3	Encoder Y/C
5 101xxxxx	Bias	Aux CVBS VIN12	AUX CVBS
6 110xxxxx	Aux Chroma VIN13	Aux CVBS VIN12	AUX Y/C
7 111xxxxx	Bias	Bias	Video mute

After power on VCR outputs are off (high impedance) and muted.

"Y/C MIXER CONTROL" [Data 6 Bits 0, 1]

I^2C setting	Vout7 Mixer output
0 xxxxxx00	No mix, Vout7 = Vout4 (CVBS)
1 xxxxxx01	Mix Vout4 (Y) + Vout3 (C)
2 xxxxxx10	No mix, Vout7 = Vin8 (CVBS)
3 xxxxxx11	No mix Vout7 = Vout4 (CVBS)

The power on default is no mix.

Input Clamp Control "VIN3 Clamp" [Data 6 Bit 2]

xxxxx0xx = GREEN input on VIN3. DC restore clamp active. (Power on default)

xxxxx1xx = CVBS input on VIN3. Sync tip clamp active.

Input Clamp Control "VIN7 Clamp" [Data 6 Bit 3]

xxxx0xxx = CHROMA input on VIN7. Chroma bias applied. (Power on default)

xxxx1xxx = RED input on VIN7. DC restore clamp applied.

Input Clamp Control "VIN5 Clamp" [Data 6 Bit 4]

xxx0xxxx = RED input on VIN5. DC restore clamp applied. (Power on default)

xxx1xxxx = CHROMA input on VIN5. Chroma bias applied.

Sync Select Control for RGB DC Restore Circuits "SYNC_SEL" [Data 6 Bits 5, 6]

When the TV output is set to RGB + Y/CVBS mode. Then it is necessary to select the input that contains the sync information for the RGB signal. This will normally be the digital encoder CVBS or VCR CVBS input.

I²C setting "SYNC_SEL"	Input with sync
0 x00xxxxx	VIN8
1 x01xxxxx	VIN9
2 x10xxxxx	VIN10
3 x11xxxxx	VIN12

The power on default is Vin8 ie. Digital encoder input.

Video Input Gain [Data 4 Bits 6, 7]

Extra gain applied to Vin1, 3, 5, 6, 8, 9

I²C setting "VIDEO INPUT GAIN"	Extra gain/dB
0 00xxxxxx	0 (Bypass)
1 01xxxxxx	+1
2 10xxxxxx	+3
3 11xxxxxx	+6

The power on default is bypass.

Filter Control [Data 6 Bit 7]

The filters on the six digital encoder inputs Vin1, 3, 5, 6, 8, 9 are switched on with this control bit.

0xxxxxxx = Filter bypass. Power on default.

1xxxxxxx = Filter on.

Standby Mode Control [Data 7 Bits 0, 1, 2, 3, 4, 5, 6]

The video outputs VOUT1, 2, 3, 4, 5, 6, 7 can be individually turned off using data byte 7.

0 = Video output off. (Power on default)

1 = Video output on.

Note) When switched off, the video outputs are in a high impedance state. With a normal 150Ω load, the outputs will be pulled to 0V.

Bi-directional Line Control on VCR Scart "Vout5_0V" [Data 7 Bit 7]

0xxxxxxx = Vout5 active. Connected to input specified in VCR switch table.

1xxxxxxx = Vout5 set to 0V.

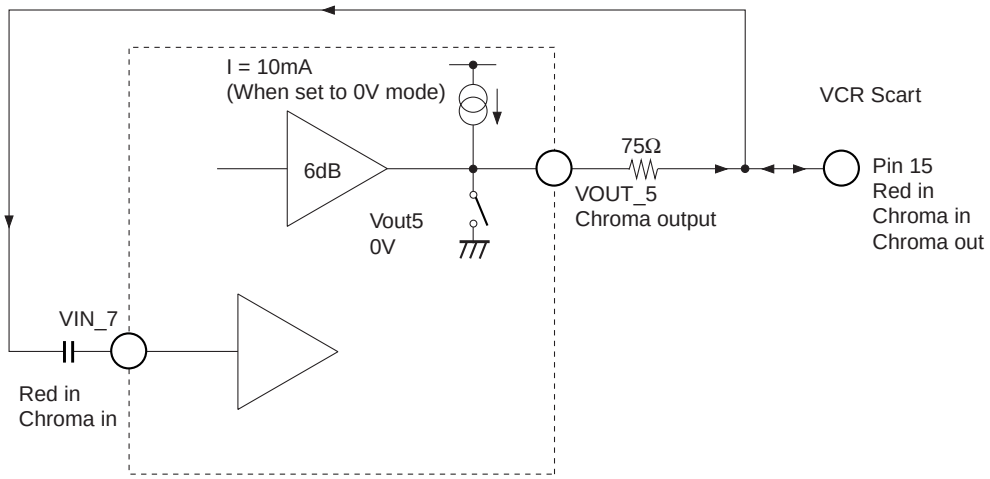


Fig 5. Bi-directional Line to VCR

As Pin 15 on the VCR scart can be bi-directional, either chroma output or red/chroma input, it is necessary for output Vout5 to be individually controlled. When the red or chroma signal comes from the VCR, then output Vout5 is set to 0V giving the required line termination impedance of 75Ω.

I²C Audio Signal Control

TV and Phono Audio Control [Data 2 Bits 1, 2]

Switch setting		RTV, Phono_R	LTV, Phono_L
0	xxxxx00x	Rin1	Lin1
1	xxxxx01x	Rin2	Lin2
2	xxxxx10x	Rin3	Lin3
3	xxxxx11x	Rin4	Lin4

After power on Rin1/Lin1 are selected.

VCR Audio Control [Data 2 Bits 3, 4]

Switch setting		Rout1	Lout1
0	xxx00xxx	Rin1	Lin1
1	xxx01xxx	RTV signal	LTV signal
2	xxx10xxx	Rin3	Lin3
3	xxx11xxx	Rin4	Lin4

After power on Rin1/Lin1 are selected.

TV Mono Switch [Data 2 Bit 6]

Switch setting		Connection to R channel output	Connection to L channel output	Comment
0	x0xxxxxx	R	L	Normal
1	x1xxxxxx	(R + L mix)	(R + L mix)	Mono mix

VCR Mono Switch [Data 1 Bit 6]

Switch setting		Connection to R channel output	Connection to L channel output	Comment
0	x0xxxxxx	R	L	Normal
1	x1xxxxxx	(R + L mix)	(R + L mix)	Mono mix

"AUDIO DISABLE" [Data 3 Bit 4]

xxx0xxxx = Normal outputs

xxx1xxxx = All outputs disabled. When the outputs are disabled, they are in a high impedance state. For a single supply configuration, the output voltage will drop to 0V.

"PHONO BYPASS" [Data 2 Bit 0]

xxxxxxx0 = Phono outputs connected after volume control block. (Default)

xxxxxxx1 = Phono outputs connected before volume control block.

"TV VOL BYPASS" [Data 2 Bit 5]

xx0xxxxx = TV outputs connected after volume control block. (Default)

xx1xxxxx = TV outputs connected before volume control block.

"MONO SWITCH" [Data 2 Bit 7]

0xxxxxxx = Mono output connected to mix of TV R + L channels. (Default)

1xxxxxxx = Mono output connected to mix of RIN1 + LIN1 inputs.

"VOLUME CONTROL" [Data 1 Bits 1, 2, 3, 4, 5]

Setting		Volume gain
0	xx00000x	+6dB
1	xx00001x	+4dB
2	xx00010x	+2dB
3	xx00011x	0dB (power on default)
4	xx00100x	–2dB
5	xx00101x	–4dB
6	xx00110x	–6dB
7	xx00111x	–8dB
8	xx01000x	–10dB
9	xx01001x	–12dB
10	xx01010x	–14dB
11	xx01011x	–16dB
:		:
31	xx11111x	–56dB

"OVERLAY ENABLE" [Data 3 Bit 0]

xxxxxxx0 = Overlay off (Power on default)

xxxxxxx1 = Overlay on: Rin3 and Lin3 are mixed and added to Rin1, Lin1 channels.

TV Mute and Zero Cross Operation

When the zero cross is switched on (ZCD = 1), volume control changes are only implemented when the audio signal passes though the zero cross point. Similarly, when a mute instruction is sent, the TV outputs are only muted when the signal passes the zero cross point. This eliminates any click noise.

There are two TV audio mute control bits in the bus map. By having two bits it allows the TV outputs to be muted, the TV channel changed and then un-muted all in one I^2C write operation. The normal structure for a click free audio channel change is as follows:

Data 1: Mute the TV audio output with the ZCD switched on.

Data 2: Change the TV audio source.

Data 3: Un-mute the TV audio output again with the ZCD switched on.

Operation of the Mute circuit

TV Audio Mute [Data 1 Bit 0], [Data 3 Bit 7]	ZCD [Data 3 Bit 5]	Operation TV, Phono, Mono output
0	0	Un-mute immediately
0	1	Un-mute on next zero cross
1	0	Mute immediately
1	1	Mute on next zero cross

After power on TV Audio Mute = 1 and ZCD are set to 1.

"TV INPUT MUTE" [Data 3 Bit 6]

x0xxxxxx = The input to the TV switch is not muted.

x1xxxxxx = The input to the TV switch is muted. (Power on default)

"VCR INPUT MUTE" [Data 3 Bit 1]

xxxxxx0x = The input to the VCR switch is not muted.

xxxxxx1x = The input to the VCR switch is muted. (Power on default)

"AUDIO LIMITER" [Data 1 Bit 7]

When active, the output of the volume control block is limited to 2.2Vrms maximum.

0xxxxxxx = The volume control outputs are not limited. (Power on default)

1xxxxxxx = The volume control outputs are limited to 2.2Vrms.

Fast Blanking Operation (Pin 16 on SCART), FBLK

The fast blanking signal instructs the TV to select either the external CVBS information or the external RGB information. This is used to superimpose an on screen display (OSD) presentation (normally RGB) upon a CVBS background. Fast blanking information has the same nominal phase as the RGB and CVBS signal, and is defined as follows,

Fast blanking output at scart,

1. CVBS mode: Scart pin voltage = 0 to 0.4V
2. RGB mode: Scart pin voltage = 1 to 3.0V

The threshold voltage is approximately 0.75V at the scart input.

Fast Blanking I^2C Control

In the CXA7002R has two fast blanking inputs, one associated with the digital encoder input (FBLK_IN1) and another associated with the VCR RGB/CVBS input (FBLK_IN2). These can be selected and switched to the output using an I^2C instruction. In addition, the fast blank output pin can be set to a constant 0V or +3.5V by means of the I^2C control. Hence there are four possible states. These are set according to the following table.

"FAST_BLANK" [Data 4 Bits 0, 1]

I^2C setting "BLANK_LEVEL"	Fast blank output pin voltage
0 xxxxxx00	0V (Power on default)
1 xxxxxx01	Same status as Fast Blank in 1 (0/+3.5V)
2 xxxxxx10	Same status as Fast Blank in 2 (0/+3.5V)
3 xxxxxx11	+3.5V

Fast Blank Output Interface

The Fast Blanking output pin is connected to the scart via a 75Ω resistor. Optional ESD protection circuitry can be added.

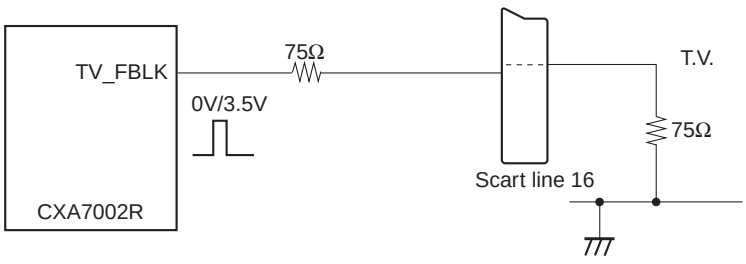


Fig. 6. Fast Blanking Output Interface

Function Switching Operation (Pin 8 on scart)

Both, VCR and TV function lines can be set to outputs and controlled independently. The TV function line has two modes, the first being control via I²C and secondly the follow mode where the output will follow the same state as the VCR input.
When the VCR function lines is set as input, the level can be read back from the status resistor. An interrupt is generated when the level changes.

"FNC TV_LEVEL" [Data 4 Bits 2, 3]
These bits set the voltage at the output TV_FNC function line (Pin 8).

I²C control "FNC_TV"	Voltage at output	Mode
0 xxxx00xx	Follows VCR input	Follows VCR input
1 xxxx01xx	< 1V	Internal TV
2 xxxx10xx	> 4.5V, < 7V	External scart input 16:9 mode
3 xxxx11xx	> 9.5V	External scart input 4:3 mode

Note) After power on the output is internal TV mode ie. 0V at the pin.

"FNC VCR_LEVEL" [Data 4 Bits 4, 5]
These bits set the voltage at the output VCR_FNC function line (Pin 8).

I²C control FNC_VCR	Voltage at output	Mode
0 xx00xxxx	NA	Input
1 xx01xxxx	< 1V	Internal
2 xx10xxxx	> 4.5V, < 7V	External scart input 16:9 mode
3 xx11xxxx	> 9.5V	External scart input 4:3 mode

Note) The power on default is "Input" mode.

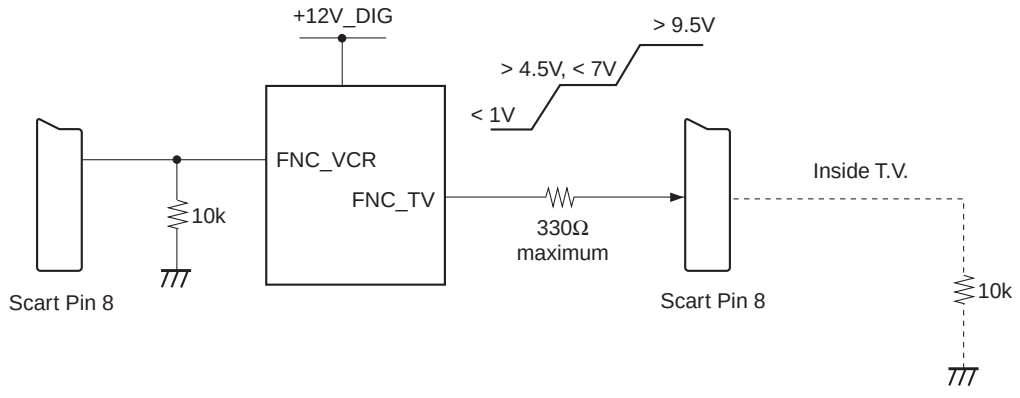


Fig. 7. TV Function Switch Output

Logic and Interrupt Output Pins

These two pins are open collector type and require an external pull-up resistor.

Interrupt Output

The interrupt pin will become a current sink for approximately 1µs when the VCR input function line changes from:

a) 0 to 6V, 6 to 0V b) 0 to 12V, 12 to 0V c) 6 to 12V, 12 to 6V

OR

When the sync detector detects that a valid video signal has been added or removed.

This pin will normally be connected to +5V through a 10kΩ resistor.

Multiple interrupt signal may be generated for signals on the threshold of having a valid sync.

Logic Output

The logic output level can be changed using the logic output bit in the I^2C register, "LOGIC_LEVEL".

"LOGIC LEVEL" [Data 3 Bit 3]

xxxxx0xx = Current sink mode resulting in < 0.4V saturation voltage on logic pin. (default)

xxxxx1xx = Open collector/high output impedance on logic pin.

Imax during current sink = 1mA

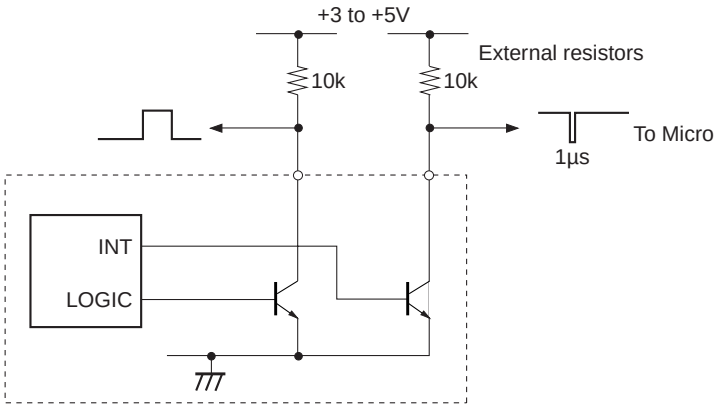


Fig. 8. INT and Logic Line Interface

Read Mode Status Register

The following information can be read from the status register:

FNC VCR [Bits 0, 1]

The status register bits 0, 1 hold the level of the input function line.

Input pin voltage	SCART mode	Read	Data 8
FNC_VCR		b1	b0
0 to +2V (default)	(Internal)	0	0
+4.5 to +7V	(16:9 External)	1	0
+9.5 to +12V	(4:3 External)	1	1

"SYNC DETECT" [Bit 2]

Once a valid sync signal is detected on the input selected by "SYNC_SELECT" this bit is set to 1. The bit is reset to 0 every time the SYNC_SELECT is changed. It is assumed that when a video input is in-active then the input level will be 0V with minimum noise.

"POD" (Power on Detect) [Bit 4]

This bit is set to 1 after power on. It is then changed to 0 after the first I^2C read. It is used to detect if the supply has been corrupted. If the POR bit is read as 1 at any time then the IC should be re-initialized to the correct I^2C settings.

"ZERO CROSS STATUS" [Bit 5]

This audio function is used to determine if an input audio signal has passed the zero cross point.

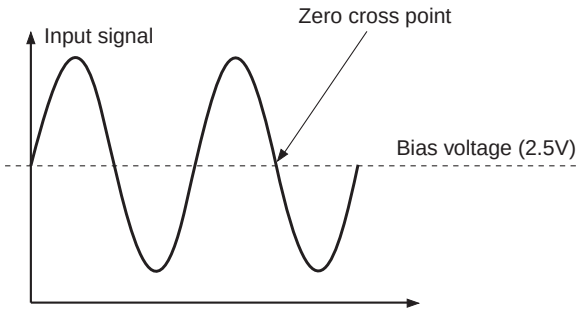


Fig. 9. Zero Cross Point

0 = No zero cross detected.
1 = Signal has passed through zero cross point.

Description of Operation

Video Section

Inputs and Outputs

The video section comprises of thirteen (13) high impedance inputs switched through to seven (7) video outputs. An internal +6dB amplifier is connected to each output. The amplifier is required to compensate for the 6dB attenuation that occurs at the 75Ω series output resistor. Outputs VOUT_1 to VOUT_7 are capable of driving 150Ω loads. Output VOUT_7 is designed to interface to an RF Modulator.

Composite/Luminance Inputs

The 4 composite (or luma) inputs are ac coupled to the input pins. The signals are first sync tip clamped to a set level. These clamps are permanently active, therefore these inputs should only be used for signals with a sync.

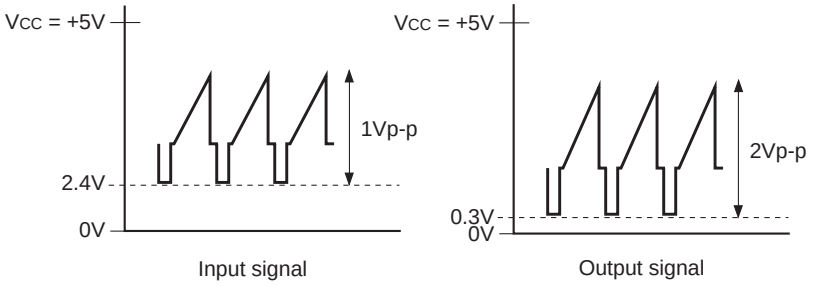


Fig. 10. CVBS/Y Waveforms

RGB Inputs

The RGB inputs are ac coupled to the input pins. The inputs have a dc restore circuit, which is used to set the blanking level to a fixed voltage. The clamps are controlled by the timing signal provided by the sync detect circuit. It is necessary to select the correct luma or CVBS signal associated with the RGB inputs for the sync select circuit. It is assumed that a sync signal will not be present on any of the RGB input signals. For inputs that can be either red or chroma then the clamp can be switched between the dc restore mode (for red input) and average level bias (for chroma). The RGB signals are fed through additional gain amplifiers which are controlled by I^2C. These allow the nominal 0.7Vp-p signal to be increased to 0.8Vp-p, 0.9Vp-p or 1Vp-p. When the TV output is in Y/C mode, the RGB gain should be set to 0dB to prevent over amplification of the chroma output.

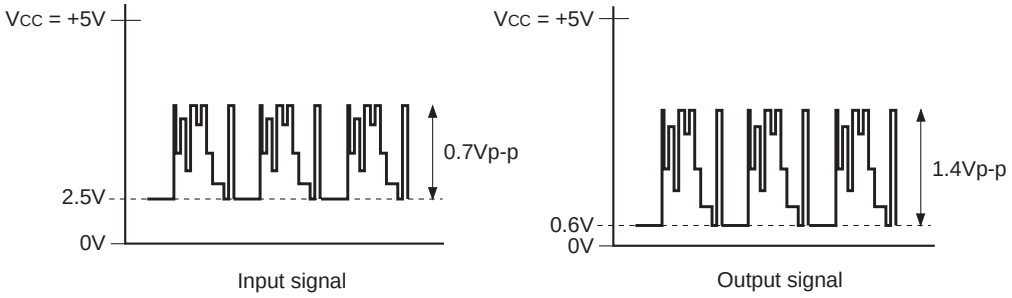


Fig. 11. RGB Waveforms

Sync Detection Circuit

The clamp signals, used to restore the RGB level, are generated from the sync detect circuit. By using the "SYNC_DETECT" control bits, the 4 different CVBS/Y inputs may be selected. Once selected, the signal is compared with a threshold voltage 65mV above the tip level. If the signal is less than this threshold it is not passed to the next block. If greater than the threshold, it is passed to the discrimination circuit which checks that the duty cycle is greater than 91%. The discrimination block also contains a time constant which, when a sync is detected, holds the status line high for at least 7 video lines. If a valid sync signal is detected the "SYNC_DETECT" bit in the read register is set to 1.

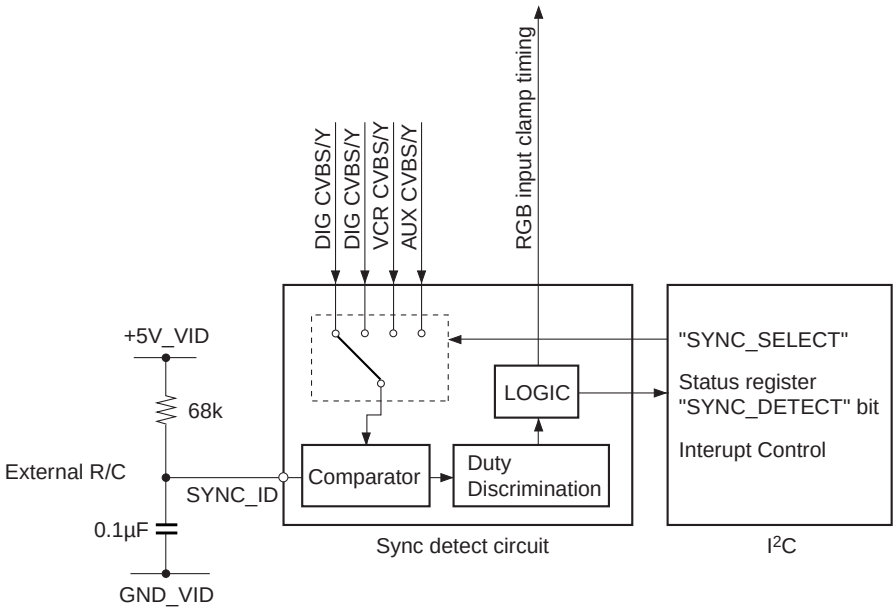


Fig. 12. Sync Detection Circuit

Chroma Inputs

The chroma signals are ac coupled to the input pins. The inputs have a fixed dc bias that sets the average level to approximately 3.1V for VIN_5 & VIN_7 and 2.45V for VIN_6 & VIN_13. For inputs that can also be RED signals the input circuit can be switched to the dc restore mode.

Typical waveforms:

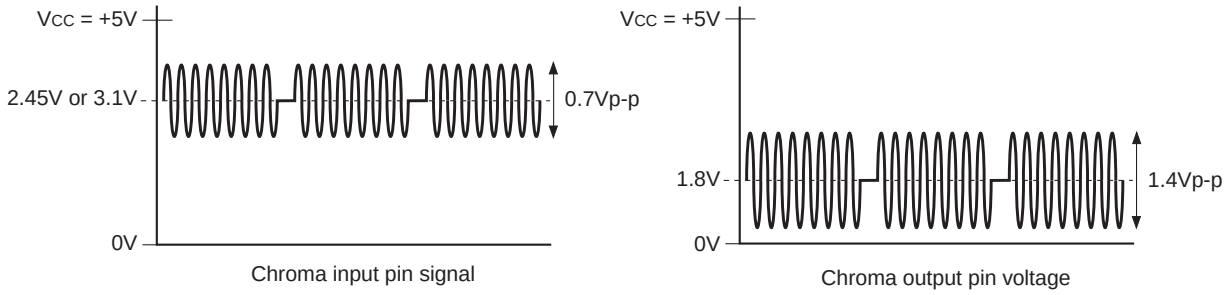


Fig. 13. Chroma Waveforms

Video Input Gain Stage

The six inputs from the digital encoder, VIN_1, 3, 5, 6, 8, 9 may need further amplification. An adjustable gain stage is provided with settings of +1, 3, 6dB extra gain. For normal inputs (1Vp-p for CVBS, 0.7Vp-p for RGB), the gain section may be bypassed.

Video Input filters

To reduce any digital noise, the six inputs from the digital encode pass through a low pass filter. The filter has a high attenuation at the clock frequency of 27MHz.

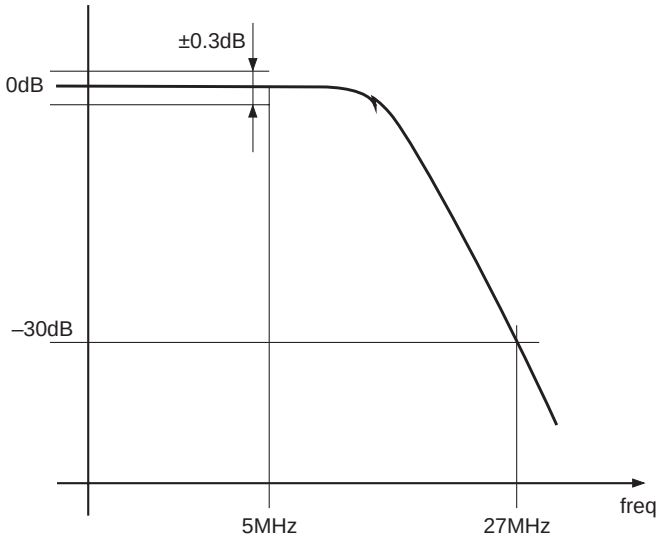


Fig. 14. Basic Filter Response

Y/C Mixer

A Y/C mixer can be used for mixing Luma and Chroma signals for use with an external RF modulator connected to VOUT_7. The Y/C mixer is controlled via the I^2C data bus. The signal may be a mix of the TV Y/C signals or simply the TV CVBS signal. It is also possible to select the CVBS signal from the digital encoder. The circuit is shown in Fig. 15 with a trap circuit used to give 6dB attenuation at 4.43MHz of the Luma signal.

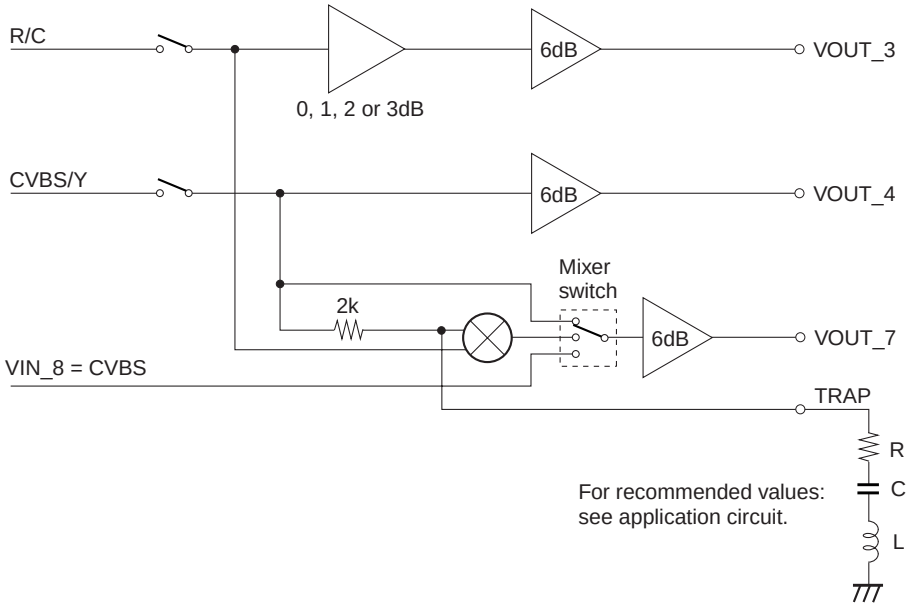


Fig. 15. Internal Y/C Mixer Circuit

Switching the Video Outputs Off

Each video output can be individually turned off using the I^2C. When turned off, the output is set to a high impedance state and hence the current consumption and power dissipation is reduced. After power on, all the video outputs are set to the high impedance state.

Typical Video Interface Circuits

Single or Dual Supply

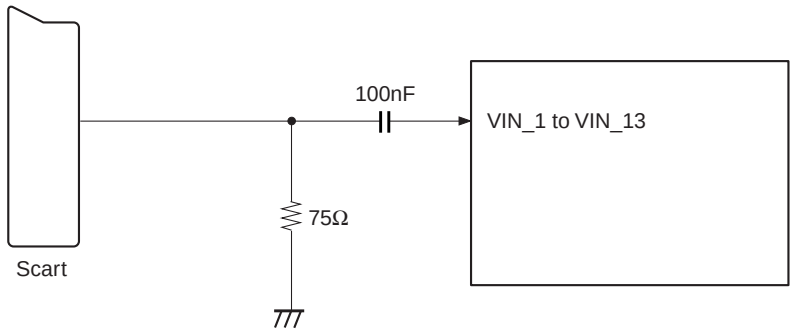


Fig. 16. Video Input Interface

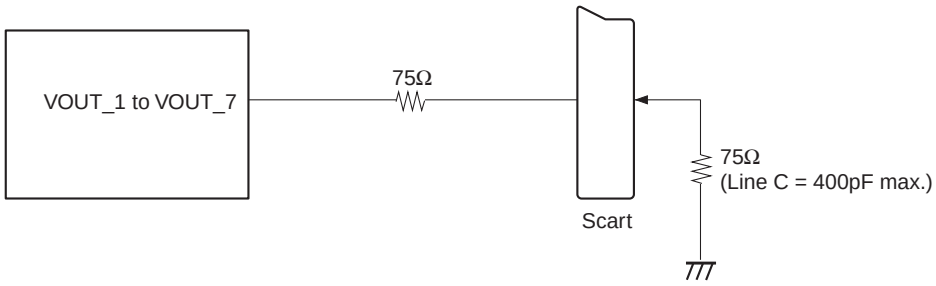


Fig. 17. Video Output Interface

Audio Section

Inputs and Outputs

The audio system consists of 4 stereo inputs, 2 stereo outputs and separate mono and Phono outputs. The stereo outputs can be connected to any one of the 4 stereo inputs. All audio inputs have a –12dB attenuator except RIN_1 and LIN_1. Therefore, as an amplifier having +12dB of gain follows the interval switch, the net gain of the audio system from input to output is 0dB. The stereo input RIN_1/LIN_1 has fixed gain from input to output of +6dB. This input is typically connected to an audio DAC with full scale of 1Vrms or less.

The output impedance of each audio amplifier is near zero. The output may be directly coupled to the scart for the dual supply case but must be ac coupled through a capacitor (typically 10µF) for the single supply case. The outputs are capable of driving 600Ω loads. The user may add additional low pass filters to the outputs.

TV Output Switching

The TV audio section is composed of an audio switch followed by a volume control stage. The volume is adjustable from +6dB to –56dB in 2dB steps. The volume control block includes a switchable limiter function to prevent the output signals exceeding 2.2Vrms. When activated, the output signals from the volume control block will be clamped to 2.2Vrms. A mono switch that allows the mixed R + L signal to be switched to the R and L output channels follows the volume control section.

TV Mute

This I^2C mute function acts on the TV, Phono and Mono audio circuits. Audio mute will be implemented after an audio zero cross detection to reduce click noise if "ZCD" = 1.

Zero Cross Detector (ZCD)

The zero cross detector reduces the effect of "click noise" when implementing a volume change or an audio mute. The volume change or mute instruction sent by I^2C will only be implemented when a minimal (ie zero cross) signal amplitude is detected.
It can be seen from the I^2C write format that the same mute bit occurs in DATA1 and DATA3. This allows the software to action a mute, then after a delay (1/Audio_freq (min)) make any suitable changes to the audio source and then un-mute the output buffer. Such a period provides ample time to allow any audio signals to pass the zero cross point before the signal source is changed.

VCR Output Switching

The outputs ROUT1, LOUT1 have a fixed gain of 0dB from the input except when position 2 is selected. Position 2 selects the RTV and LTV signals. These signals are affected by the TV volume control.

Phono outputs

There is a stereo Phono output that carries the same signal as the TV output. This is typically used for connection to a hi-fi. The signal level of the Phono outputs is normally the same as the TV outputs however it is possible to bypass the volume section and set the Phono outputs to a fixed level. If any attenuation is required then this can be done externally.

Mono Output

The mono output for the RF modulator has two settings. The first is a mix of the TV R + L channels. In this case, the output signal will have the same volume control as the RTV/LTV outputs. The second setting is a mix of the audio DAC inputs (RIN_1 + LIN_1). In this setting the output will always have fixed volume and if the tone overlay is used, this will appear on the output.

Audio Overlay

The inputs RIN_3, LIN_3 may be used for a normal stereo audio input or alternatively to overlay an external audio source onto the TV outputs. This may be a tone or voice. The R and L inputs are mixed and then added equally to the RIN_1 and LIN_1 inputs. The I^2C control bit "AUDIO OVERLAY ENABLE" is used to switch on this facility.

Audio Disable

All the audio outputs may be disabled using the "Audio Output Disable" function (Data Byte 3 Bit 4). This disable mode is different from the normal mute as it puts the outputs into a high impedance state. The disable mode is different from the normal mute as it can be used for power reduction in standby modes.

Hardware Mute

The hardware mute input pin is used to instantaneously mute all the audio outputs. It has the same operation as the audio disable function. The outputs are muted when the pin goes below +2V.

Typical Audio Interface Circuits

Supply type 1: Dual supply

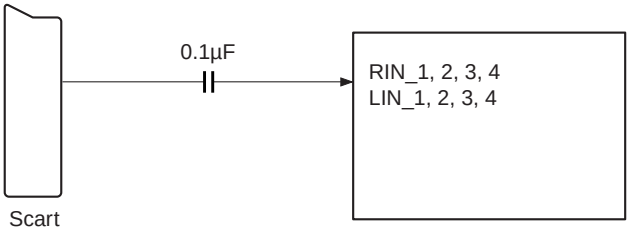


Fig. 18. Audio Input Interface

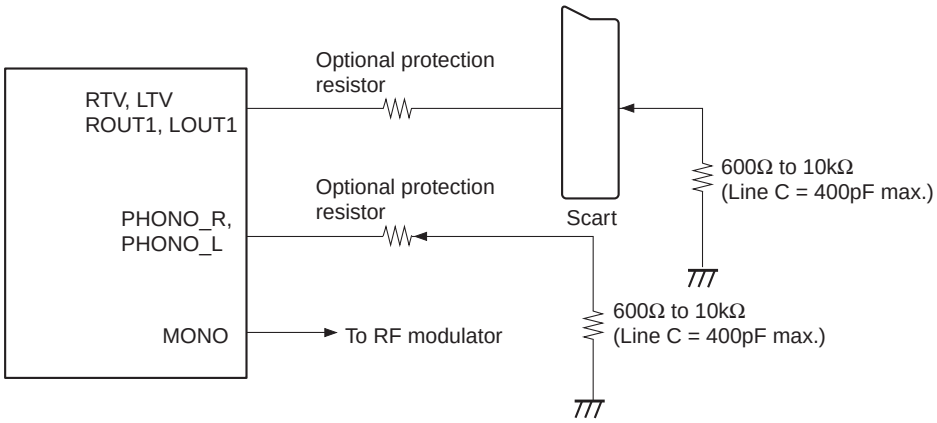


Fig. 19. Audio Output Interface

Supply type 2: Single supply

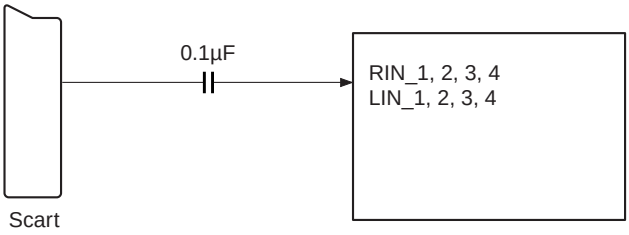
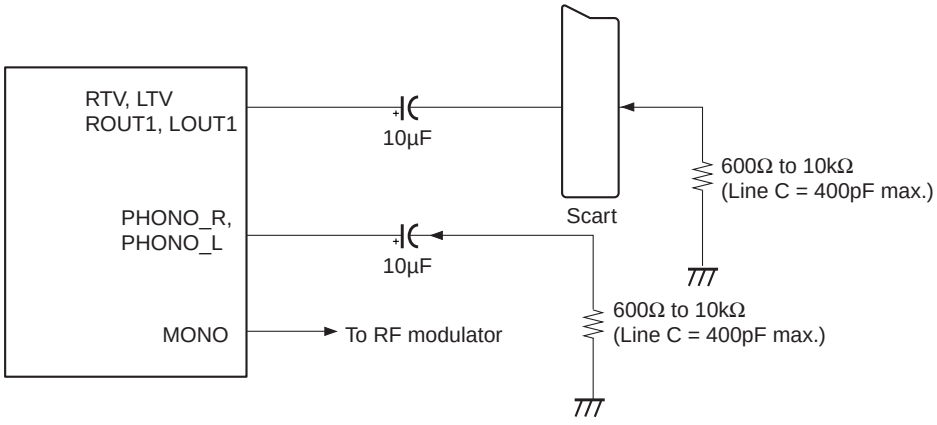


Fig. 20. Audio Input Interface



* For loads = 600Ω, larger capacitors may be needed

Fig. 21. Audio Output Interface

Application in Set Top Box

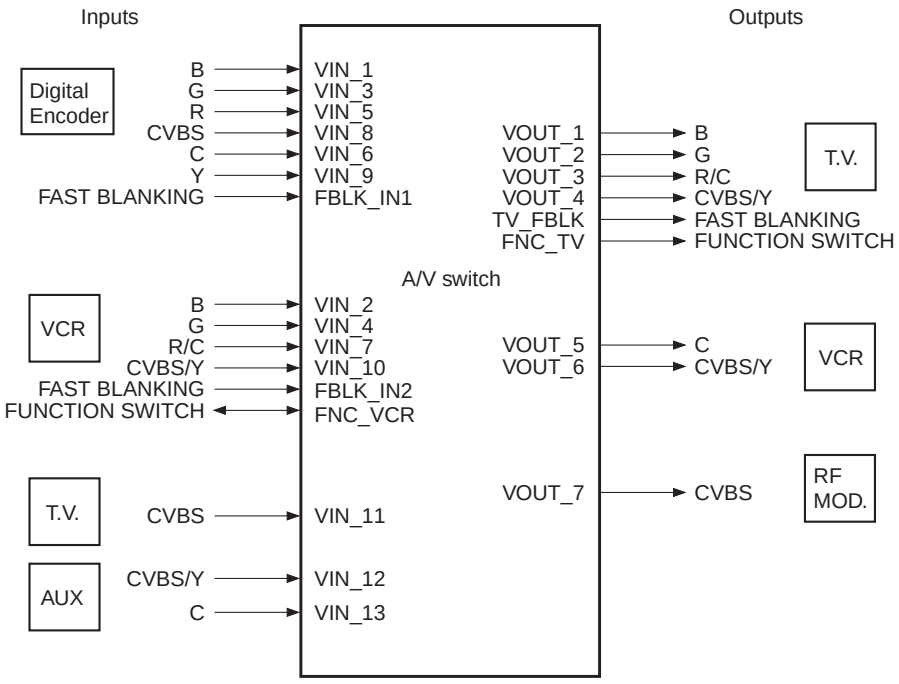


Fig. 22. Video Application with 6 Output Digital Encoder

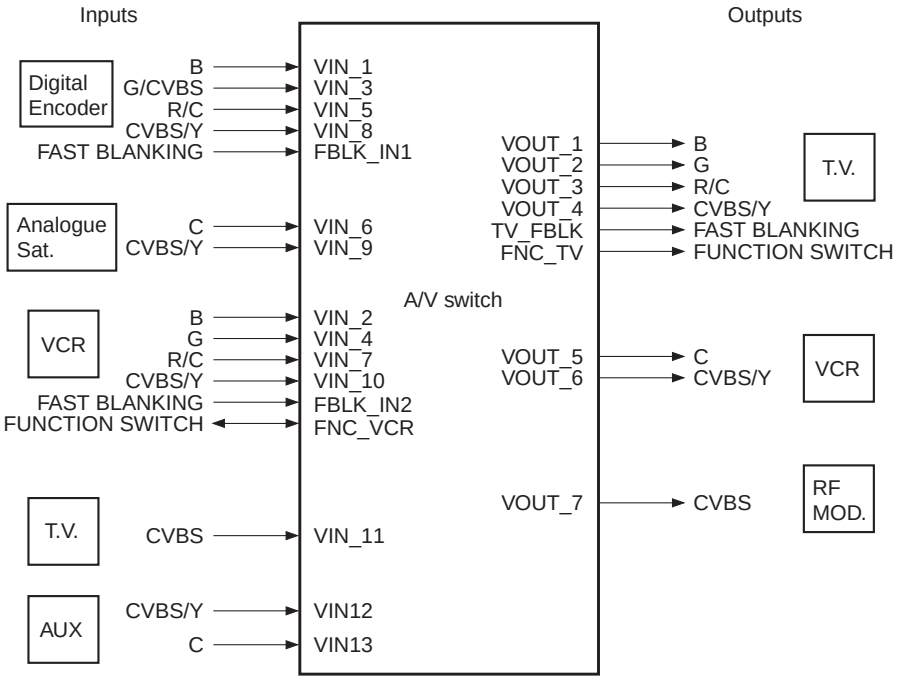


Fig. 23. Video Application with 4 Output Digital Encoder

Audio Application

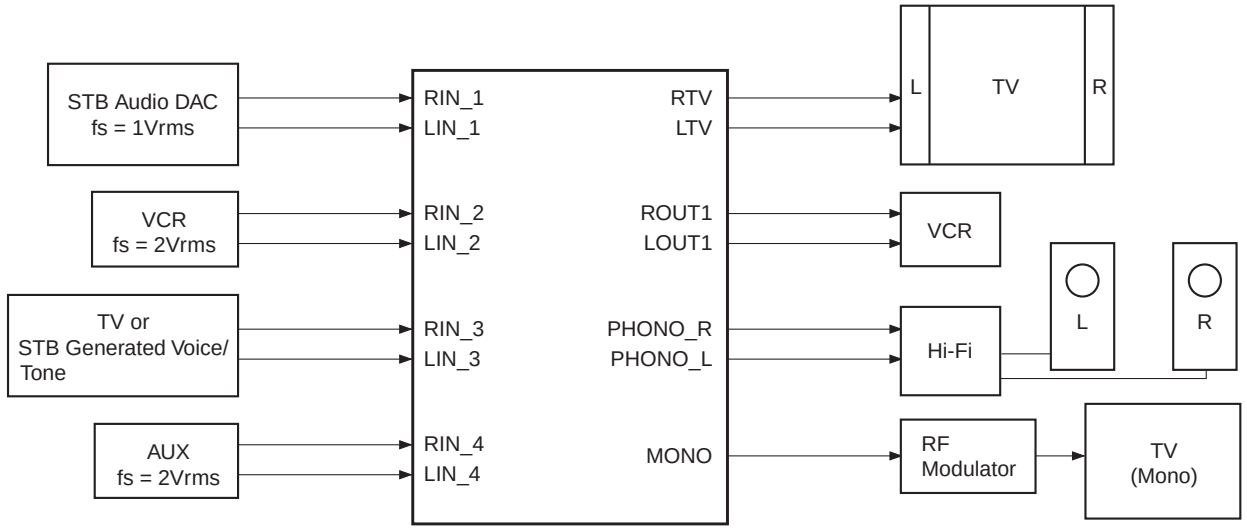


Fig. 24. Audio Application

Supply Connections

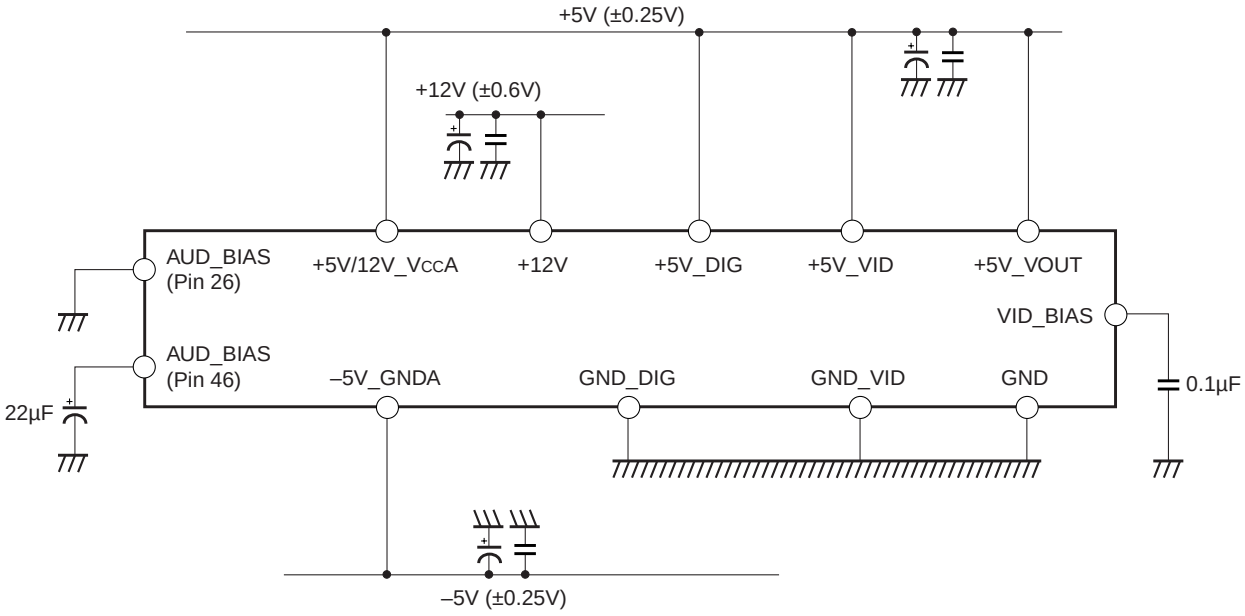


Fig. 25. Dual Supply

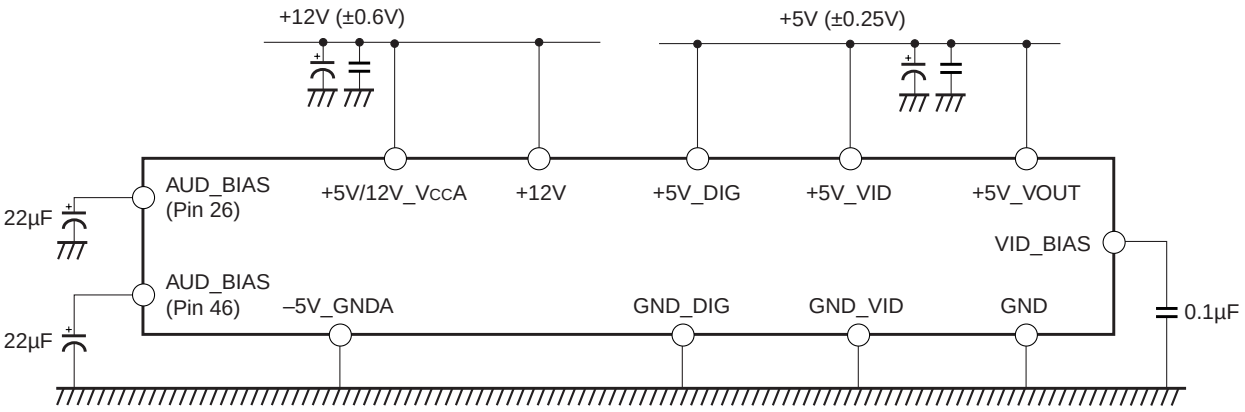
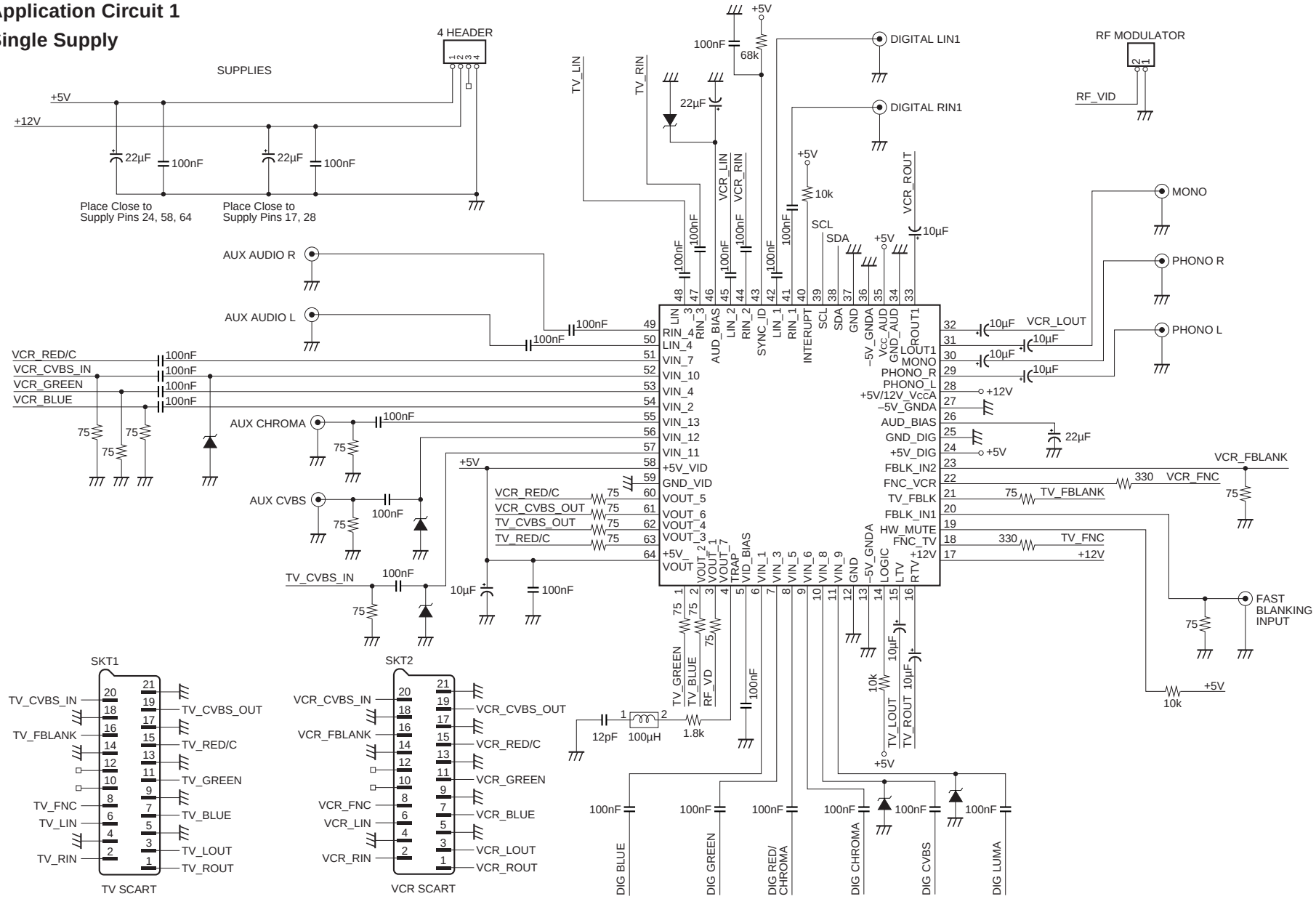


Fig. 26. Single Ended Supply

Application Circuit 1

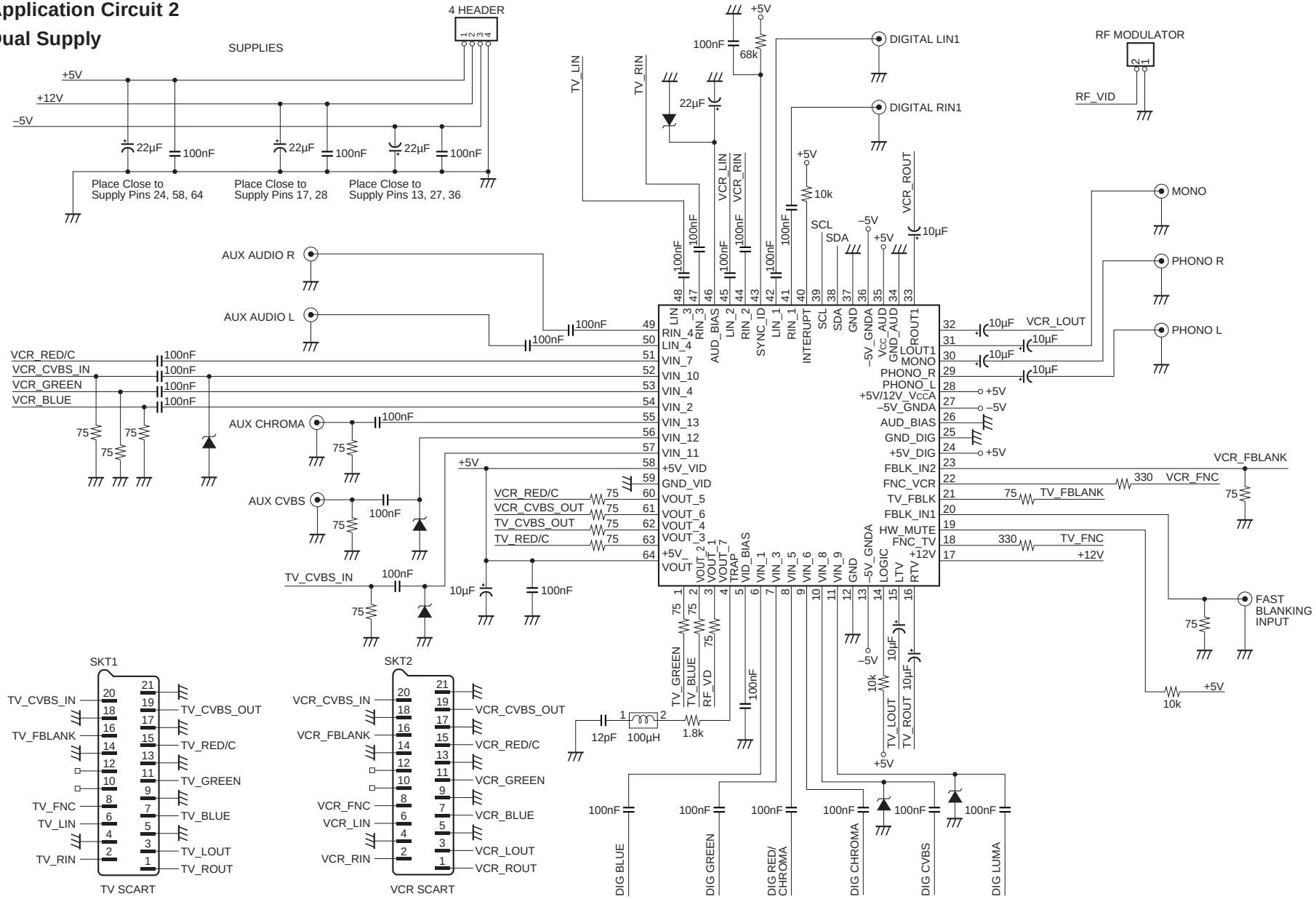
Single Supply



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2

Dual Supply



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1) Supply de-coupling capacitors, 10nF and 10µF in parallel should be inserted as close as possible to the supply Pins 17, 24, 28, 35, 58 and 64. When using the dual supply configuration apply the capacitors to Pins 13, 27, 36 in addition to the listed supply pins.

2) To minimize crosstalk, attention should be given to the routing of audio and video to the IC inputs. PCB track lengths should be kept as short as possible and preferably, audio placed on a separate layer to the video.

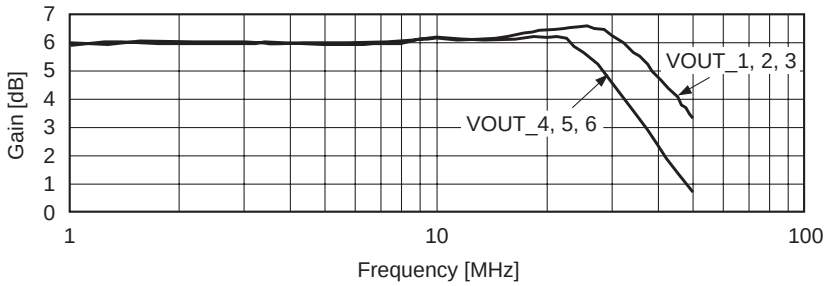
3) Attention should be given to the electrolytic capacitors on the output pins. In single supply configuration the audio pin dc bias voltage will be approximately 6.0V, therefore the positive terminal of the capacitors should be orientated towards the device pin.

4) To minimize stray capacitance the 75Ω series resistor on video outputs VOUT_1 to VOUT_7 should be mounted as close as possible to the device Pins 1, 2, 3, 60, 61, 62 and 63.

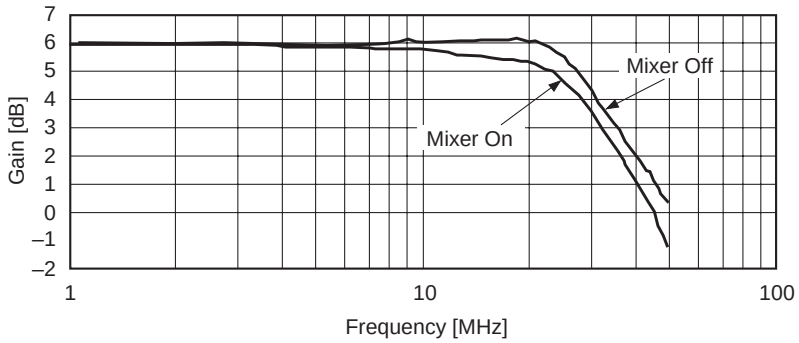
5) Pins 10, 11, 46, 52, 56, 57 have reduced ESD performance and external protection circuitry may be added. As shown in the application schematic, zener diodes may be added. Zener diodes with a rating > 5V may be used.

Typical Performance Curves

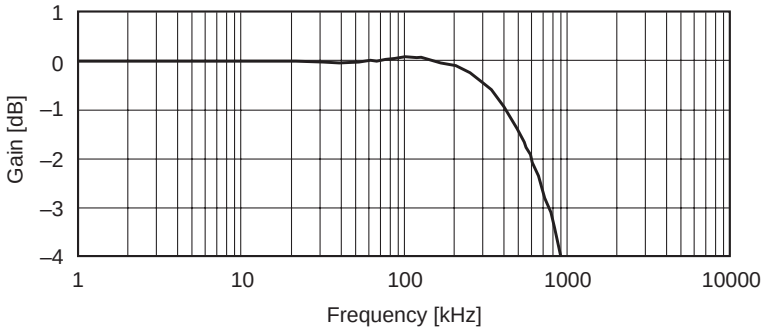
Video gain – VOUT_1, 2, 3, 4, 5, 6



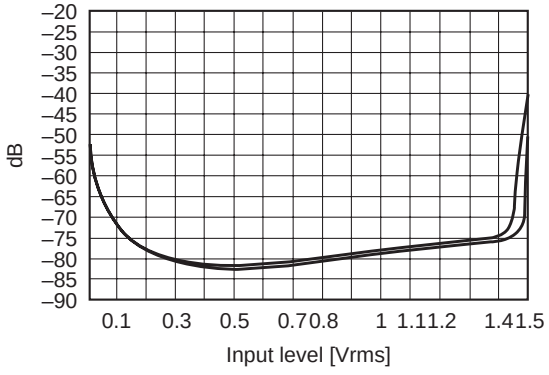
Video gain – VOUT_7



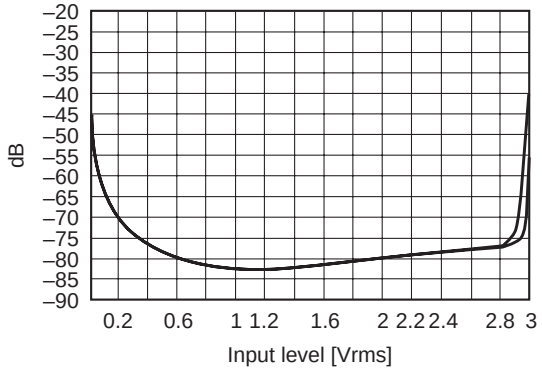
Audio gain



Audio THD + N
RIN_1/LIN_1 to TV outputs

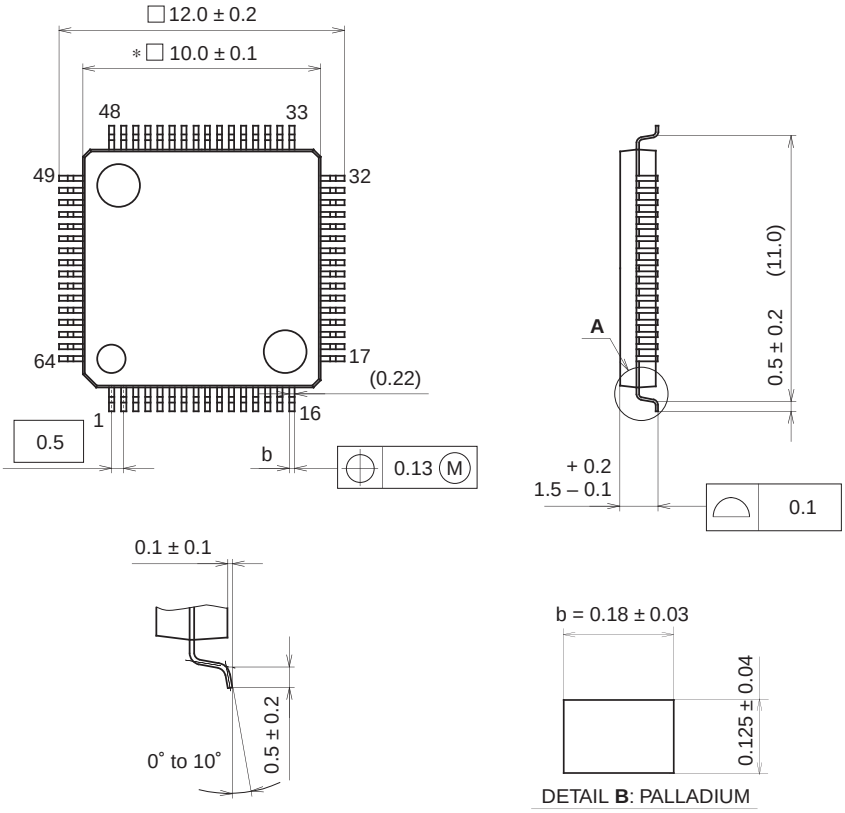


Audio THD + N
RIN_2, 3, 4/LIN2, 3, 4 to TV outputs



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	P-LQFP64-10x10-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g