SONY

CXA2697ER

5-Channel 2-LD Driver for Optical Disc Drive

Preliminary

Description

The CXA2697ER is a laser driver IC corresponded to DVD ×12 and capable of driving two high output lasers (CD/DVD) for writable optical discs.

Features

- CD write channel maximum drive current: 300mA
  (V_{CC} = 3V, V_{CC_LD} = 4.5V, VOP = 2.5V)
- CD total maximum drive current: 370mA
  (V_{CC} = 3.3V, V_{CC_LD} = 5V, VOP = 2.5V)
- DVD write channel maximum drive current: 270mA
  (V_{CC} = 3V, V_{CC_LD} = 4.5V, VOP = 3V)
- DVD total maximum drive current: 360mA
  (V_{CC} = 3.3V, V_{CC_LD} = 5V, VOP = 3V)
- Capable of generating five-value recording waveform through control of five channels
- Rise/Fall times = 1ns
- Read Channel: ×125
- Write Channel: ×470
- Read Channel has extensive low-noise design
  1.5nA/$\sqrt{Hz}$ (@20MHz, I_{LD} = 35mA, Imod = 20mAp-p)
- High frequency modulator circuit
- Frequency variable range: 200 to 600MHz
- Modulator amplitude can be set separately for CD and DVD.
- DVD modulator amplitude switching function
- Timing input for generating recording waveform can be adapted to both differential input (LVDS) and single-end input (3.3V CMOS/TTL).

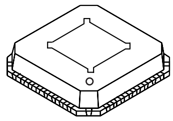
Applications

CD-R, CD-RW, DVD-R, DVD-RW, DVD+R/RW, DVD-ROM and DVD-RAM for high-speed writable optical disc drives

Structure

Bi-CMOS IC

32 pin VQFN (Plastic)



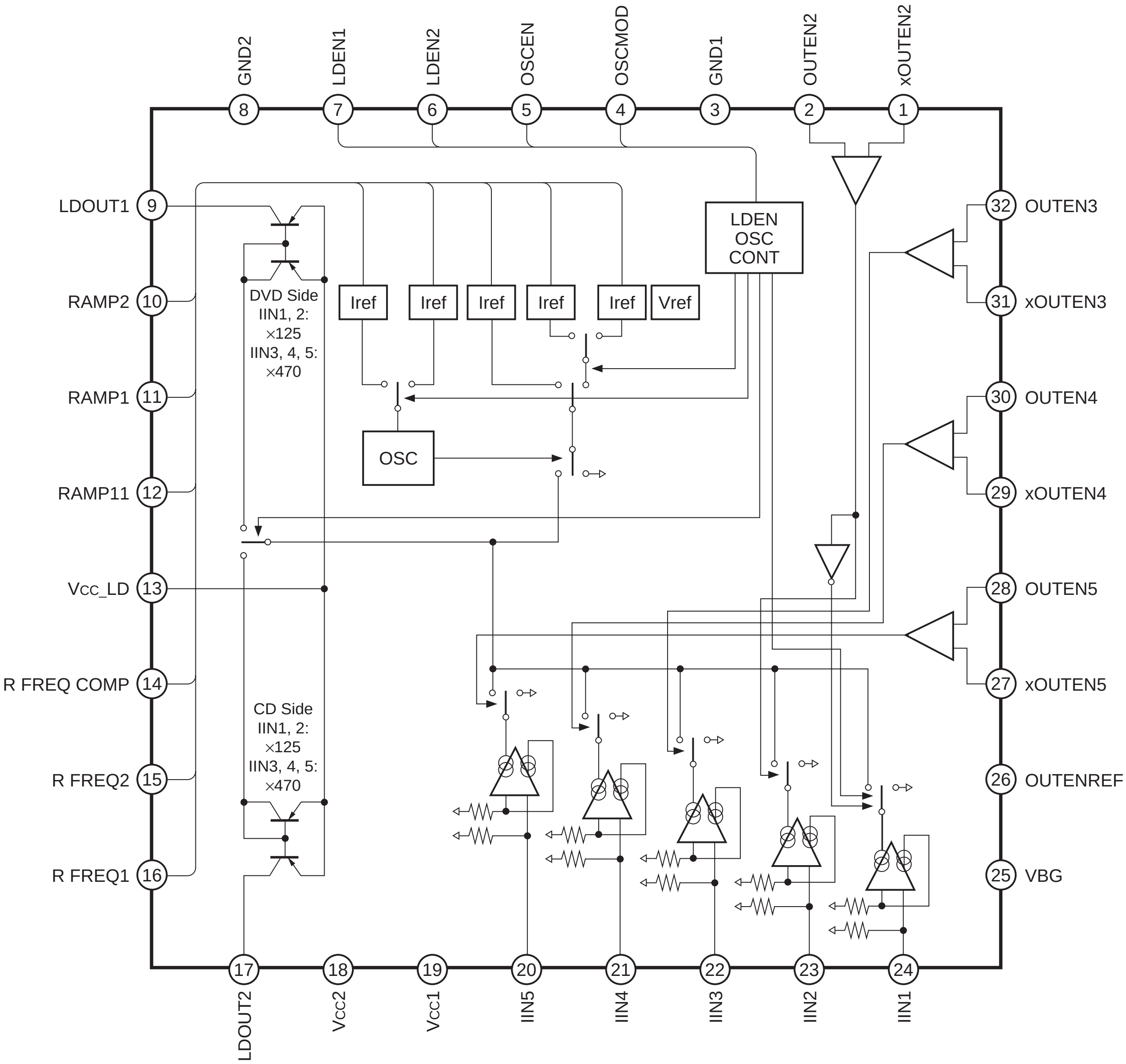
Absolute Maximum Ratings

• Supply voltage	V_{CC}	3.6	V
	V_{CC_LD}	5.5	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D	TBD	mW

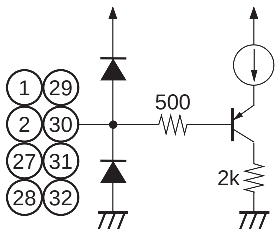
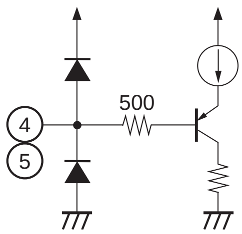
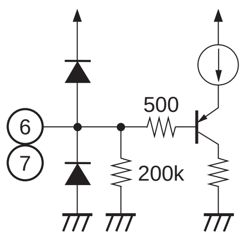
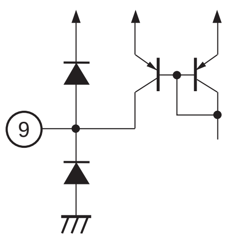
Operating Conditions

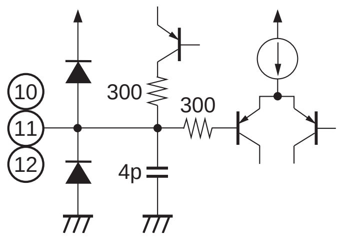
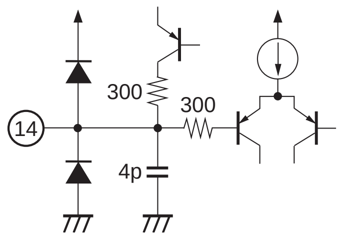
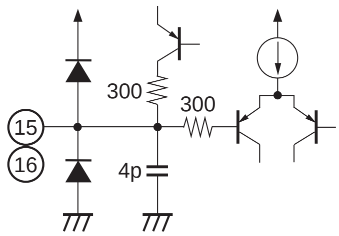
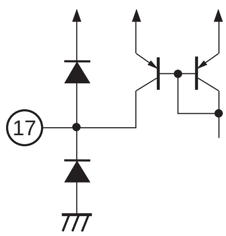
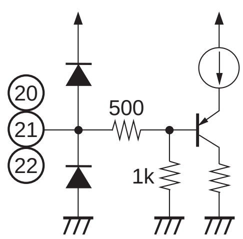
• Supply voltage	V_{CC}	3 to 3.6	V
	V_{CC_LD}	4.5 to 5.5	V
• Operating temperature	Topr	–10 to +75	°C

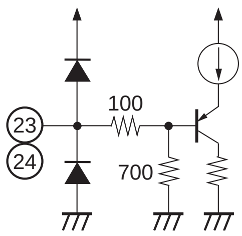
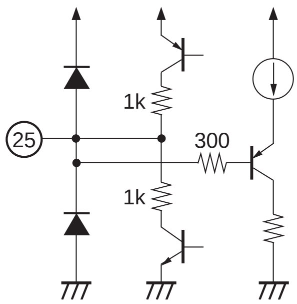
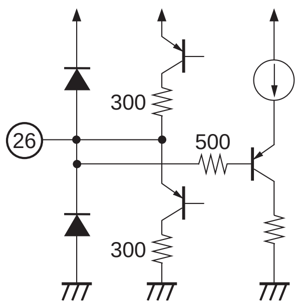
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
1	xOUTEN2	I	—		IIN1 or IIN2 set current control signal input.
2	OUTEN2	I	—		IIN1 or IIN2 set current control signal input.
27	xOUTEN5	I	—		IIN5 set current control signal input. (negative logic)
28	OUTEN5	I	—		IIN5 set current control signal input. (positive logic)
29	xOUTEN4	I	—		IIN4 set current control signal input. (negative logic)
30	OUTEN4	I	—		IIN4 set current control signal input. (positive logic)
31	xOUTEN3	I	—		IIN3 set current control signal input. (negative logic)
32	OUTEN3	I	—		IIN3 set current control signal input. (positive logic)
3	GND1	—	—	—	Ground.
4	OSCMOD	I	—		DVD modulator amplitude switching control signal. When OSCMOD = high, RAMP1 is selected. When OSCMOD = low, RAMP11 is selected.
5	OSCEN	I	—		Modulator control signal. (positive logic) When OSCEN = high, the modulator waveform is output.
6	LDEN2	I	—		CD output control. (positive logic)
7	LDEN1	I	—		DVD output control. (positive logic)
8	GND2	—	—	—	Ground.
9	LDOUT1	O	—		DVD laser drive current output. Enabled when LDEN 1 = high and LDEN2 = low.

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
10	RAMP2	O	—		Modulator amplitude setting 2. Enabled when LDEN1 = low and LDEN2 = high. Connects resistance to ground.
11	RAMP1	O	—		Modulator amplitude setting 1. Enabled when LDEN1 = high, LDEN2 = low and OSCMOD = high. Connects resistance to ground.
12	RAMP11	O	—		Modulator amplitude setting 11. Enabled when LDEN1 = high, LDEN2 = low and OSCMOD = low. Connects resistance to ground.
13	Vcc_LD	—	—	—	Output stage supply voltage.
14	R FREQ COMP	O	—		Modulator frequency variation adjustment. Connects resistance to ground.
15	R FREQ2	O	—		Modulator frequency setting 2. Enabled when LDEN1 = low and LDEN2 = high. Connects resistance to ground.
16	R FREQ1	O	—		Modulator frequency setting 1. Enabled when LDEN1 = high and LDEN2 = low. Connects resistance to ground.
17	LDOUT2	O	—		CD laser drive current output. Enabled when LDEN1 = low and LDEN2 = high.
18	Vcc2	I	—	—	Supply voltage for timing system and current switch.
19	Vcc1	I	—	—	Supply voltage for control system and modulator system.
20	IIN5	I	—		Current setting 5.
21	IIN4	I	—		Current setting 4.
22	IIN3	I	—		Current setting 3.

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
23	IIN2	I	—		Current setting 2.
24	IIN1	I	—		Current setting 1.
25	VBG	O	1.26V		Internal reference voltage decoupling.
26	OUTENREF	O	$1/2V_{CC}$		Reference voltage output for current control signal. Connects decoupling capacitance to ground.

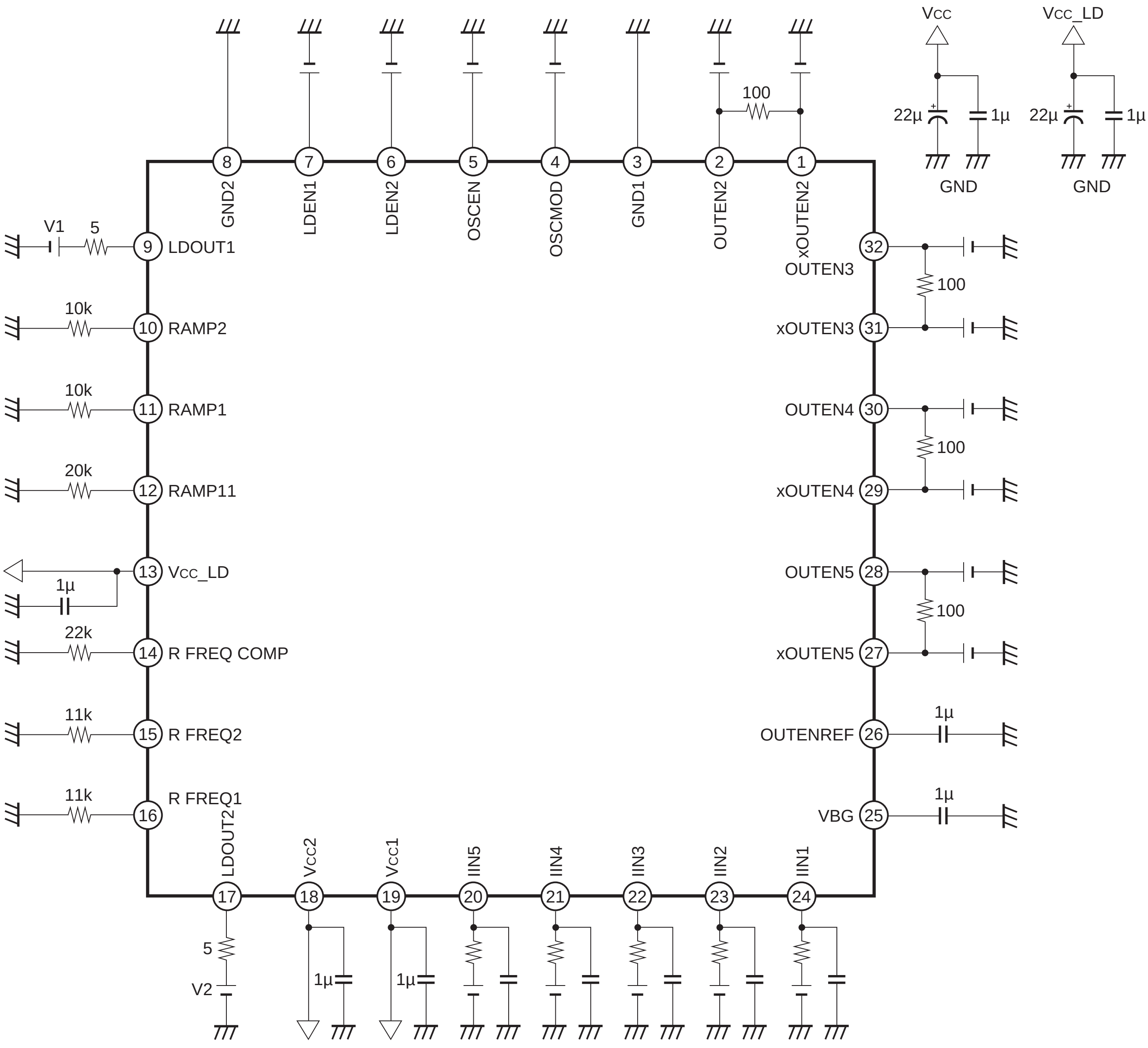
Electrical Characteristics (V_{CC} = 3.3V, V_{CC}_LD = 5V, Ta = 25°C)

Test No.	Measurement item	Symbol	Min.	Typ.	Max.	Unit	Conditions
1	Current consumption 1	Icc1	1.4	2	2.6	mA	LDEN1, 2 = L
2	Current consumption 1'	Icc1'	23	34	45	mA	(LDEN1 = H, LDEN2 = L) or (LDEN1 = L, LDEN2 = H)
3	Current consumption 2	Icc2	75	110	145	mA	LDEN1 = H, IOUT1 = 60mA, OSCEN = H, AMP = 20mAp-p
4	Current consumption 3	Icc3	162	236	310	mA	LDEN = H, IOUT1 = 60mA, IOUT3 = 240mA (Duty = 25%), IOUT4 = 120mA (Duty = 50%), IOUT = IOUT1 + IOUT3 + IOUT4
5	Current consumption 3-1	Icc3_1	140	200	260	mA	LDEN = H, IOUT1 = 30mA, IOUT3 = 240mA (Duty = 25%), IOUT4 = 120mA (Duty = 50%), IOUT = IOUT1 + IOUT3 + IOUT4
<Logic input block: During single-end transfer>							
6	Input voltage high level	VSH	2	—	V_{CC}	V	
7	Input voltage low level	VSL	GND	—	1.3	V	
<Logic input block: During differential input>							
8	LVDS Input voltage high level	VDH	0.2	—	2.6	V	
9	LVDS Input voltage low level	VDL	0	—	1.6	V	
10	LVDS Input voltage amplitude	VPP	0.2	—	1	V	
<LD driver block: DC>							
11	LD drive current 1, 2	IOUTR	120	—	—	mA	
12	LD drive current 3, 4, 5 (DVD)	IOUTW1	270	—	—	mA	
13	LD drive current 3, 4, 5 (CD)	IOUTW2	300	—	—	mA	
14	Total LD drive current 1 (DVD)	IOUT1	360	—	—	mA	V_{CC} = 3.3V, V_{CC}_LD = 5V, VOP = 3V
15	Total LD drive current 2 (CD)	IOUT2	370	—	—	mA	V_{CC} = 3.3V, V_{CC}_LD = 5V, VOP = 2.5V
16	Minimum LD drive current 1 (DVD)	OFFSET1	—	—	5	mA	IIN = 0µA, LDEN1 = OUTEN2 = OUTEN3 = OUTEN4 = OUTEN5 = H
17	Minimum LD drive current 2 (CD)	OFFSET2	—	—	5	mA	IIN = 0µA, LDEN2 = OUTEN2 = OUTEN3 = OUTEN4 = OUTEN5 = H
18	Output current noise 1	NOISE1	—	1.5	—	nA/$\sqrt{Hz}$	f = 400MHz, I_{LD} = 35mA, Imod = 20mAp-p (20MHz: NOISE)
19	Output current noise 2	NOISE2	—	1.5	—	nA/$\sqrt{Hz}$	f = 400MHz, I_{LD} = 35mA, Imod = 40mAp-p (20MHz: NOISE)

Test No.	Measurement item	Symbol	Min.	Typ.	Max.	Unit	Conditions
<LD driver block: Pulse driving>							
20	Propagation delay	DELAY	—	3	—	ns	
21	Rise time (Tr)	TR	—	1	—	ns	I_{LD} = 50 to 100mA pulse Settling 10 to 90% (resistance load)
22	Fall time (Tf)	TF	—	1	—	ns	I_{LD} = 100 to 50mA pulse Settling 10 to 90% (resistance load)
<ILD control block>							
23	Input resistance 1 (Pins 23, 24)	ZIINR	0.56	0.8	1.04	kΩ	
24	Input resistance 2 (Pins 20, 21, 22)	ZIINW	1.05	1.5	1.95	kΩ	
25	Input/output gain 1, 2	GAINR	110	125	140	—	
26	Input/output gain 3, 4, 5 (DVD)	GAINW1	400	470	510	—	
27	Input/output gain 3, 4, 5 (CD)	GAINW2	400	470	510	—	
28	ILD control linearity 1 (DVD)	LINEA1	–3	—	3	%	Based on linearity when I_{LD} = 50 to 150mA (I_{READ} = 30mA) V_{CC}_LD = 4.5V, V_{CC} = 3V, V1 = 1.65V, RL = 5Ω, I_{LD} = 270mA
29	ILD control linearity 2 (CD)	LINEA2	–3	—	3	%	Based on linearity when I_{LD} = 50 to 150mA (I_{READ} = 30mA) V_{CC}_LD = 4.5V, V_{CC} = 3V, V2 = 1V, RL = 5Ω, I_{LD} = 300mA
30	Input/output R gain relative precision 1		–5	—	5	%	IIN1 = IIN2 = 250µA IIN2 output current precision based on IIN1 output current
31	Input/output R gain relative precision 2		–5	—	5	%	IIN1 = IIN2 = 500µA IIN2 output current precision based on IIN1 output current
32	Input/output R gain relative precision 3		–5	—	5	%	IIN1 = IIN2 = 750µA IIN2 output current precision based on IIN1 output current
33	Input/output W gain relative precision	GACCU	–5	—	5	%	
34	Input/output transmission band	FBAND	7	—	—	MHz	Frequency for input/output gain of –3dB

Test No.	Measurement item	Symbol	Min.	Typ.	Max.	Unit	Condition
<High frequency modulator>							
35	Frequency variable range	VARIF	200	—	600	MHz	
36	Amplitude variable range	VARIAMP	—	—	100	mAp-p	fmod = 400MHz
37	Frequency variation	FREQ	–10	—	11	%	fmod = 400MHz
38	Frequency temperature characteristic	TFREQ	—	TBD	—	%	fmod = 400MHz
39	Amplitude variation	AMP	—	31	—	mAp-p	fmod = 300MHz
40	Amplitude temperature characteristic	TAMP	—	TBD	—	%	fmod = 400MHz
41	OSCEN response time (ON)	OSCRES1	—	5	—	ns	fmod = 300MHz, RAMP = 10kΩ
42	OSCEN response time (OFF)	OSCRES2	—	5	—	ns	
<LDEN control>							
43	LDEN response time 1 (ON)	RLDRES1	—	—	1	µs	Time to reach 90% of Read set current (same condition as current consumption 3)
44	LDEN response time 1 (OFF)	RLDRES2	—	—	10	ns	Time to reach 10% of Read set current (same condition as current consumption 3)
45	LDEN response time 2 (ON)	WLDRES1	—	—	1	µs	Time to reach 90% of Write set current (same condition as current consumption 4)
46	LDEN response time 2 (OFF)	WLDRES2	—	—	10	ns	Time to reach 10% of Write set current (same condition as current consumption 4)

Electrical Characteristics Measurement Circuit



Description of Operation

(1) LD Drive Current Value Setting

The current controlled by the current setting pins IIN1, IIN2, IIN3, IIN4 and IIN5 is output from the LDOUT1 and LDOUT2 pins. IIN1, IIN2, IIN3, IIN4 and IIN5 can be set respectively by OUTEN and xOUTEN for the output drive current from the LDOUT pin.

(2) Differential Input and Single-end Input

External processing is required for the differential input and single-end input switching.
For the single-end input, if the device is used at the active Low, the OUTENREF pin and the OUTEN pin should be shorted externally; if it is used at the active High, the OUTENREF pin and the xOUTEN pin should be shorted externally. Leave the OUTENREF pin open for the differential input.

(3) Modulator Circuit

The modulator ON/OFF is controlled by the OSCEN pin.
For the DVD side, the modulator frequency is varied by the external resistance connected to the RFREQ1 pin and the modulator amplitude can be varied by the external resistance connected to the RAMP1 pin when the OSCMOD is high, and the RAMP11 pin when it is low.
For the CD side, the modulator frequency is varied by the external resistance connected to the RFREQ2 pin and the modulator amplitude can be varied by the external resistance connected to the RAMP2 pin.

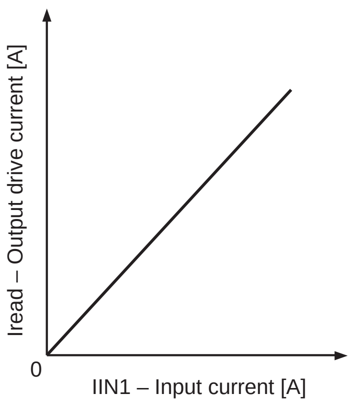
(4) R FREQ COMP Pin

The current depending on the internal resistance is generated using the R FREQ COMP pin external resistance to suppress the dispersion of the modulator frequency depending on the internal resistance.
The R FREQ COMP pin external resistance is recommended to be fixed to 22kΩ.

(5) Modulator Level Adjustment

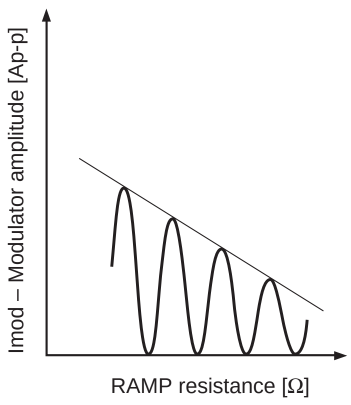
The modulator level adjustment can be performed by varying the IIN1 input current value.

Modulator OFF



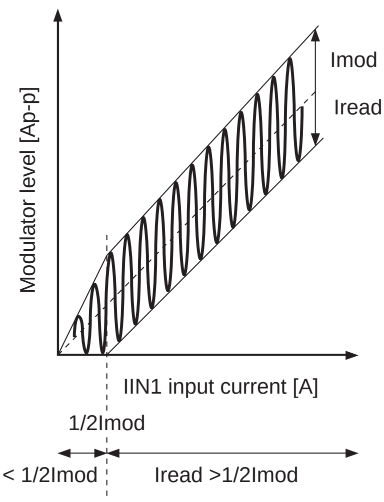
Iread = IIN1 × 125

Modulator amplitude



$$\text{Imod} \approx \frac{\text{RAMP pin voltage (1.26V)}}{\text{RAMP external resistance}} \times 200$$

Modulator level adjustment



Description of Functions

1. Logic Table

Output control

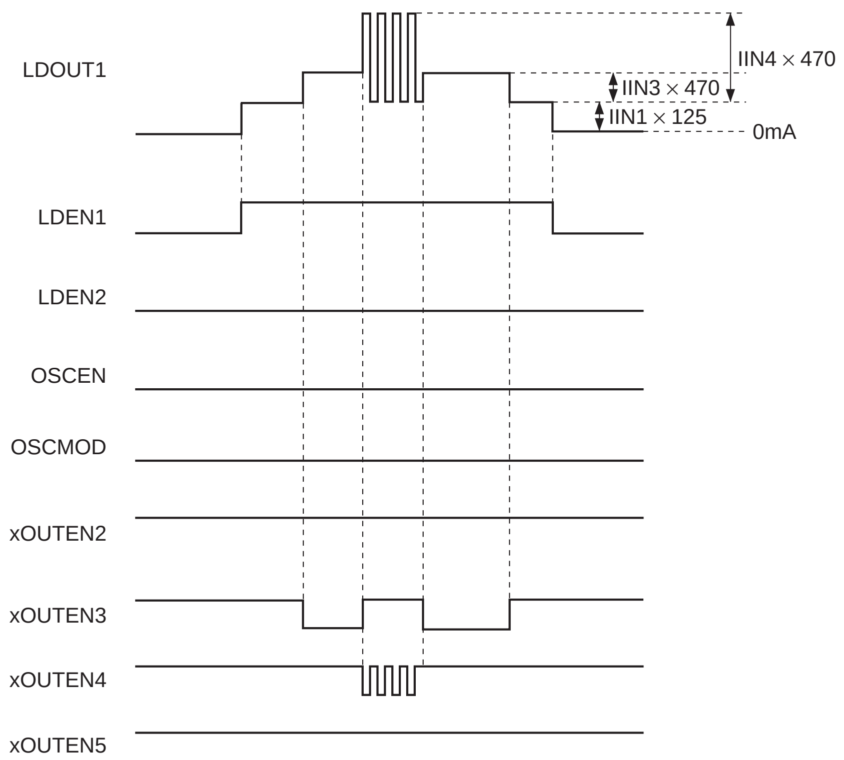
		IN1/IN2	IN3	IN4	IN5				
LDEN1	LDEN2	xOUTEN2	xOUTEN3	xOUTEN4	xOUTEN5	OSCEN	OSCMOD	LDOUT1 (DVD)	LDOUT2 (CD)
L	L	X	X	X	X	X	X	OFF	OFF
H	L	H	H	H	H	L	L	IIN1 × 125	OFF
H	L	L	H	H	H	L	L	IIN2 × 125	OFF
H	L	H	L	H	H	L	L	IIN1 × 125 + IIN3 × 470	OFF
H	L	H	H	L	H	L	L	IIN1 × 125 + IIN4 × 470	OFF
H	L	H	H	H	L	L	L	IIN1 × 125 + IIN5 × 470	OFF
H	L	H	L	L	L	L	L	IIN1 × 125 + (IIN3 + IIN4 + IIN5) × 470	OFF
L	H	H	H	H	H	L	L	OFF	IIN1 × 125
L	H	L	H	H	H	L	L	OFF	IIN2 × 125
L	H	H	L	H	H	L	L	OFF	IIN1 × 125 + IIN3 × 470
L	H	H	H	L	H	L	L	OFF	IIN1 × 125 + IIN4 × 470
L	H	H	H	H	L	L	L	OFF	IIN1 × 125 + IIN5 × 470
L	H	H	L	L	L	L	L	OFF	IIN1 × 125 + (IIN3 + IIN4 + IIN5) × 470
H	H	X	X	X	X	X	X	OFF (INHIBIT)	OFF (INHIBIT)

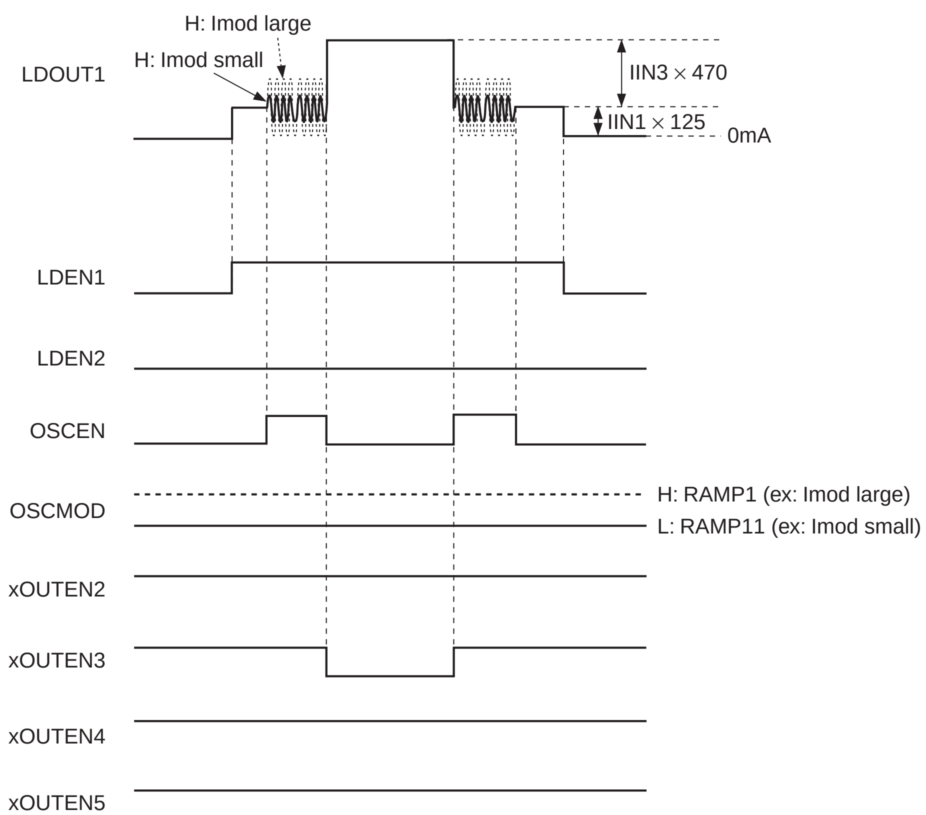
Module control

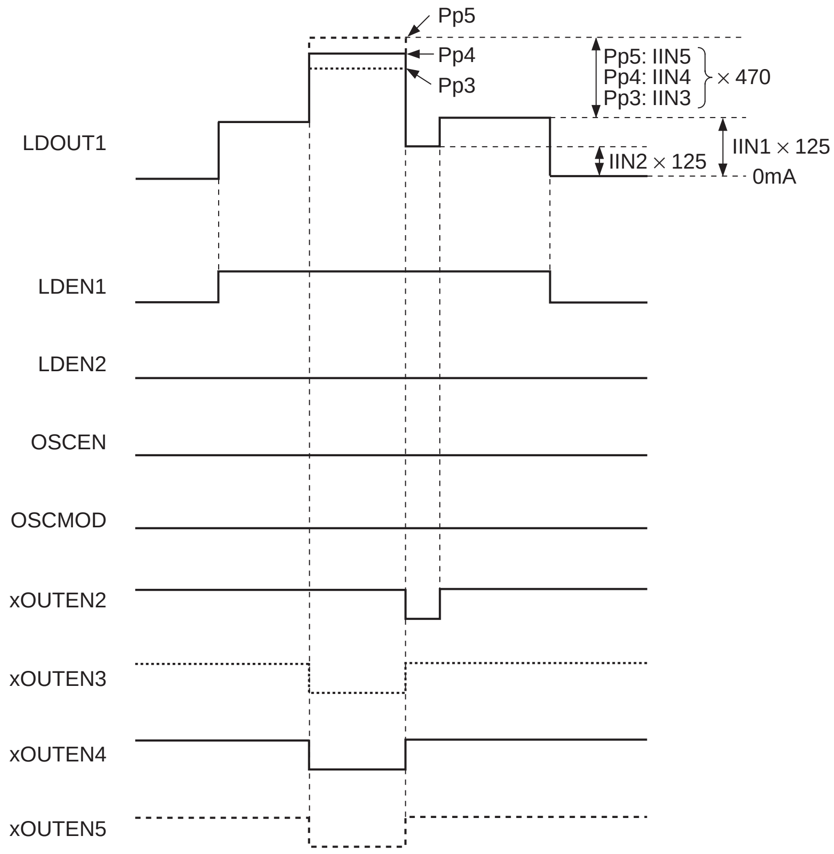
LDEN1	LDEN2	xOUTEN2	xOUTEN3	xOUTEN4	xOUTEN5	OSCEN	OSCMOD	LDOUT1	LDOUT2
L	L	X	X	X	X	X	X	OFF	OFF
H	L	X	X	X	X	L	H	MODOFF	OFF
H	L	X	X	X	X	H	H	MODON (R FREQ1, RAMP1)	OFF
H	L	X	X	X	X	H	L	MODON (R FREQ1, RAMP11)	OFF
L	H	X	X	X	X	L	X	OFF	MODOFF
L	H	X	X	X	X	H	X	OFF	MODON (R FREQ2, RAMP2)
H	H	X	X	X	X	X	X	OFF (INHIBIT)	OFF (INHIBIT)

Note: Module control does not depend on a data timing signals.

2. Timing Chart






Pp5
Pp4
Pp3
Pp5: IIN5
Pp4: IIN4
Pp3: IIN3
× 470
IIN1 × 125
IIN2 × 125
0mA
LDOUT1
LDEN1
LDEN2
OSCEN
OSCMOD
xOUTEN2
xOUTEN3
xOUTEN4
xOUTEN5

Notes on Operation

- Arrange the external resistance connected to the IIN1, IIN2, IIN3, IIN4 and IIN5 pins near the IC package to reduce the influence from other signal lines.

- Wiring between the output LDOUT pin and the laser diode, and wiring between the Vcc_LD pin and external decoupling capacitance should be the shortest. Making the distance for wiring long increases output waveform overshoots and undershoots caused by the influence of wiring inductance.

- The Vcc_LD pin's external decoupling capacitance ground can be grounded to the GND grounding the load from the LDOUT pin. This reverses the phase of the drive waveform at the LDOUT and Vcc_LD and moves in the direction that suppresses overshoots and undershoots.

- Temperature guarantee
  Thermal resistance (θj-a) when the CXA2697ER is mounted on PWB varies according to the set (PWB) and because it is difficult to predict along with the tendency for higher power for power consumption (Po), the following points should be considered when using.
  Use in a range that does not exceed a junction temperature of 150°C. Also, power consumption (P_O) should be below allowable power dissipation (P_D). Use with the thermal resistance (θj-a) of the PWB mounting lowered so that it can be operated normally at a maximum operating temperature of 75°C. To lower θj-a, radiating measures on the set, such as widening the GND region with the set PWB are needed. Also, the die-pad on the CXA2697ER 32-pin VQFN package is exposed on the surface, so thermal transmission from the IC surface is excellent. For that reason, it is possible to release heat to the set chassis thereby lowering the thermal resistance of the PWB mount.
  Find the thermal resistance (θj-a) when mounted on PWB and power consumption (P_O) using the following method.

$$Po = (Icc \times Vcc) - (Iop \times Vop)$$

Icc: IC current consumption when operating (Including Iop)
Iop: Output drive current flowed from the LDOUT pin to the Laser Diode
Vop: Operating voltage of the laser diode

Thermal resistance (θj-a) when mounted on PWB
Diode temperature coefficient XXmV/°C and the positive protection diode temperature characteristics are used to find this.
The V2 voltage found in (2) below cancels the voltage decrease caused by the wiring resistance between the positive protection diode connection Vcc and the Vcc pins as reference and is measured to find the precise temperature characteristics of the positive protection diode.

(1) V1 to LDEN pin voltage to Vcc pin voltage, Icc1 to current consumption when 0V is applied to the IIN1, IIN2, IIN3, IIN4 and IIN5 pins.
(2) V2 to LDEN pin voltage to Vcc pin voltage immediately after applying the arbitrary voltage to the IINx pin.
(3) V3 to LDEN pin voltage to Vcc pin voltage, Icc3 to current consumption when applying the arbitrary voltage to the IINx pin and heat reaches equilibrium.

ΔTj using the voltage drop (V1 to V2) between the positive protection diode connection Vcc and the Vcc pins that are the reference, as described above are:

$$\Delta Tj = ((V3 + (V1 - V2)) - V1)/XXmV/°C$$

Thermal resistance (θj-a) is:

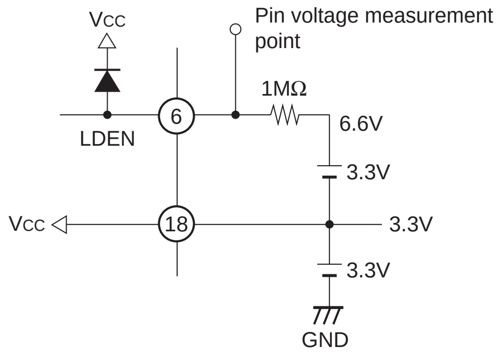
$$\theta j\text{-}a = \Delta Tj/(Icc3 - Icc1) \times Vcc - Iop \times Vop$$

- Allowable power dissipation (P_D) ≥ P_O [W]

$$P_D = (150°C - \text{Ambient temperature})/\theta j\text{-}a$$

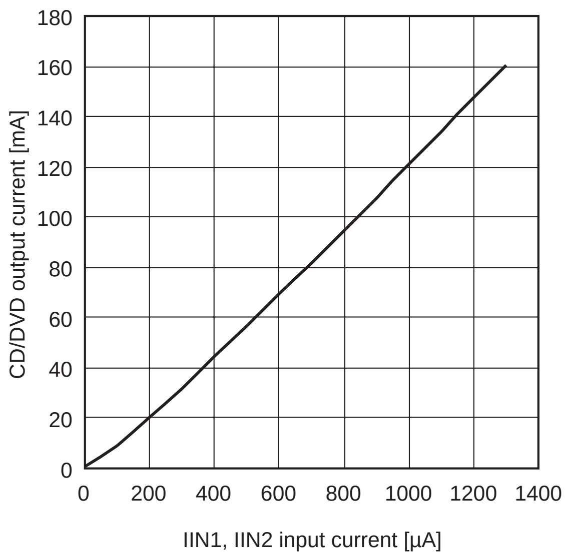
- Maximum operating temperature 75°C

$$(150°C - \Delta Tj) \geq 75°C$$

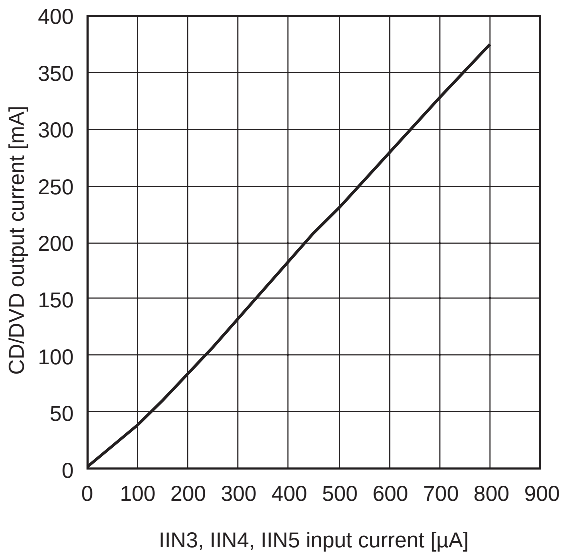


Example of Representative Characteristics

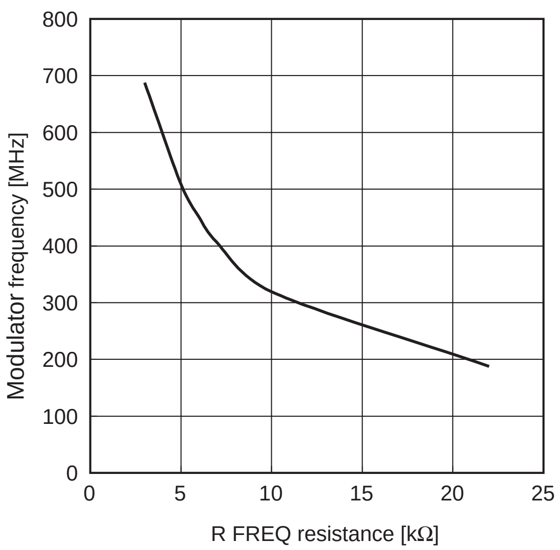
**IIN1, IIN2 input current vs.
CD/DVD output current characteristics**
Vcc_LD = 5V, Vcc = 3.3V, resistance load



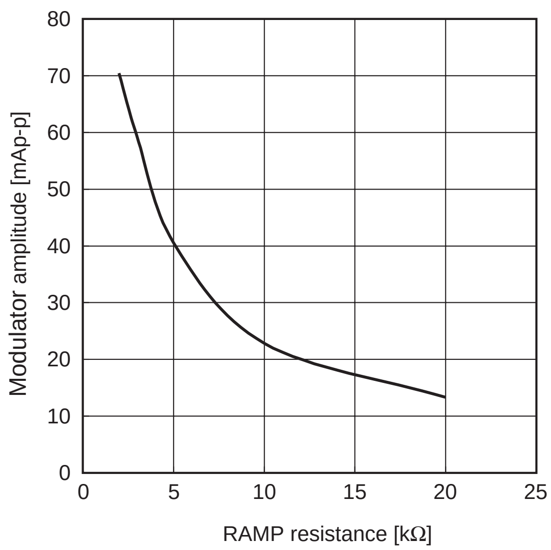
**IIN3, IIN4, IIN5 input current vs.
CD/DVD output current characteristics**
Vcc_LD = 5V, Vcc = 3.3V, resistance load



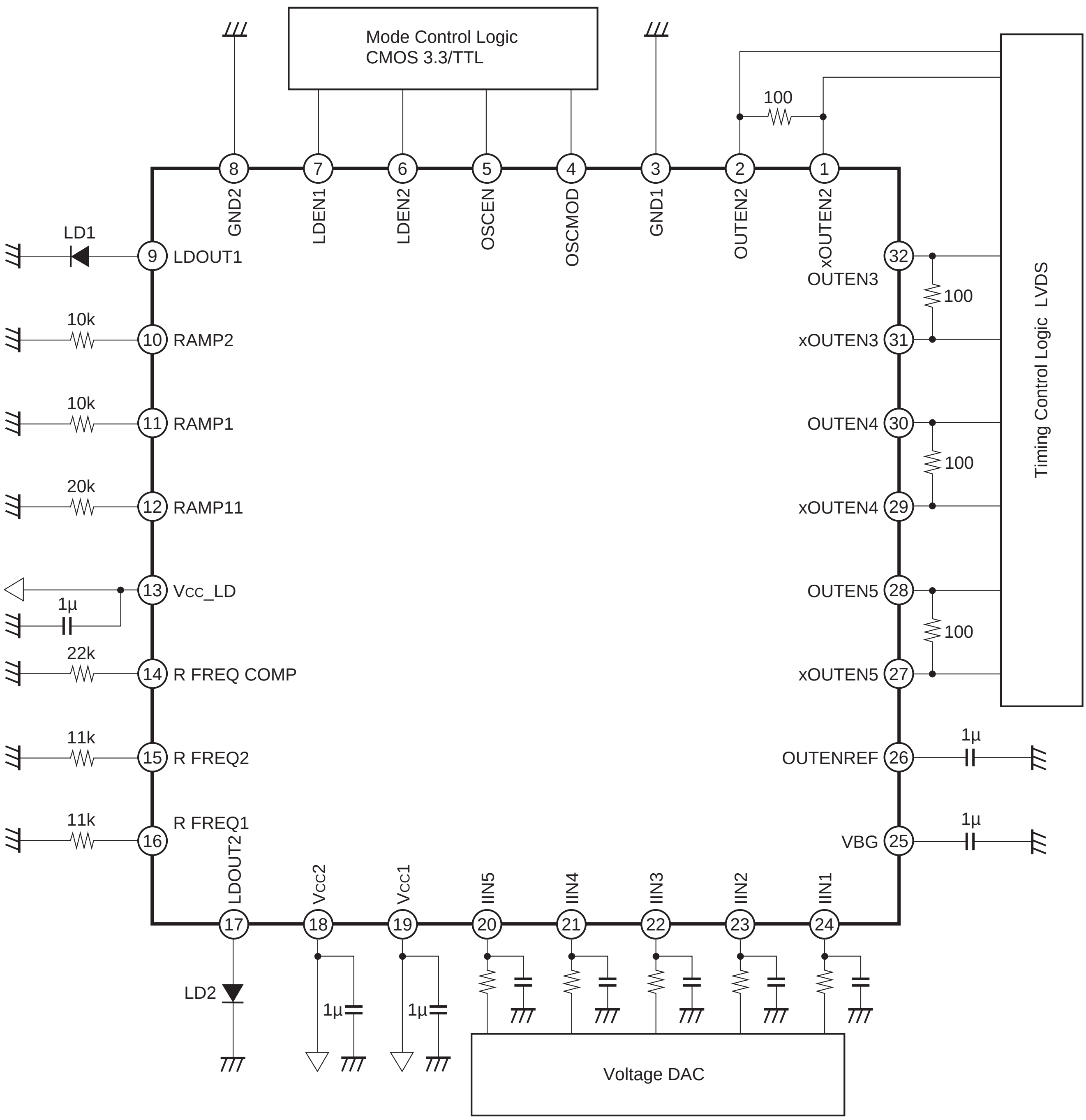
Modulator frequency control characteristics
Imod = 40mAp-p (RAMP = 5kΩ)
R FREQ COMP = 22kΩ



**RAMP resistance value vs.
Modulator waveform peak current characteristics**
fmod = 400MHz (R FREQ = 7kΩ)
R FREQ COMP = 22kΩ

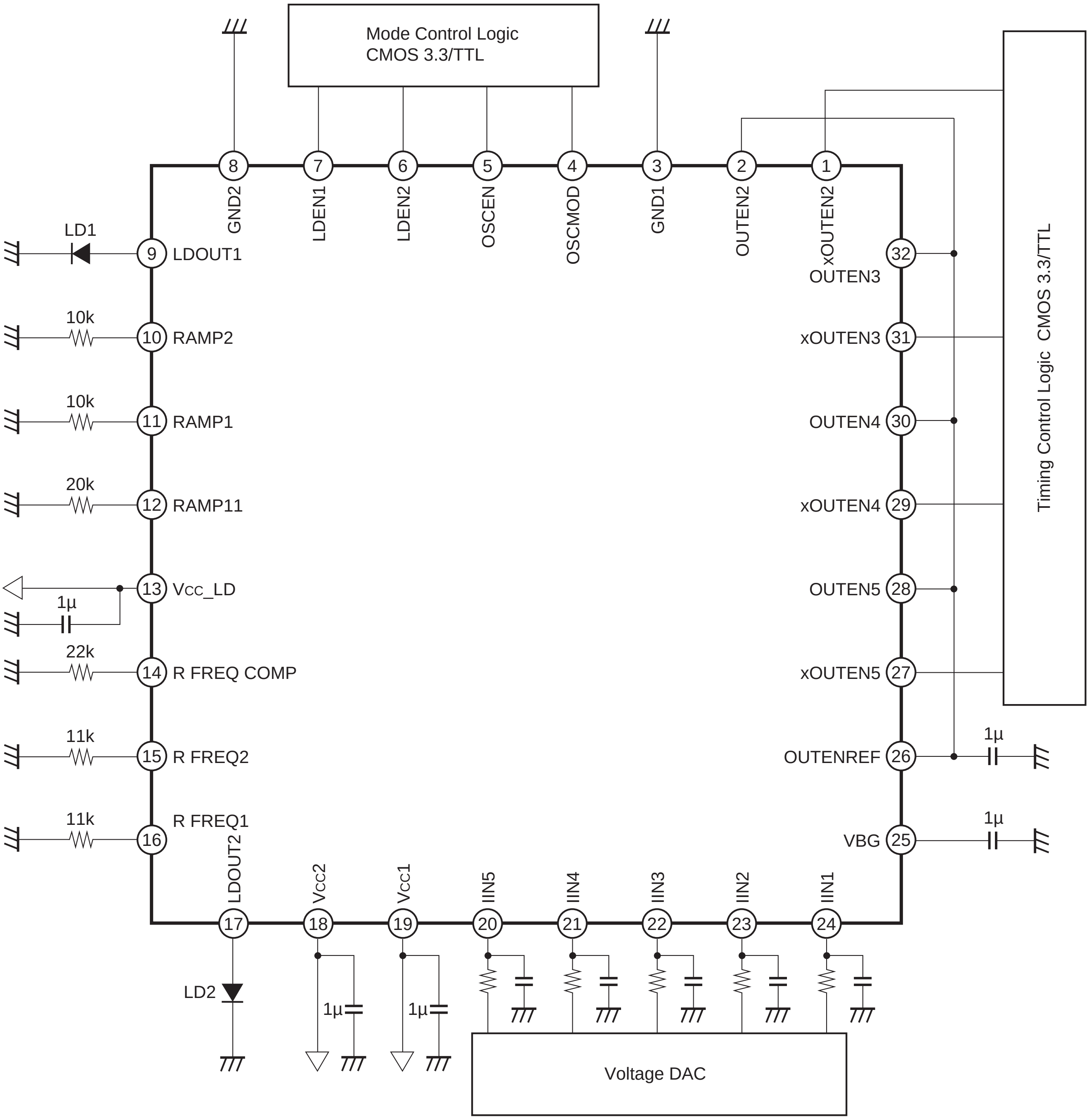


Application Circuit 1



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

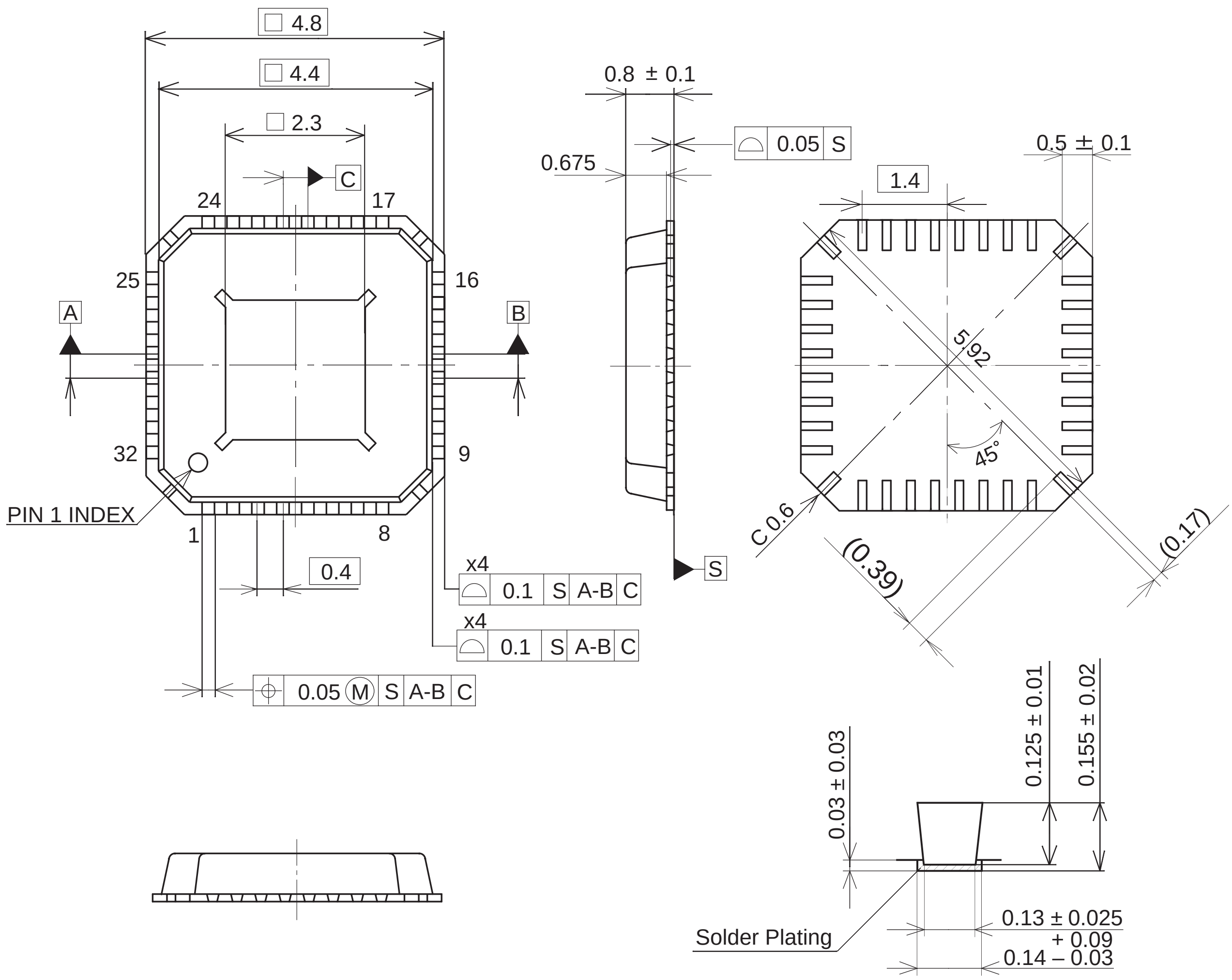
Application Circuit 2



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

32PIN VQFN (PLASTIC)



NOTE:1)The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

TERMINAL SECTION

PACKAGE STRUCTURE

SONY CODE	VQFN-32P-07
EIAJ CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g