

Video Amplifier Monolithic IC MM1002

Outline

This IC is a video amplifier that can perform superimpose. It has a built-in 75Ω driver.

Features

1. Built-in superimpose function
2. Built-in Y-C mix circuit
3. Vertical/horizontal sync signal output pin
4. Built-in clamp circuit (for Y signal only)
5. 75Ω driver built in
6. EVF driver built in
7. External pin (Pin 14) allows fine tuning of character level
8. Frequency response 5MHz
9. Power supply voltage 4.7V~5.3V

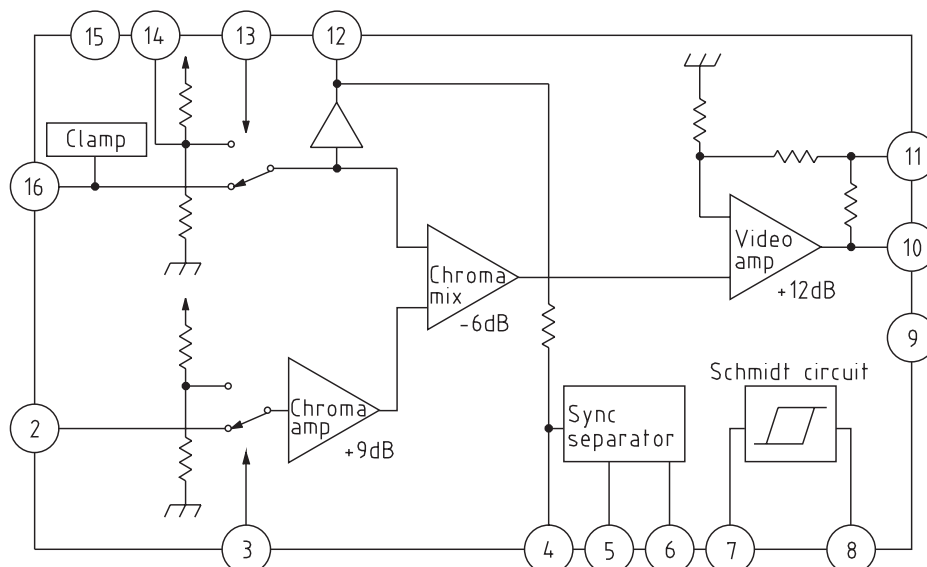
Package

SOP-16A (MM1002F)

Applications

1. TV
2. VCR
3. VCR with camera
4. Other video equipment

Block Diagram



Pin Description

Pin no.	Pin name	Internal equivalent circuit diagram	Pin no.	Pin name	Internal equivalent circuit diagram
1	NC		9	GND	
2	CHROMA IN		10	VIDEO OUT	
3	MIX		11	Anti-sag pin	
4	C1		12	EVF	
5	R		13	Character signal	
6	H-SYNC		14	Character signal level	
7	C2		15	Vcc	
8	V-SYNC		16	VIDEO IN	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC}	7	V
Allowable loss	P _d	350	mW

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=5.0V, pulse level 0V, short between V_{CC}-Id pin)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V _{CC}	V _{CC}		4.7	5.0	5.3	V
Consumption current	I _d	I _d			18.0	25.0	mA
EVF output							
Voltage gain	G _{U1}	TP3	SG-1 sweep signal 1V _{P-P} , 0.1MHz	-0.5	0.0	+0.5	dB
Differential gain	DG1	Buf	SG-1 staircase wave 1V _{P-P} APL=10, 50, 90%, SW→1		1	3	%
Differential phase	DP1	Buf	SG-1 staircase signal 1V _{P-P} APL=10, 50, 90%, SW→1		1	3	deg
Frequency characteristic	fc1	TP3	SG-1 sweep signal 1V _{P-P} 5MHz/0.1MHz *1	-1	0	1	dB
Video amp output							
Voltage gain	G _{U2}	TP4	SG-1 sweep wave 1V _{P-P} , 0.1MHz	5.5	6.0	6.5	dB
Differential gain	DG2	Buf	SG-1 staircase wave 1V _{P-P} APL=10, 50, 90%, SW→2		1	3	%
Differential phase	DP2	Buf	SG-1 staircase signal 1V _{P-P} APL=10, 50, 90%, SW→2		1	3	deg
Frequency characteristic	fc2	TP4	SG-1 sweep signal 1V _{P-P} 5MHz/0.1MHz *1	-1	0	1	dB
Character addition							
Character level	V _{CL}	TP4	SG-1 staircase wave (no chroma signal) 1V _{P-P} H _D horizontal sync signal TP7 pulse level 5V	115	120	125	IRE
Input threshold voltage	V _{TH13}	TP7	SG-1 staircase wave (no chroma signal) 1V _{P-P} H _D horizontal sync signal TP7 pulse level L→H *2	0.7	1.4	2.1	V
Chroma amp							
Voltage gain	G _{U3}	TP4	SG-2 sine wave 0.1V _{P-P} , 0.1MHz	13.5	15.0	16.5	dB
Frequency characteristic	fc3	TP4	SG-2 sine wave 0.1V _{P-P} 5MHz/0.1MHz *1	-1	0	1	dB
Crosstalk	C	TP4	SG-2 sine wave 0.1V _{P-P} , 4MHz TP8 pulse level 5V *3		-60	-40	dB
Input threshold voltage	V _{TH3}	TP8	SG-2 sine wave 0.1V _{P-P} , 4MHz TP8 pulse level L→H *4	0.7	1.4	2.1	V
Sync separation							
Sync separation level	V _{SEPA}	TP1	SG-1 staircase wave (no chroma signal) 1V _{P-P} SG-1 SYNC level max→min *5	55	110	165	mV
7PIN threshold voltage	V _{TH7H}	TP9	TP9 DC voltage 0V→H *6	1.9	2.1	2.3	V
	V _{TH7L}		TP9 DC voltage 5V→L *6	1.1	1.3	1.5	V
Horizontal sync output voltage	V _{OH6}	TP10	SG-1 staircase wave (no chroma signal) 1V _{P-P} *7	4.8	5.0		V
	V _{OL6}				0.2	0.4	V
Vertical sync output voltage	V _{OH8}	TP11	SG-1 staircase wave (no chroma signal) 1V _{P-P} *8	4.8	5.0		V
	V _{OL8}				0.2	0.4	V

Notes : *1 Frequency response f_{c1} , f_{c2} , f_{c3}

For the same conditions as the G_{u1} measurement, given video output for 0.1MHz as V_2 , and for 5MHz as V_1 , f_{c1} is obtained as follows. The same applies for f_{c2} and f_{c3} .

$$f_{c1} = 20 \text{LOG} \frac{V_2}{V_1} \text{ dB}$$

*2 Character addition input threshold voltage V_{TH13}

For the same conditions as the V_{CL} measurement, adjust VR1 to raise pulse level gradually, and TP7 pulse level when a character signal is output on TP4 is V_{TH13} .

*3 Chroma amp crosstalk C

Given TP4 level when there is no pulse input as V_3 , and the level when pulse input exists as V_4 , C is obtained as follows.

$$C = 20 \text{LOG} \frac{V_4}{V_3} \text{ dB}$$

*4 Chroma amp input threshold voltage V_{TH3}

For the same conditions as C measurement, adjust VR2 to raise TP8 level from 0V. The TP8 level when TP4 level changes at pulse input is V_{TH3} .

*5 Sync separation sync separation level V_{SEPA}

Input a $1V_{P-P}$ staircase signal (no chroma signal) to SG-1, and gradually shrink the sync signal. TP1 sync level when TP10 horizontal sync signal starts to disappear is V_{SEPA} .

*6 Sync separation Pin 7 threshold voltage V_{TH7H} , V_{TH7L}

Impress external DC voltage on TP9 and raise gradually from 0V. TP9 level when TP11 level goes from high to low is V_{TH7H} . Lower gradually from 5V. TP9 level when TP11 level goes from low to high is V_{TH7L} .

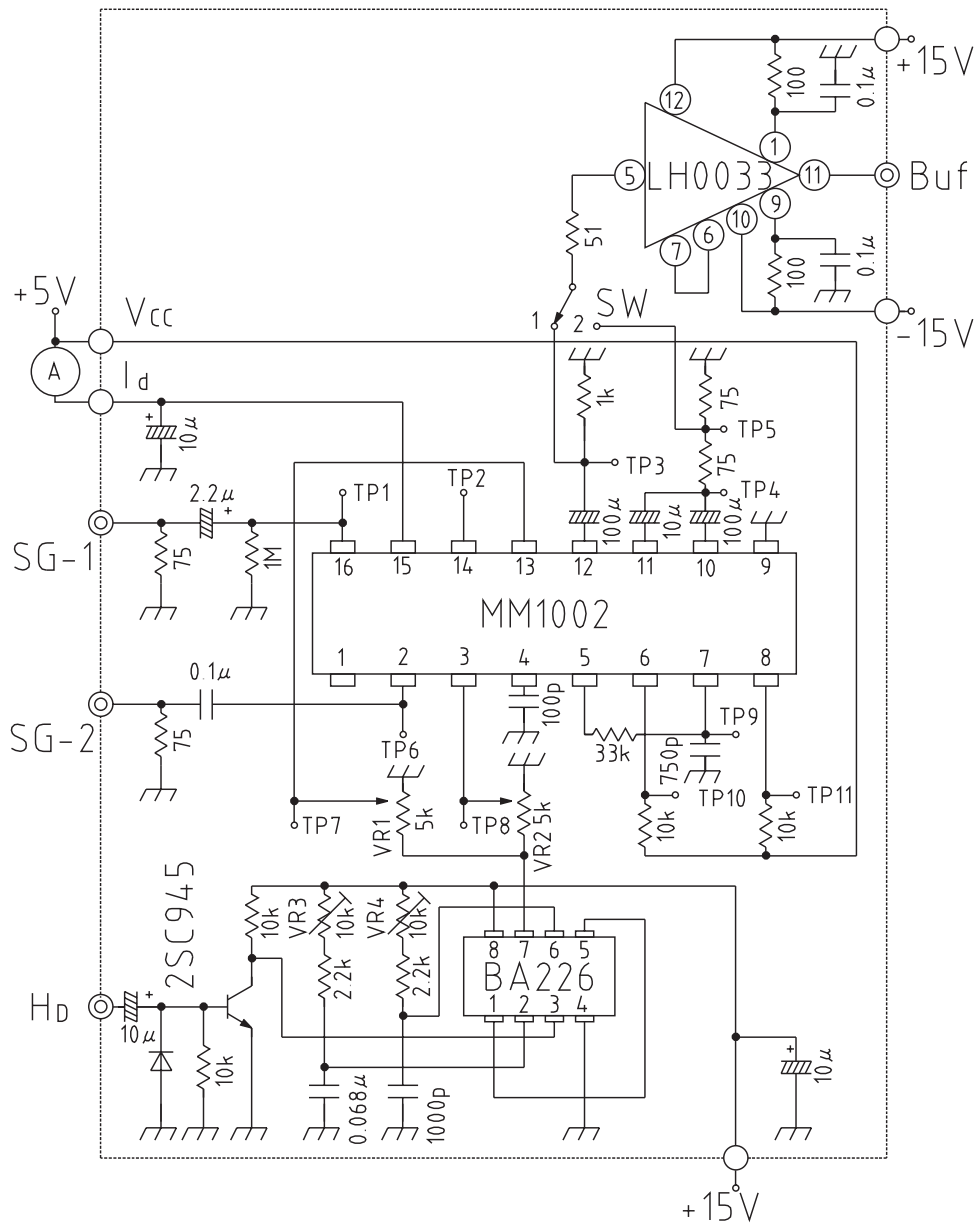
*7 Sync separation horizontal sync output voltage V_{OH6} , V_{OL6}

TP10 high level when a $1V_{P-P}$ staircase signal (no chroma signal) is input to SG-1 is V_{OH6} , and low level is V_{OL6} .

*8 Sync separation vertical sync output voltage V_{OH8} , V_{OL8}

TP10 high level when a $1V_{P-P}$ staircase signal (no chroma signal) is input to SG-1 is V_{OH8} , and low level is V_{OL8} .

Measuring Circuit



Application Circuits

