MOTOROLA
■ SEMICONDUCTOR ■
TECHNICAL DATA

Designer's Data Sheet
Power Field Effect Transistor
### N-Channel Enhancement-Mode
Silicon Gate

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

● Silicon Gate for Fast Switching Speeds — Switching Times
    Specified at 100°C
● Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified
    at Elevated Temperature
● Rugged — SOA is Power Dissipation Limited
● Source-to-Drain Diode Characterized for Use With Inductive Loads

MTP12N05E

Motorola Preferred Device

TMOS POWER FET
12 AMPERES
$R_{DS(on)} = 0.12$ OHM
50 VOLTS

CASE 221A-06
TO-220AB
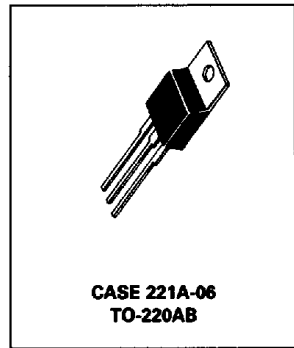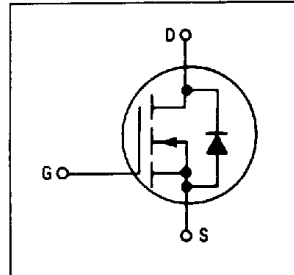
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage ($R_{GS} = 1$ MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	I_D I_{DM}	12 30	Adc
Total Power Dissipation @ $T_C = 25$°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient TO-204 TO-220	$R_{\theta JA}$	30 62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C

Preferred device is a Motorola recommended choice for future use and best overall value.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)	$R_{DS(on)}$	—	0.12	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 100°C)	$V_{DS(on)}$	— —	3 2.8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)	g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	400	pF
Output Capacitance	C_{oss}	—	300	
Reverse Transfer Capacitance	C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time	$t_{d(on)}$	—	60	ns
Rise Time	t_r	—	160	
Turn-Off Delay Time	$t_{d(off)}$	—	80	
Fall Time	t_f	—	110	
Total Gate Charge	Q_g	13 (Typ)	26	nC
Gate-Source Charge	Q_{gs}	6 (Typ)	—	
Gate-Drain Charge	Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage	V_{SD}	1.8 (Typ)	3.2	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

Dynamic Characteristics conditions: (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11

Switching Characteristics conditions: (V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14

Gate Charge conditions: (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12

Source Drain Diode conditions: (I_S = Rated I_D, V_{GS} = 0)

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

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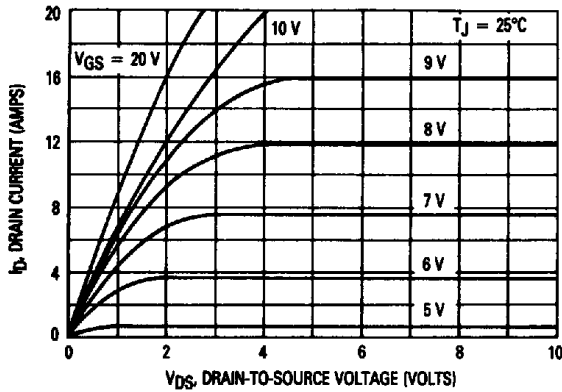**TYPICAL ELECTRICAL CHARACTERISTICS**

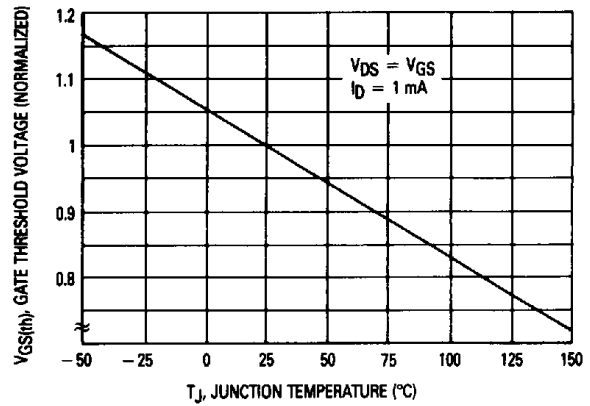Figure 1. On-Region Characteristics

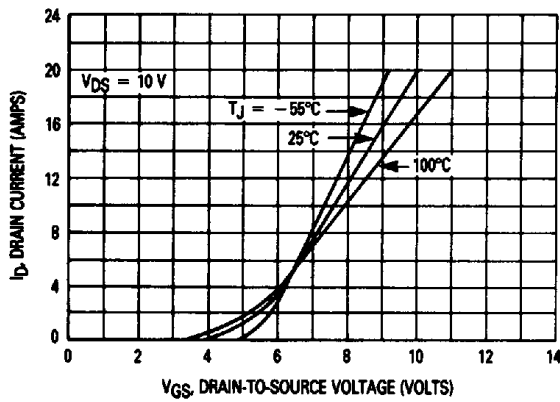Figure 2. Gate-Threshold Voltage Variation With Temperature
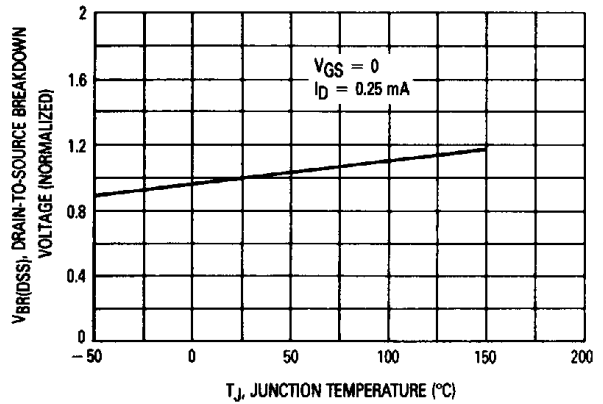

Figure 3. Transfer Characteristics

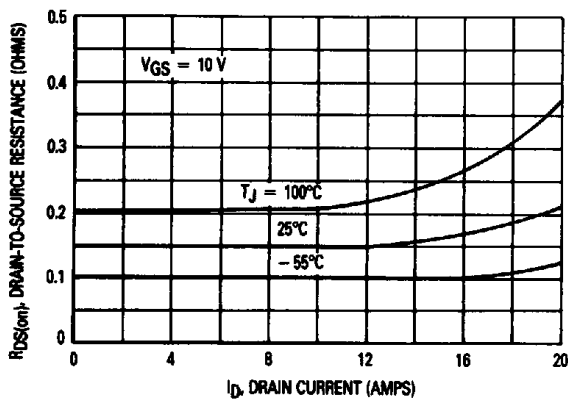Figure 4. Breakdown Voltage Variation With Temperature
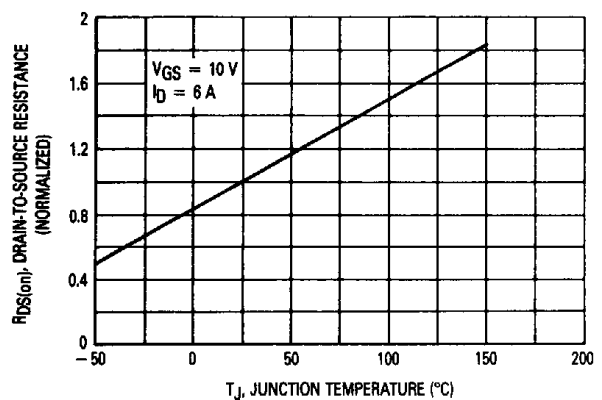

Figure 5. On-Resistance versus Drain Current

Figure 6. On-Resistance Variation With Temperature
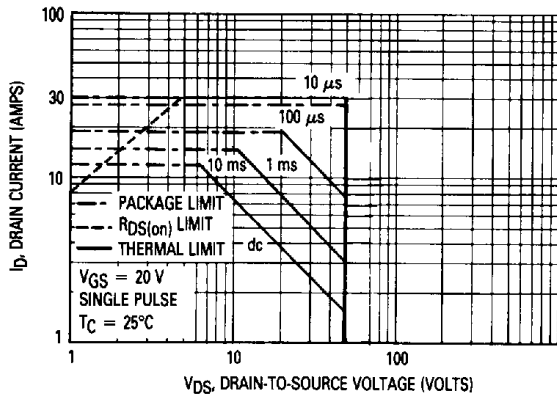
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SAFE OPERATING AREA INFORMATION
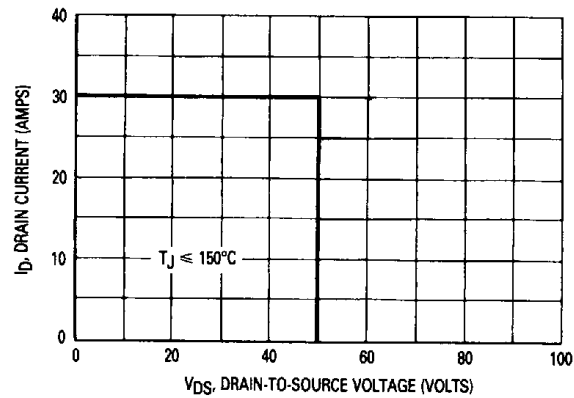

Figure 7. Maximum Rated Forward Biased
Safe Operating Area

Figure 8. Maximum Rated Switching
Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:
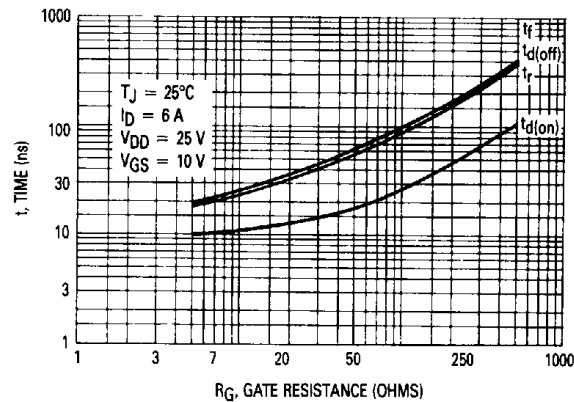
$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time
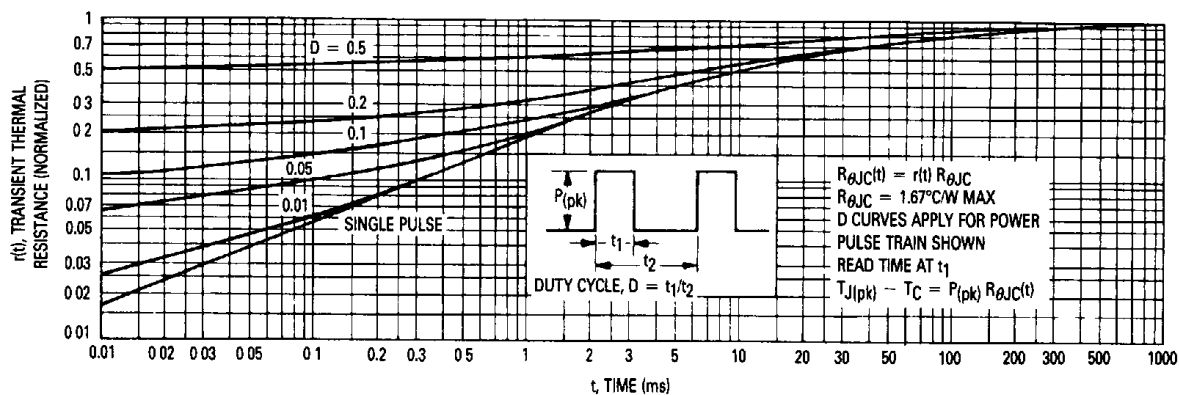Variation versus Gate Resistance
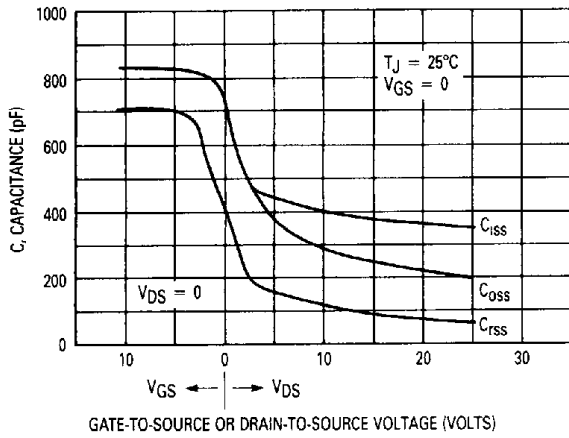

Figure 10. Thermal Response

MOTOROLA TMOS POWER MOSFET DATA

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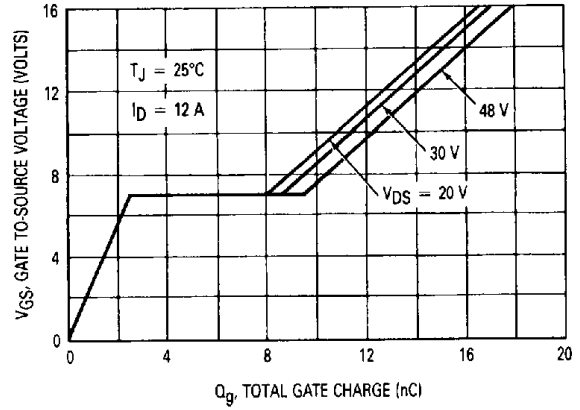
Figure 11. Capacitance Variation

Figure 12. Gate Charge versus
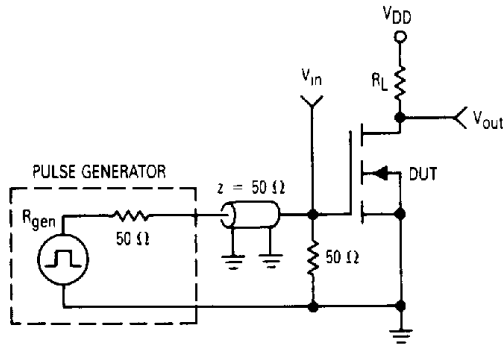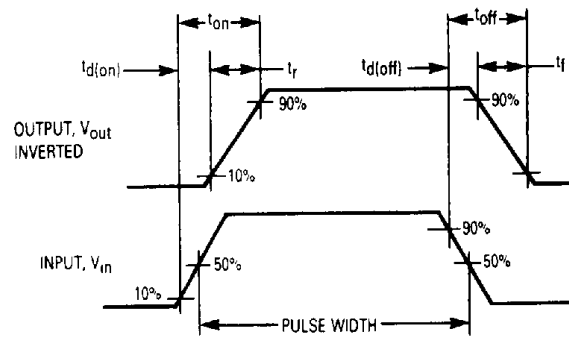Gate-to-Source Voltage

RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms