

SED1606D_{0A}/D_{0B}

CMOS LCD SEGMENT DRIVER

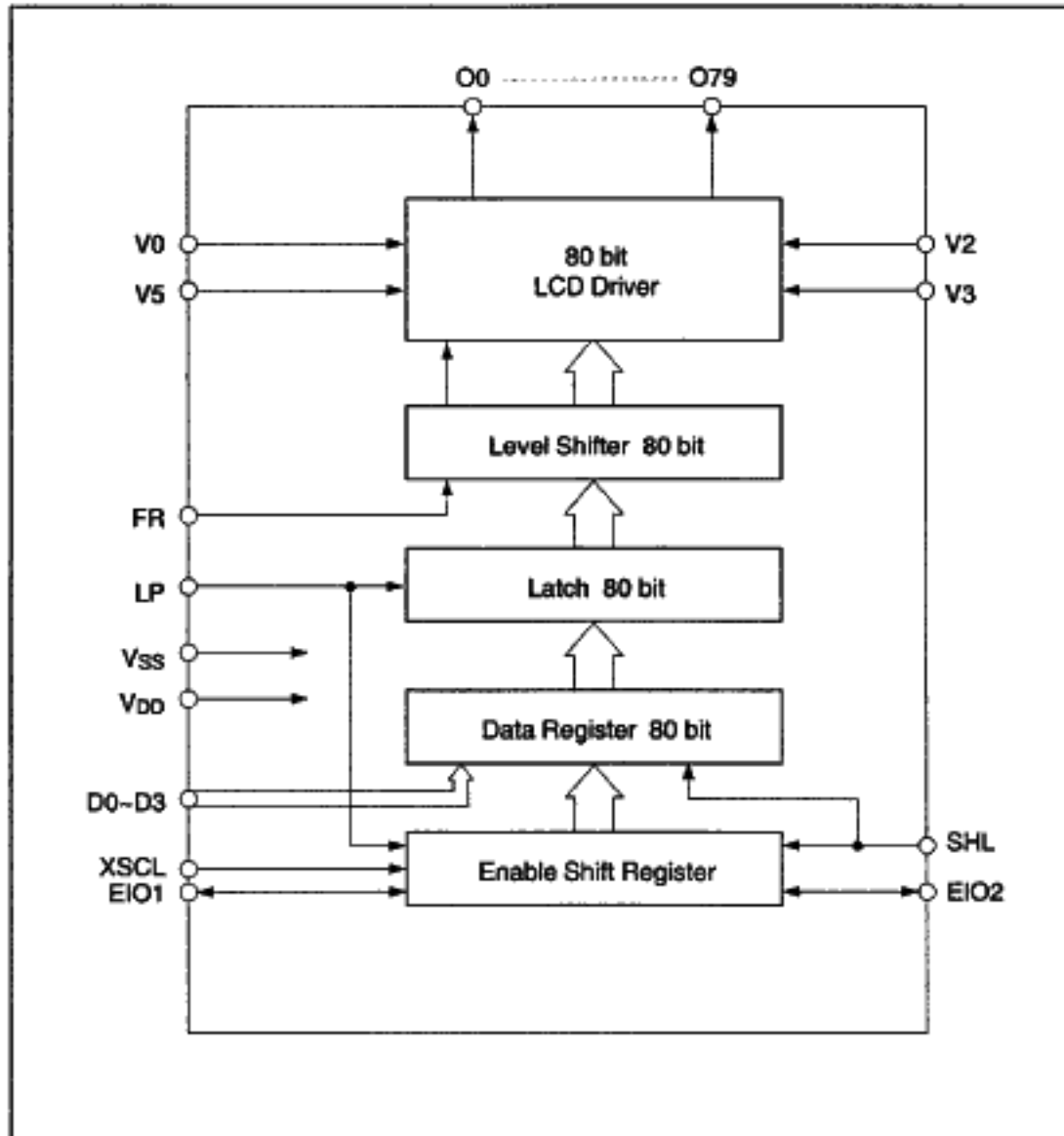
■ DESCRIPTION

The SED1606 is an 80-output segment (column) driver for use in combination with an SED1635. It is provided with high-vision measure of the LCD display and adopts high speed inable chain system for low power operation and slim chip shape suitable for minimizing of the LCD panel. Also, low voltage operation of the logic power source suits a wide range of applications.

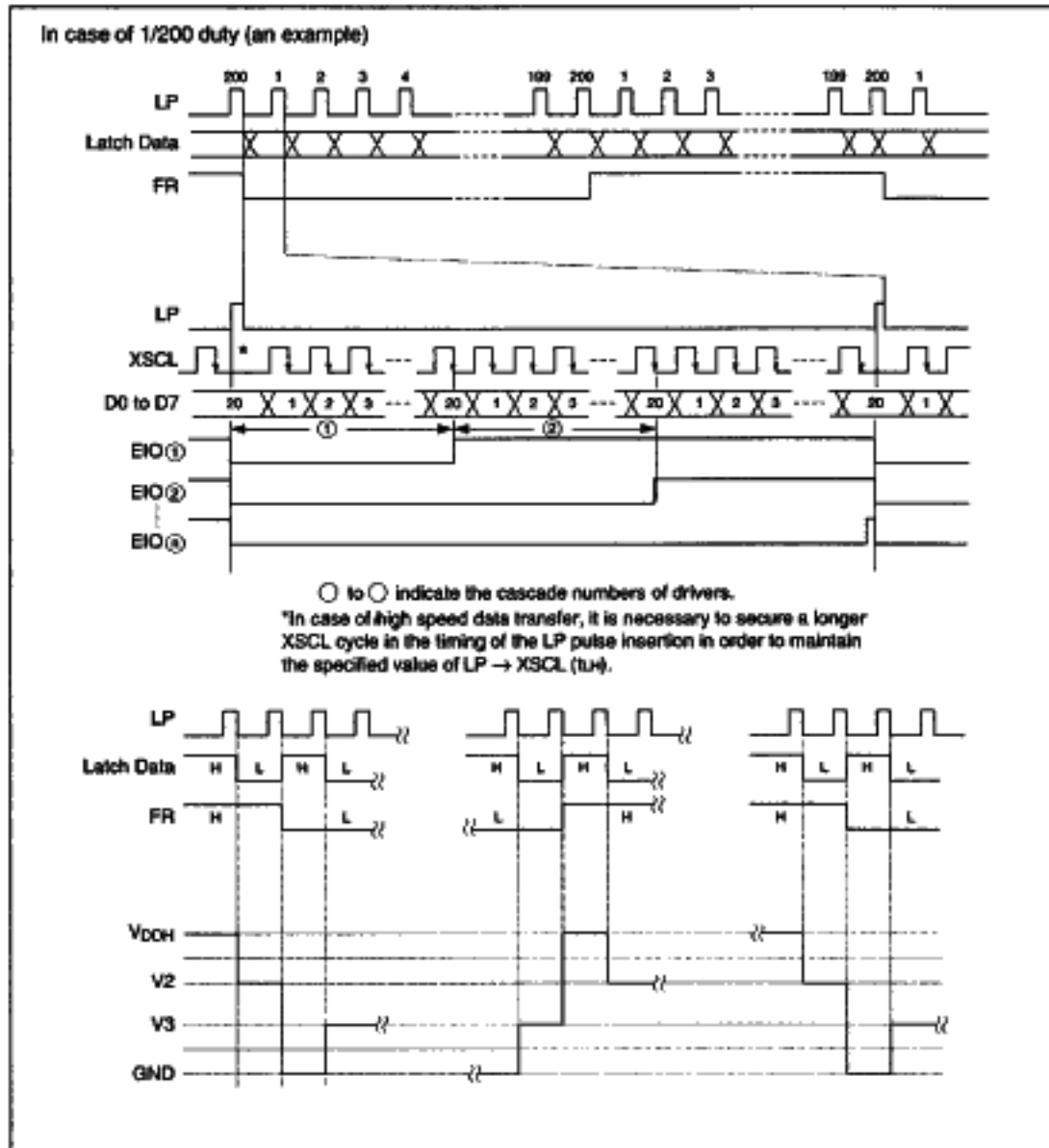
■ FEATURES

- LCD driver output number 80
- Ultra-slim chip
- Low current consumption
- Low voltage operation -2.7V max.
- Wide range of liquid crystal drive voltage -8 to -28V
- High speed and low power data transfer is possible by adoption of the 4-bit bus inable chain system.
Shift clock frequency:
 - 6.5MHz (at -2.7V)
 - 10.0MHz (at -4.5V)
- Non-bias display off function
- Pin selection of the output shift direction is available
- Offset bias regulation of the liquid crystal power is possible depending on the V_{cc} level
- Logic system power source -2.7 to -5.5V
- Product shapes

■ BLOCK DIAGRAM



■ TIMING DIAGRAM



■ FUNCTIONS

● Inable Shift Register

The inable shift register is a bi-directional shift register where with the shift direction is determined by the SHL. Inputs and outputs of such shift register are used to store data bus signals to the data register. When inable signals are in the disable state, the internal clock signal and data bus are fixed to "L" to become the power save mode.

When using multiple units of the segment driver, EIO terminals of each driver should be connected by the cascade connection and the EIO terminals of the top end driver should be connected to "V_{cc}". (Refer to the connection example). Since the inable control circuit automatically detects when all the 80-bit data are taken in and automatically transfers the inable signal, control signals from a controlling LSI are not needed.

● Data Register

This is a register for serial and parallel conversion of data bus signals by means of the inable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independently from the shift clock input number.

● Latch

It takes in the contents of the data register by means of the trailing edge trigger of the LP to transmit the output to the level shifter.

● Level Shifter

This is a level interface circuit to convert the voltage level of signals from logic level to LCD driving level.

● LCD Driver

It outputs the LCD drive voltage.

Relations among data bus signals, alternating signals FR and the segment output voltage are given below.

Data Bus Signals	FR	O Output Voltage
H	H	V ₀
	L	V ₅
L	H	V ₂
	L	V ₃

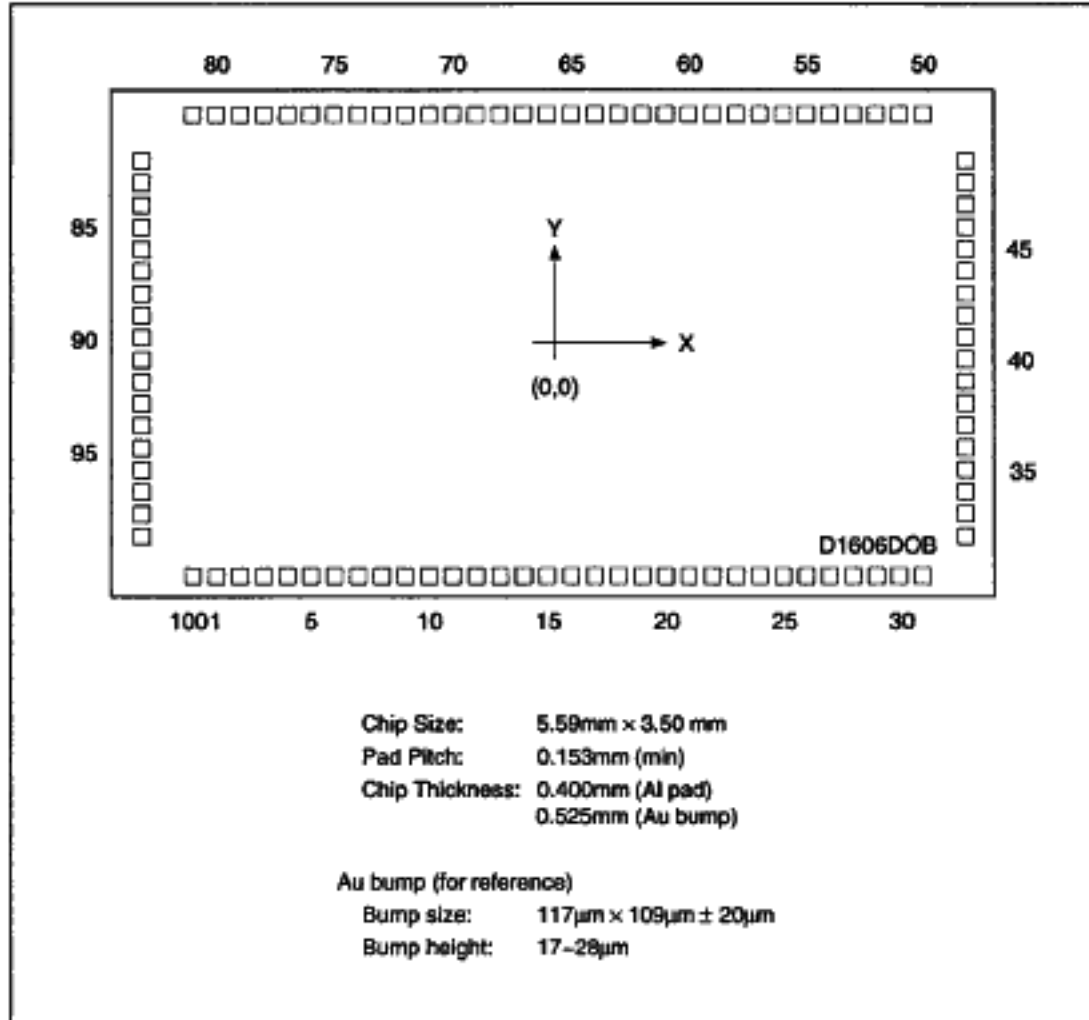
■ FUNCTIONS OF THE TERMINALS

Terminal Name	I/O	Description	Numbers of Pins																																							
O 0 ~ O79	O	LCD driving segment (column) output The output level varies at the trailing edge of the LP.	80																																							
D0 ~ D3	I	Display data input	4																																							
XSCL	I	Shift clock input of display data (trailing edge trigger)	1																																							
LP	I	Latch pulse input of display data (trailing edge trigger)	1																																							
EIO1 EIO2	I/O	Enable input and output Set to input or output depending on the SHL input level. The output is reset by the LP input and, after receiving 80 bit data, it automatically rises to "H"	2																																							
SHL	I	Shifting direction choice, and input/output controlling input to the EIO terminal When data is input to (D3, D2, ..., D0) terminals in the order of (a3, a2, a1, a0) (b3,b2,b1,b0)..... (t2, t2, t1, t0), relations between data and segment outputs are as follows. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="7">O Output</th> <th colspan="2">EIO</th> </tr> <tr> <th>79</th> <th>78</th> <th>77</th> <th>...</th> <th>2</th> <th>1</th> <th>0</th> <th>EIO1</th> <th>EIO2</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>a3</td> <td>a2</td> <td>a1</td> <td>....</td> <td>t2</td> <td>t1</td> <td>t0</td> <td>Output</td> <td>Input</td> </tr> <tr> <td>L</td> <td>t0</td> <td>t1</td> <td>t2</td> <td>....</td> <td>a1</td> <td>a2</td> <td>a3</td> <td>Input</td> <td>Output</td> </tr> </tbody> </table> Note: Relations between the data and segment outputs are determined independent from the shift clock number.	SHL	O Output							EIO		79	78	77	...	2	1	0	EIO1	EIO2	H	a3	a2	a1	t2	t1	t0	Output	Input	L	t0	t1	t2	a1	a2	a3	Input	Output	1
SHL	O Output							EIO																																		
	79	78	77	...	2	1	0	EIO1	EIO2																																	
H	a3	a2	a1	t2	t1	t0	Output	Input																																	
L	t0	t1	t2	a1	a2	a3	Input	Output																																	
FR	I	Input of the alternating signal of the LCD drive output	1																																							
V _{cc} , V _{ss}	Power source	Power supply for the logics V _{cc} : 0V V _{ss} : -2.7 ~ -5.5V	2																																							
V ₀ , V ₂ , V ₃ , V ₅	Power source	Power supply for the LCD driver circuit V _{cc} : 0V V ₅ : -8 ~ -28V V _{cc} ≥ V ₀ ≥ V ₂ 6/9 V ₅ *1 3/9 V ₅ ≤ V ₃ ≤ V ₅	4																																							

Total 100
(including NC4)

*1. Be sure to connect pairs of V0 ~ V5 to respective LCD power sources.

■ PAD LAYOUT



■ PAD COORDINATES

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	O 0	-2227	-1578	35	O 34	2622	-871	69	O 68	-537	1578
2	O 1	-2073		36	O 35		-713	70	O 69	-691	
3	O 2	-1920		37	O 36		-554	71	O 70	-846	
4	O 3	-1768		38	O 37		-398	72	O 71	-998	
5	O 4	-1612		39	O 38		-238	73	O 72	-1152	
6	O 5	-1459		40	O 39		-79	74	O 73	-1305	
7	O 6	-1305		41	O 40		79	75	O 74	-1459	
8	O 7	-1152		42	O 41		238	76	O 75	-1613	
9	O 8	-998		43	O 42		398	77	O 76	-1768	
10	O 9	-845		44	O 43		554	78	O 77	-1920	
11	O 10	-691		45	O 44		713	79	O 78	-2073	
12	O 11	-537		46	O 45		871	80	O 79	-2227	
13	O 12	-384		47	O 46		1029	81	EIO2	-2381	
14	O 13	-230		48	O 47		1188	82	D0	-2622	1346
15	O 14	-78		49	O 48		1348	83	D1		1192
16	O 15	77		50	O 49	2381	1578	84	D2		1039
17	O 16	231		51	O 50	2228		85	D3		885
18	O 17	384		52	O 51	2074		86			732
19	O 18	538		53	O 52	1921		87			578
20	O 19	692		54	O 53	1767		88			424
21	O 20	845		55	O 54	1613		89			271
22	O 21	999		56	O 55	1460		90	VDD		106
23	O 22	1152		57	O 56	1306		91	VSS		-58
24	O 23	1306		58	O 57	1152		92	V0		-224
25	O 24	1460		59	O 58	999		93	V2		-389
26	O 25	1613		60	O 59	845		94	V3		-553
27	O 26	1767		61	O 60	692		95	V5		-718
28	O 27	1921		62	O 61	538		96	SHL	-2611	-885
29	O 28	2074		63	O 62	384		97	XSCL		-1039
30	O 29	2228		64	O 63	231		98	LP		-1192
31	O 30	2381		65	O 64	77		99	FR		-1346
32	O 31	2622	-1346	66	O 65	-78		100	EIO1	-2381	-1578
33	O 32	2622	-1188	67	O 66	-230					
34	O 33	2622	-1029	68	O 67	-384					

■ ELECTRICAL CHARACTERISTICS

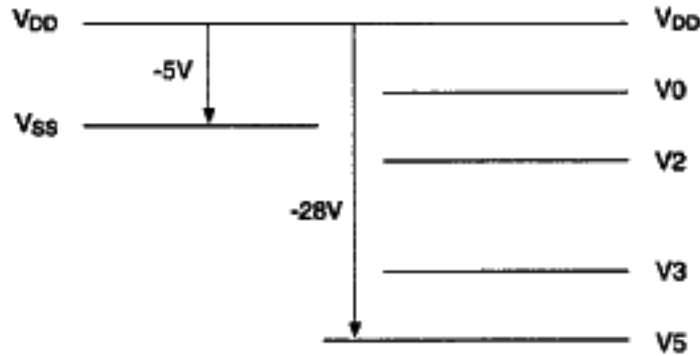
● Absolute Maximum Rating

Parameters	Codes	Ratings	Units
Power voltage (1)	V _{ss}	-7.0 - +0.3	V
Power voltage (1)	V _s	-30.0 - +0.3	V
Power voltage (3)	V _s , V ₂ , V ₃	V _s - 0.3 - V _{DD} +0.3	V
Input voltage	V _i	V _{ss} - 0.3 - V _{DD} +0.3	V
Output voltage	V _o	V _{ss} - 0.3 - V _{DD} +0.3	V
EIO output current	I _{oi}	20	mA
Working temperature	T _{opr}	-40 - +85	°C
Storage temperature 1	T _{sig1}	-65 - +150	°C

Note 1. All the above voltages are based on V_{DD} = 0V.

Note 2. The storing temperature 1 specifies that of chips proper.

Note 3. Voltage of V₀, V₂ and V₃ should always be maintained under a condition of V_{ss} ≥ V₀ ≥ V₂ ≥ V₃ ≥ V_S.



Note 4. When logic power becomes floating state or if V_{ss} = -2.8 or beyond while the LCD driver power source is being applied, the LSI may be permanently damaged and avoid such circumstances.

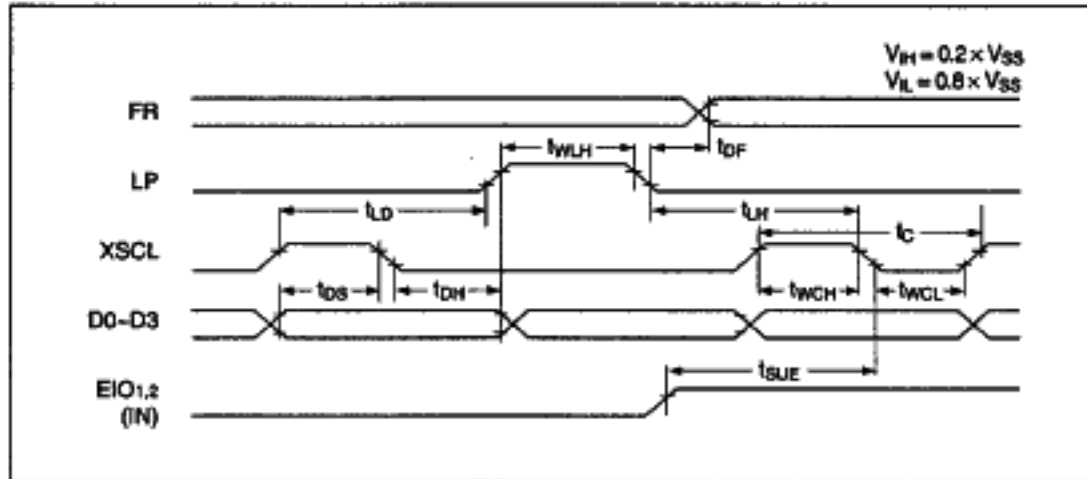
Pay extra attention to the power sequence at times of turning on and turning off the power supply.

● DC Characteristics

Unless otherwise designated, $V_{DD} = V_0 = 0V$, $V_{SS} = -5.0 \pm 10\%$ and $T_a = -40$ to $85^\circ C$

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}	—	V_{SS}	-5.5	-5.0	-2.7	V
Recommended working voltage	V_1	—	V_1	-28.0	—	-12.0	V
Operable voltage	V_1	Function	V_1	—	—	-8.0	V
Power voltage (2)	V_0	Recommended value	V_0	$V_{DD} - 2.5$	—	V_{DD}	V
Power voltage (3)	V_2	Recommended value	V_2	V_2	$3/9 V_1$	—	V
Power voltage (4)	V_2	Recommended value	V_2	V_2	—	$6/9 V_1$	V
High level input voltage	V_{IH}	$V_{SS} = 2.7 - 5.5V$	EIO1, EIO2, FR D0-D3, XSCL SHL, LP,	$0.2V_{DD}$	—	—	V
Low level input voltage	V_{IL}					$0.5V_{SS}$	V
High level output voltage	V_{OH}	$V_{SS} = 2.7 - 5.5V$ $I_{OH} = -0.6mA$	EIO1, EIO2	$V_{DD} - 0.4$	—	—	V
Low level output voltage	V_{OL}	$I_{OL} = 0.6mA$		—	—	0.4	V
Input leak current	I_I	$V_{SS} \leq V_{IN} \leq V_{DD}$	D0-D3, LP, FR XSCL, SHL	—	—	2.0	μA
Input Output leak current	I_{IO}	$V_{SS} \leq V_{IN} \leq V_{DD}$	EIO1, EIO2	—	—	5.0	μA
Rest current	I_{SS}	$V_1 = 28.0 - -14.0V$ $V_{IN} = GND, V_L = GND$	V_{SS}	—	—	25	μA
Output resistance	R_{SO}	$\Delta V_{OH} = 0.5V, T_a = 25^\circ C$ $V_1 = -20.0V, V_2 = 13/15 V_1$ $V_2 = 2/15 V_1, V_0 = V_{DD}$	O 0 - O 79		1.2	1.6	K Ω
Average operating current consumption (1)	I_{SA}	$V_{SS} = +5.0V, V_{IN} = V_{DD}$ $V_L = V_{SS}, f_{SCL} = 2.69MHz$ $f_{LP} = 18.8KHz, f_{IN} = 70Hz$ input data: Diced display no-load	V_{SS}	—	0.10	0.2	mA
		$V_{SS} = +3.0V$ Other conditions are the same as with $V_{SS} = -5V$		—	0.7	0.15	
Average operating current consumption (2)	I_b	$V_{SS} = 5.0V, V_0 = 0.0V$ $V_2 = +9.30V, V_5 = -18.6V,$ $V_1 = +28.0V$ Other conditions are the same as with the item I_{SA} .	V_1	—	0.05	0.04	mA
input terminal capacity	C_I	Freq. = 1 MHz $T_a = 25^\circ C$ XSCL, SHL	D0-D3, LP, FR	—	—	8	pF
I/O terminal capacity	C_{IO}	chips proper	EIO1, EIO2	—	—	15	pF

- AC Characteristics
- Input Timing Characteristics



$V_{SS} = -5.0V \pm 0.5V, T_a = -40 \text{ to } 85^\circ\text{C}$

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_L		100	—	ns
XSCL high level pulse duration	t_{WCH}		30	—	ns
XSCL low level pulse duration	t_{WCL}		30	—	ns
Data setup time	t_{DS}		20	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}		40	—	ns
LP high level pulse duration	t_{WLH}	*3	40	—	ns
FR delay allowance	t_{DF}		-900	+900	ns
EIO setup time	t_{SUE}		35	—	ns

$V_{SS} = -4.5V$ to $2.7V$, $T_a = -40$ to $85^\circ C$

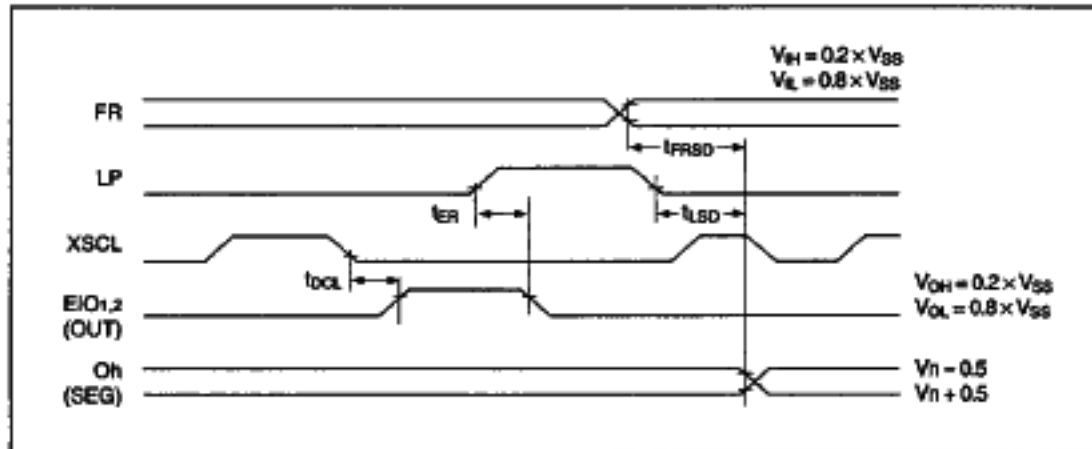
Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_c	$V_{SS} = -2.7V$ *1	153	—	ns
		$V_{SS} = -3.0V$ *2	133		
XSCL high level pulse duration	t_{WH}		50	—	ns
XSCL low level pulse duration	t_{WL}		50	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		15	—	ns
XSCL → LP rise time	t_{LO}		0	—	ns
LP → XSCL fall time	t_{LH}	$V_{SS} = -2.7V$	75	—	ns
		$V_{SS} = -3.0V$	65		
LP high level pulse duration	t_{WLH}	$V_{SS} = -2.7V$ *3	75	—	ns
		$V_{SS} = -3.0V$ *3	65		
FR delay allowance	t_{DF}		-900	+900	ns
EIO setup time	t_{SE}	$V_{SS} = -2.7V$	60	—	ns
		$V_{SS} = -3.0V$	51		

Notes: *1. 6.5MHz equivalence

*2. 7.5MHz equivalence

*3. t_{LH} specifies the time when LP is "H" and, at the same time, XSCL is "L".*4. The input signal t_i is fixed to 20ns.*5. High-speed operation of the shift clocks (XSCL) should only be made under a condition of t_r or $t_f \leq (t_{WL} + t_{WH})/2$

◦ Output Timing Characteristics



$V_{DD} = -5.0 \pm 5\%V$, $V_5 = -12.0$ to $-28.0V$

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{EN}	$C_L = 15$ pf (EIO)	—	90	ns
EIO output delay time	t_{OCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	$C_L = 100$ pf (0 n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

$V_{DD} = -4.5$ to $-2.7V$, $V_5 = -12.0$ to $-28.0V$

Parameter	Symbol	Conditions	Min.	Max.	Units	
EIO reset time	t_{EN}	$C_L = 15$ pf (EIO)	—	150	ns	
EIO output delay time	t_{OCL}		$V_{SS} = -2.7V$	—	88	ns
			$V_{SS} = -3.0V$	—	77	ns
LP → SEG output delay time	t_{LSD}	$C_L = 100$ pf (0 n)	—	400	ns	
FR → SEG output delay time	t_{FRSD}		—	800	ns	

- Notes: *1. The input signal t_r is fixed to 20ns.
 *2. High speed operation of the shift clocks (XSCL) should be made only under a condition of t_r or $t_f \leq (t_{OCL} + t_{LSD})/2$.

■ CONNECTION EXAMPLE

