

FROM 日本電気株式会社 電子デバイス部

1993年 3月26日(金) 20:01 印刷 19:47 文書番号9303090-126 P. 2/15

FROM NESDIS
TO NORTH AMERICA 3rd Dep.

'93. 3.26 13:44
Mihoko Tokuda

4'-9" 01

TOTAL :14

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μ PD35H71

5000-BIT CCD LINEAR IMAGE SENSOR

The μ PD35H71 is a high sensitivity 5000-bit linear image sensor consisting of charge coupled devices (CCD) which changes optical images to electrical signal.

Especially, the μ PD35H71 has extra high speed CCD register, so it is suitable for high resolution scanner and facsimile which scan high definition document at high speed.

FEATURES

- Valid photocell: 5000-bit
- Photocell's pitch: 7 μ m
- High response sensitivity: Providing a response three times better than the existing equivalent NEC product (μ PD3571) to the light from a day light fluorescent lamp
- High resolution: 16 dot/mm across the shorter side of a A3-size (297 x 420 mm) sheet
- 40 MHz high speed scan: 126 μ s/line
- Peak response wavelength: 550 nm (green)
- Power supply: +12 V
- All clock signal input level: CMOS output under 5 V operation

ORDERING INFORMATION

Part Number	Package	Quality Grade
μ PD35H71D	22-pin ceramic DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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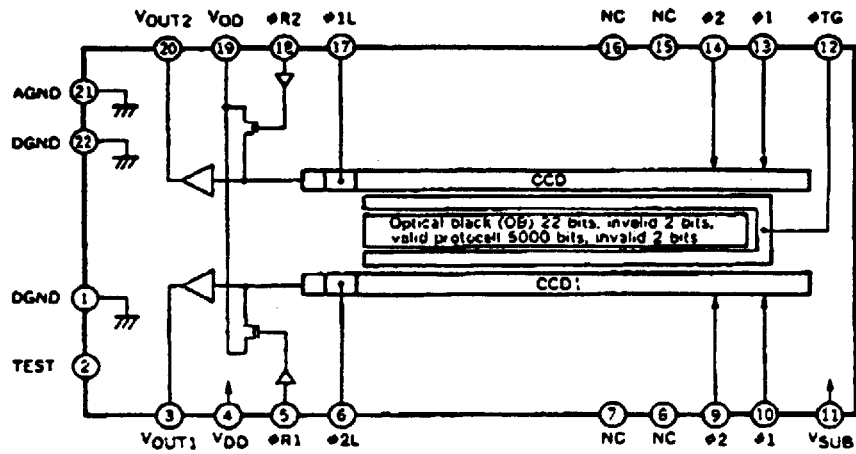
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BLOCK DIAGRAM

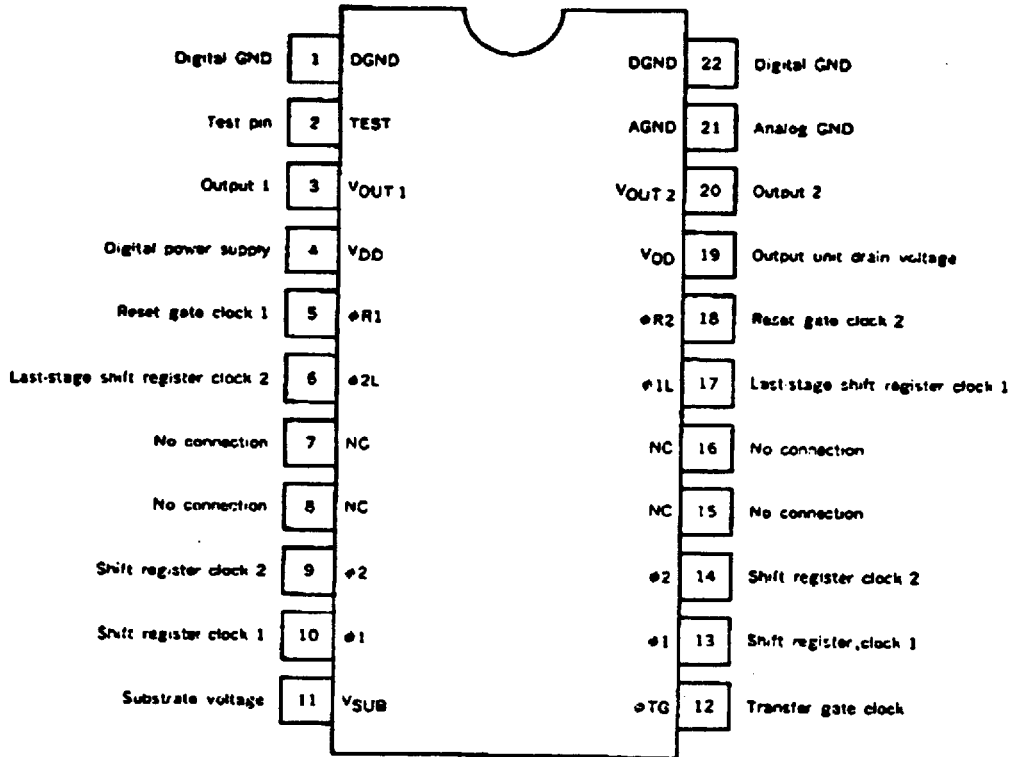


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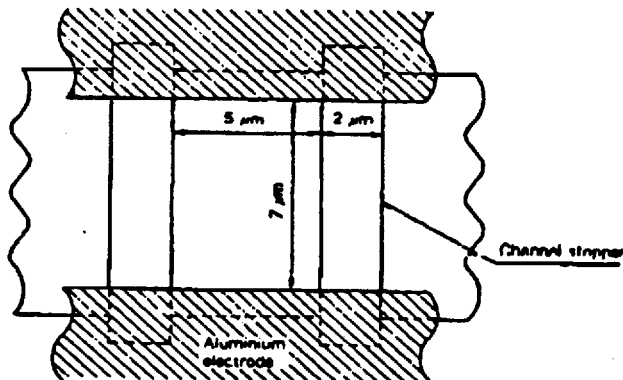
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PIN CONFIGURATION (Top View)



PHOTOCELL STRUCTURE DIAGRAM



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ABSOLUTE MAXIMUM RATINGS ($T_a = +25^\circ\text{C}$)

Parameter	Symbol	Rating	Unit
Output unit drain voltage	V_{DD}	-0.3 to +15	V
Digital power supply	V_{DD}	-0.3 to +15	V
Substrate voltage	V_{SUB}	-0.3 to +15	V
Shift register clock voltage	$V_{\phi 1, \phi 2}$	-0.3 to +15	V
Reset signal voltage	$V_{\phi R}$	-0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	-0.3 to +15	V
Operating ambient temperature	T_{opt}	-25 to +55	$^\circ\text{C}$
Storage temperature	T_{stg}	-40 to +100	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -25$ to $+55^\circ\text{C}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output unit drain voltage	V_{DD}	11.4	12.0	12.6	V
Digital power supply	V_{DD}	11.4	12.0	12.6	V
Substrate voltage	V_{SUB}	11.4	12.0	12.6	V
Shift register clock $\phi 1$, $\phi 1L$ signal high level	$V_{\phi 1H}$	4.5	5.0	5.5	V
Shift register clock $\phi 1$, $\phi 1L$ signal low level	$V_{\phi 1L}$	-0.3	0	0.5	V
Shift register clock $\phi 2$, $\phi 2L$ signal high level	$V_{\phi 2H}$	4.5	5.0	5.5	V
Shift register clock $\phi 2$, $\phi 2L$ signal low level	$V_{\phi 2L}$	-0.3	0	0.5	V
Reset signal $\phi R1$ high level Note	$V_{\phi R1H}$	4.5	5.0	5.5	V
Reset signal $\phi R1$ low level Note	$V_{\phi R1L}$	-0.3	0	0.5	V
Reset signal $\phi R2$ high level Note	$V_{\phi R2H}$	4.5	5.0	5.5	V
Reset signal $\phi R2$ low level Note	$V_{\phi R2L}$	-0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	5.0	5.5	V
Transfer gate signal low level	$V_{\phi TGL}$	-0.3	0	0.5	V
Data rate	$f_{\phi R}$		2	40	MHz

Note Input reset signal $\phi R1$, $\phi R2$ to pin 5, 18 via capacitor. Concerning the connection method refer to APPLICATION CIRCUIT.
 Operating conditions of reset signal $\phi R1$, $\phi R2$ are not the condition at device pins but the condition of the signal which applied to capacitor.
 Leave Test pin (pin 7) unconnected

3d

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ELECTRICAL CHARACTERISTICS

$T_B = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$, $f_{\text{cl}} = 1\text{MHz}$, data rate = 2 MHz, storage time = 10 ms,
 light source = 3200 K halogen lamp +CS00 (infrared cut filter), input signal clock = 5 V_{p-p}

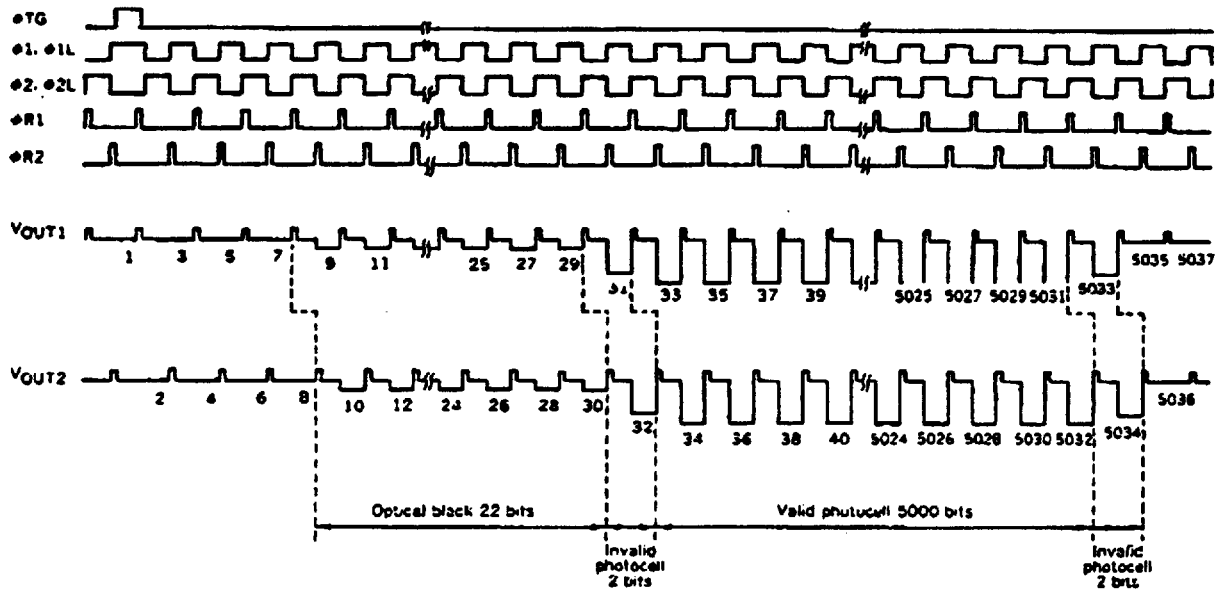
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	VSAT		1.0	1.5		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.29		lx-s
Photo response non-uniformity	PRNU	VOUT = 500 mV		15	±10	%
Average dark signal	ADS	Light shielding		1.0	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	-3	3	+6	mV
Power consumption	PW			200		mW
Output impedance	ZO			0.2	0.5	kΩ
Response	R _F	Daylight color fluorescent lamp	4.15	5.2	6.25	V/lx-s
	R _W	W lamp	-	15.6	-	
Response peak wavelength				550		nm
Image lag	IL	VOUT=1V		2	5	%
Offset level	VOS		2.0	3.0	5.0	V
Shift register clock input capacitance	C _{cl}			500	800	pF
	C _{cl2}					
Last gate clock input capacitance	C _{clL}			50	100	pF
	C _{cl2L}					
Reset input capacitance	C _{clR1}			10	15	pF
	C _{clR2}					
Transfer gate signal input capacitance	C _{clTG}			150	200	pF
Output rise delay time	t _d			20		ns
Register imbalance	RI	VOUT = 500 mV		0	4	%
Transfer efficiency	TTE	VOUT = 500 mV, f _{clR1} = 20 MHz	92	96		%
Dynamic range	DR	VSAT/DSNU		500		times
Reset feed through noise	RFSN			250	500	mV

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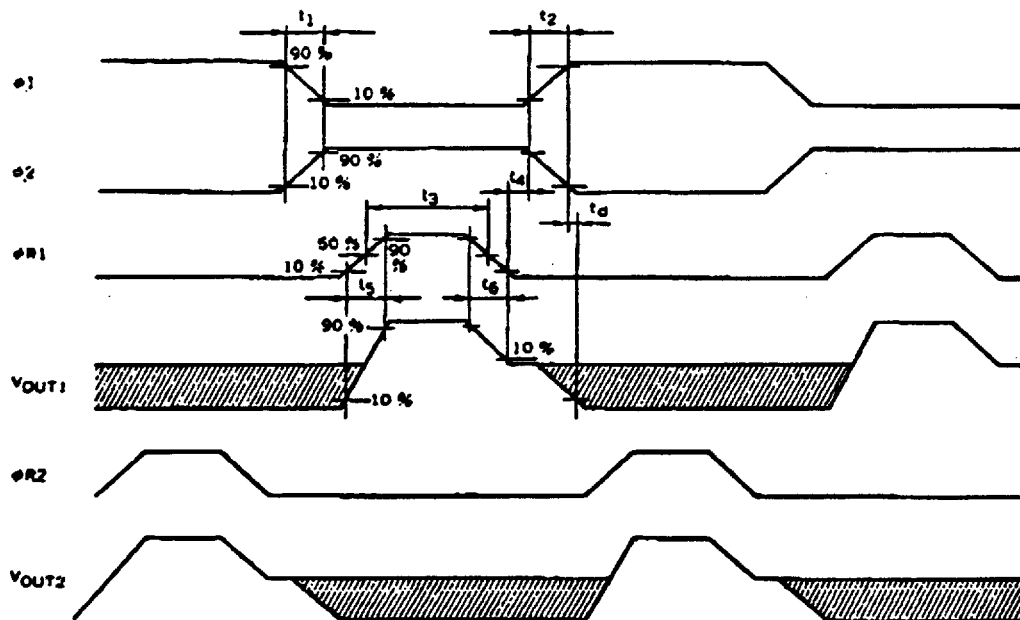
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TIMING CHART 1



TIMING CHART 2



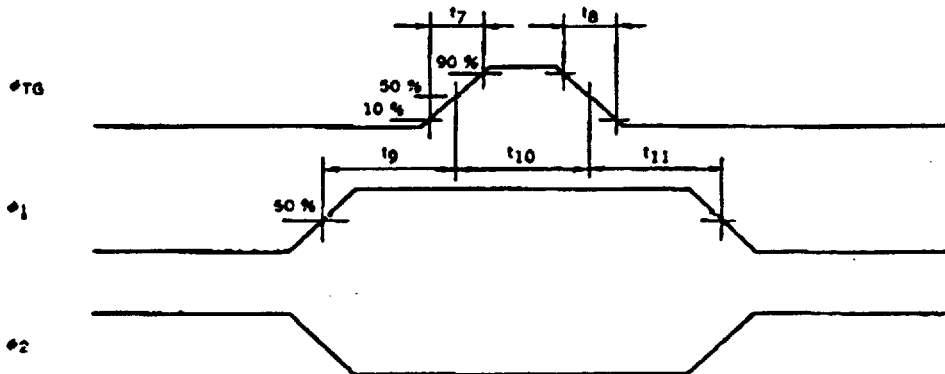
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μPD35H71

TIMING CHART 3



Recommended Timing

[Unit: ns]

Parameter	MIN.	TYP.	MAX.
t1, t2	0	50	200
t3	15	50	500
t4	5	20	500
t5, t6	0	20	50
t7, t8	0	50	100
t9, t11	10	100	500
t10	1000	2000	5000

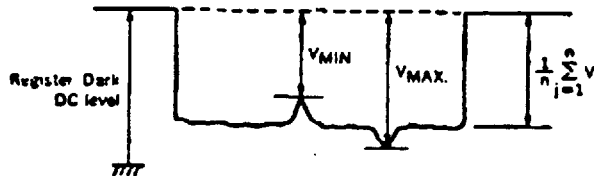
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DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: VSAT
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE
Product of intensity of illumination (lx) and storage time(s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU
The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX. \text{ or } V_{MIN.}} - 1}{\frac{1}{n} \sum_{j=1}^n V_j} \right) \times 100$$

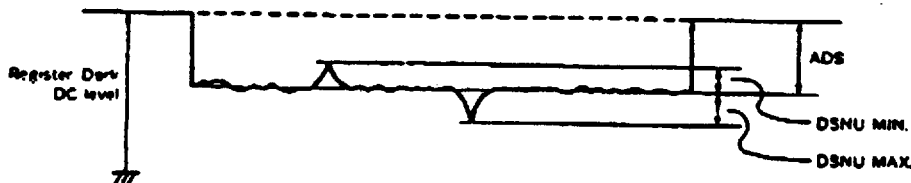
n : Number of valid bits
 V_j : Output voltage of each bit



4. Average dark signal: ADS
Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

5. Dark signal non-uniformity: DSNU
The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: Zo
Output pin impedance viewed from outside.
7. Response: R
Output voltage divided by exposure (lx.s).
Note that the response varies with the light source.

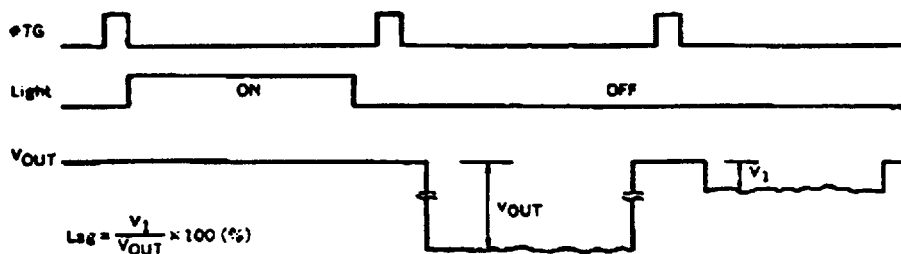
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8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



9. Register Imbalance: RI

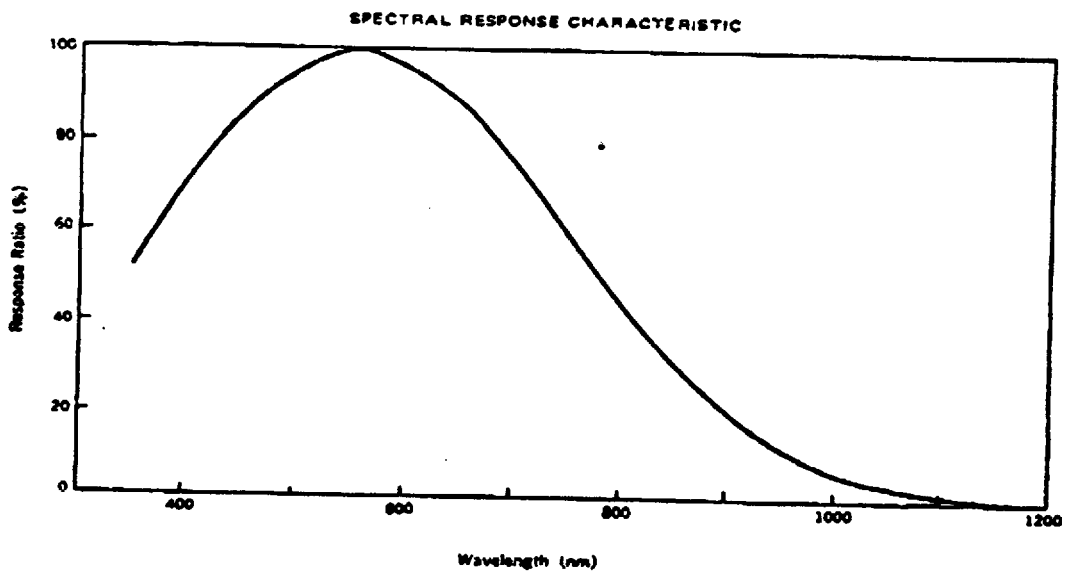
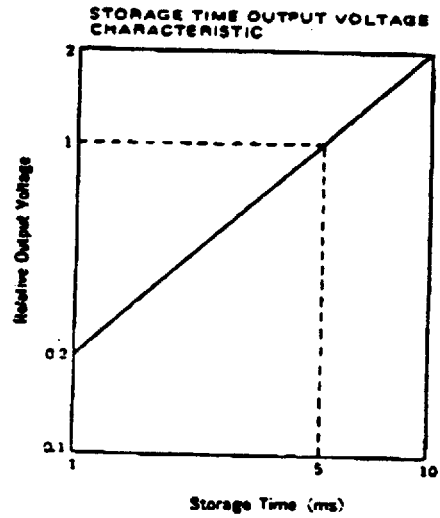
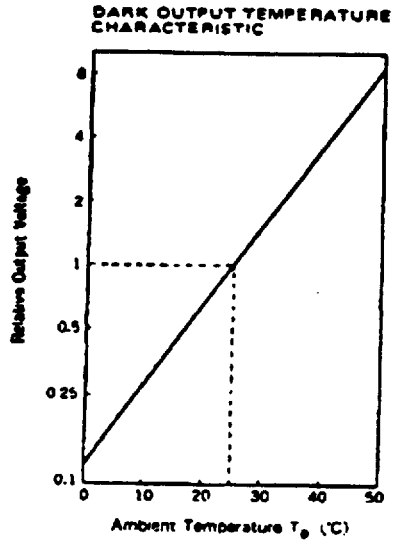
The rate of the average voltage which is the difference between the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

$$RI = \frac{\frac{1}{n} \sum_{j=1}^n |V_j - V_{j+1}|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100 (\%)$$

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STANDARD CHARACTERISTIC CURVES ($T_a = +25^\circ\text{C}$)



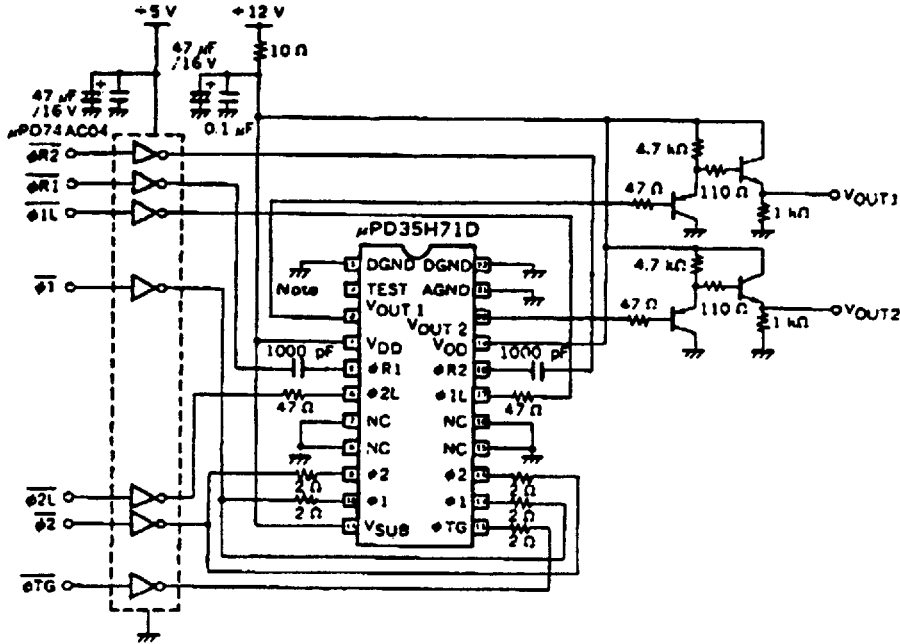
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APPLICATION CIRCUIT



Note Leave this pin unconnected.

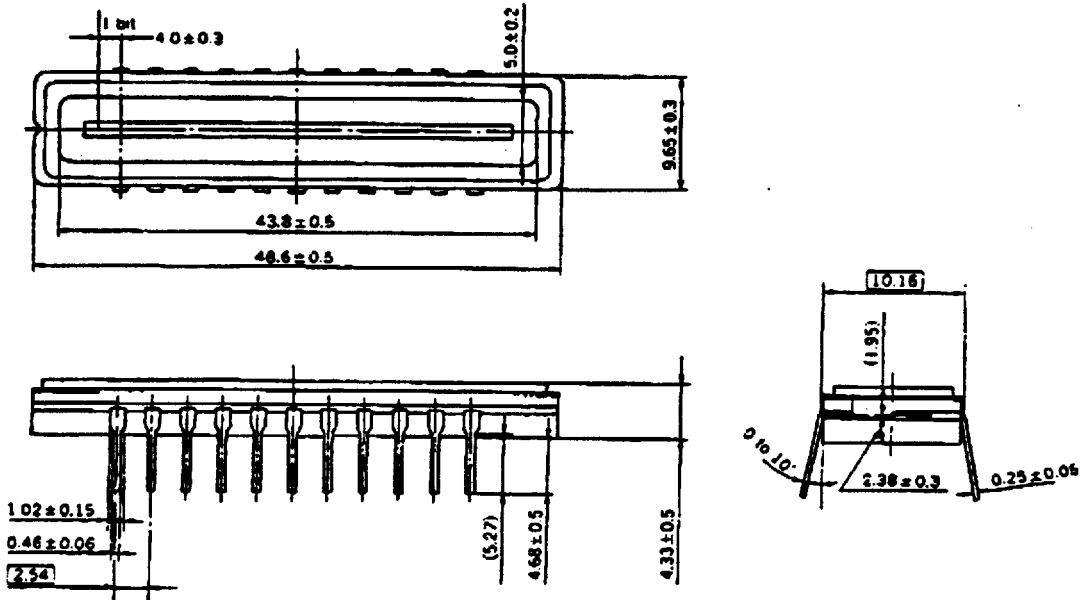
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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PACKAGE DIMENSIONS (Unit: mm)



Name	Dimensions	Refractive index
Glass cap	$475 \times 9.25 \times 0.7$	1.5

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μPD35H71

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TABLE 1 RECOMMENDED SOLDERING CONDITIONS

Part Number	Package	Symbol
μPD35H71D	22-pin ceramic DIP (CERDIP) (400 mil)	Wave soldering (Only lead part)

TABLE 2 SOLDERING CONDITIONS

Symbol	Soldering process	Soldering conditions
Wave soldering>Note (Only lead part)	Wave soldering (Only lead part)	Solder temperature: 260 °C or below. Flow time: 10 seconds or below.

Note This wave soldering should be met to only lead part.
Do not contact jet solder to the package body.

Caution Do not apply more than a single process at once, except for "Partial heating method".

Remark For more details, refer to our document "SMT MANUAL" (IE1-1207).