SYSTEM CAMERA DEVICE

Table of Contents-

1. GENERAL DESCRIPTION

W99688CBM3 is system camera device which built-in 1Mx16bit SDRAM and 128Kbyte Flash ROM. The W99688CBM3 also is a high performance and highly-integrated system camera device that it can preview, capture, compress, store, and display the digital still images or playback a short period of live video.

In addition to transfer image data, the W99688 allows to download the programs of micro controller through the USB to update the external flash program ROM, which allows for end users with firmware upgrades through the Internet.

W99688 supports CMOS image sensors with high performance DSP functions including missing color interpolation, AE (Auto Exposure), AWB (Auto White Balance), Gamma Correction, edge enhancement, contrast stretching, hue and saturation adjusting etc.

W99688 has built-in the baseline JPEG codec for image compression and decompression, which corresponds to the ISO/IEC international standard 10918-1, with YCbCr4:2:2 or YCbCr4:2:0 components in interleaved scan. W99688 also supports the Exchangeable Image File format (EXIF) to ensure data compatibility and exchangeability.

W99688 includes an 8032 compatible CPU core, a 6K-byte SRAM and two 16-bit programmable timers. It also provides the In-System-Programming (ISP) function to let users to update the firmware for external flash ROM.

W99688 also supports a digital display output to directly interface with TFT-LCD, CSTN-LCD or other display device.

2. FEATURES

❑ Sensor Interface

- Direct connect to CMOS image sensor:
  – CMOS Image Sensor:OmniVision, IC-Media , tasc , PixArt and Motorola ……..etc.
- Supports real-time video resolutions up to 640X480 and still image resolutions up to 2048X2048
- High performance Sensor DSP functions (includes black level compensation, color Interpolation, false color suppression, edge enhancement, color correction, gamma correction, AEC, AWB, contrast stretching, hue and saturation adjusting)
- Supports universal serial interface to program CMOS image sensor.

❑ User Interface

- Built-in 8-bits 8032 compatible uC with internal 6K bytes data RAM and 128K bytes Flash ROM
- Supports In-System-Programming (ISP) function for external flash ROM through USB to the internal program flash-ROM
- uC can directly access the frame buffer through bank switching.

❑ Host Interface

- 8/16 bits parallel Bus (Indirect access)

❑ JPEG CODEC for Image Compression and Decompression

- Fully compliant with ISO/IEC 10918-1 international JPEG standard

- JPEG compression and decompression for still images
- Real-time motion JPEG (MJPEG) compression with advanced bit rate control for live video
- JPEG baseline sequential mode in interleaved scan YCbCr4:2:2 or YCbCr4:2:0 format
- Three programmable quantization tables for image/video quality control and bit-rate control.
- Support Exchangeable Image File format (EXIF).

❑ **Display Interface**

- Supports OSD function to display the user interface message on LCD screen
- Supports a digital display output to directly interface with TFT-LCD or other display device, like electric – view finder
- Supports the C-STN LCD which have the MCU interface and display data memory

❑ **Power Management**

- Advanced power management including Power-down, Stand-by, and Operating modes. Engines are only active when they are needed

❑ **Operation Modes**

- Preview ModeFrame rate up to 30 fps
- Single Snapshot Mode
- Burst Snapshot Mode
  - Support up to 10 frames burst snapshot at 1/30 sec interval
- Movie Mode (Motion JPEG)
  - About 15 seconds recording time with 800K bytes vedio buffer at 160x120 size @ 15 fps
- Playback Mode
- Transfer Mode
- Still Image Size
  - 640x480 (VGA)
  - 320x240 (QVGA)
  - 160x120 (QQVGA)
  - Subject to change by request
- Video Clip Size
  - 160x120 (QQVGA)
  - Subject to change by request

❑ **Built-in Two PLL (Phase-Locked Loops) Clock Synthesizers**

❑ **5V Core, 3.3V I/O, 5 V Input Tolerant**

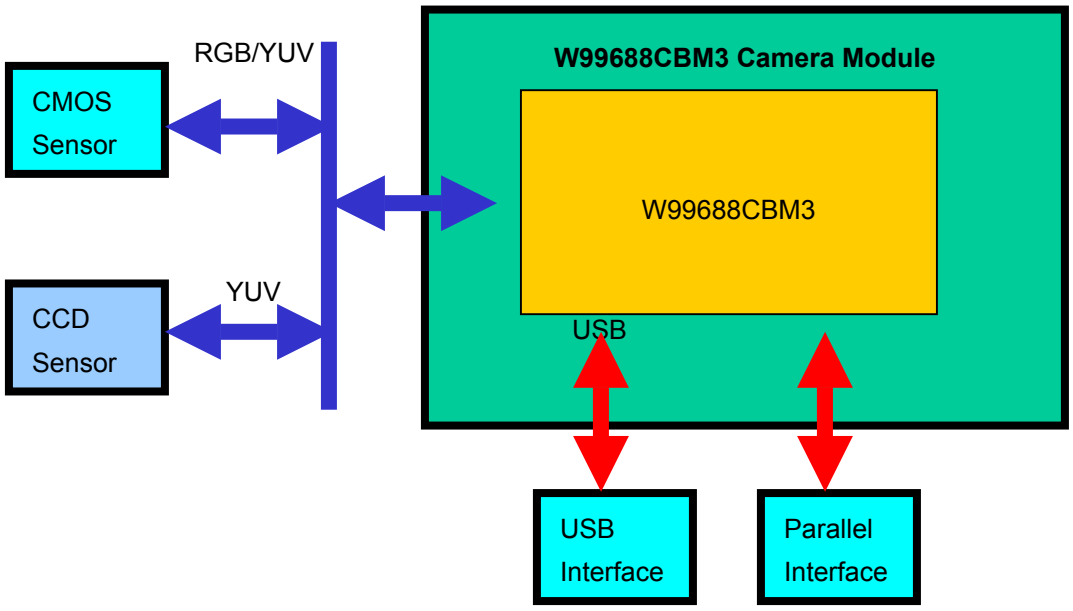
❑ **Built-in 2Mbyte frame buffer and 128Kbyte Flash ROM.**

❑ **Command set: Easy for base band chip(Host) develop Camera function through Command set protocol.**

❑ **Package: 10mmx10mm, 100-balls LFBGA package for fully function**

3. APPLICATION

3.1 System Camera Device



4. PIN DESCRIPTION

4.1 Pin Definition (100 balls, LFBGA Package)

The following signal types are used in these descriptions.

I	Input pin
IS	Input pin with Schmitt trigger
B	Bi-directional input/output pin
BR	Bi-directional input/output pin with repeater
BU	Bi-directional input/output pin with internal pull-up
O	Output pin
A	Analog input/output pin
P	Power supply pin
G	Ground pin
#	Active low

USB Interface (2 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DP	E3	A	Data Plus line of differential USB upstream port. Note: provide an external 1.5 KΩ pull-up resistor at DP so the device indicates to the host that it is a full-speed device.
DM	E2	A	Data Minus line of differential USB upstream port.

POWER ON SETTING (1 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
MD1	L4	BU	ISP mode ON/OFF, Default pull up ISP is off

Sensor or Video Input Interface (17 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SVID[9:0]	F11, F9, K4, G11, G9, G10, H10, H11, J5, D9	I	Sensor or Video Data Input SVID[9:0].
SPCLK	F10	I	Clock for Sensor or Video Data Input
SVS	J4	B	Vertical Sync Input. Programmable polarity.
SHS	K3	B	Horizontal Sync Input. Programmable polarity.
SCLK	E10	O	Clock Output to Sensor
SCK	H4	B	Serial Interface Clock
SDI/SDA	E9	B	Serial Interface Data Input/ Serial Data Acknowledge
SDO/SDE	D9	B	Serial Interface Data Output / Serial Data Enable

LCD Digital Display Interface (13 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DCLK / DFULL	L10	I	Clock Input for Display Controller Reflective Display Module: Full
DDE / DVALID / DA0	J9	O	LCD: Data Enable Reflective Display Module: Data Valid M-LCD: Address-0, for LCD Controller RS signal (CMD/DAT#)
DOCLK / DDCLK / DCS#	K10	O	Clock for Digital Display Data Output Reflective Display Module: Data Clock M-LCD: LCD Chip Select
DHSYNC / DXCLK / DWR#	K11	O	Horizontal Sync Reflective Display Module: Display Clock M-LCD: Write Enable
DVSYNC / FS / DRD#	L11	O	Vertical Sync Reflective Display Module: Frame Start M-LCD: Read Enable
DDATA [7:0]	J8, K9, K8, J7, K7, L8, K5, L9	O	Digital Display Output Data 8 bits

Flash Memory Host Interface (20 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
FWAIT#	J3	BU	Compact Flash: WAIT# Signal
FCD#	K2	BU	Compact Flash: Card Inserted Detect
FRESET	D10	BR	Compact Flash: RESET/RESET# Signal
FSCS0# / FA0	B11	BR	Smart Media: Chip-0 Enable Compact Flash: Address-0
FSCS1# / FA1	D8	BR	*Smart Media: Chip-1 Enable* *Compact Flash: Address-1*
FSCS2# / FA2	A11	BR	Smart Media: Chip-2 Enable Compact Flash: Address-2
FSR/B# / FRDY/BSY# FWP	A10	BU	Smart Media: Ready/Busy Compact Flash: Ready Signal SD: Host to detect card's write protect switch is enable
FSRE# / FIORD#	B10	BU	Smart Media: Read Enable Compact Flash: I/O Read Strobe

Flash Memory Host Interface (20 pins), continued

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
FSWE# / FIOWR# / FCMD	B9	BU	Smart Media: Write Enable Compact Flash: I/O Write Strobe SD: Master CMD
FSCLE / FCE2# / XCLK	C8	BR	Smart Media: Command Latch Enable Compact Flash: Chip Select Signal – 2 SD: Slave CLK
FSALE / FCE1# / XCMD	C9	BR	Smart Media: Address Latch Enable Compact Flash: Chip Select Signal – 1 SD: Slave CMD
FSWP# / FREG# / FCLK	A9	BR	Smart Media: Write Protect Compact Flash: Register (Attribute) Memory *Access* SD: Master CLK
FD [3:0] / FDAT [3:0]	J2, B8, C7, H3	BR	Smart Media & Compact Flash: Data Bus FD[3:0] SD: SD Master DAT [3:0]
FD [7:4] / XDAT [3:0]	D4, B7, C6, A8	BR	Smart Media & Compact Flash: Data Bus FD[7:4] XD: SD Slave DAT [3:0]

Compact Flash-IDE lite "Device" Interface (20 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
XWAIT#	J3	BU	Compact Flash: WAIT Signal
XCD# POR	K2	BU	Compact Flash: Card Insert Detect (A Low level signal Output) SD: Power-On Reset (Implement For No Powered Device)
XRESET	D10	BR	Compact Flash: Card Reset
XA[2: 0]	A11, D8, B11	BR	Compact Flash: Address [2:0]
XRDY / XBSY#	A10	BU	Compact Flash: Ready Signal
XIORD#	B10	BU	Compact Flash: I/O Read Strobe
XIOWR#	B9	BU	Compact Flash: I/O Write Strobe
XCE[2: 1]# XCS[1: 0]#	C8, C9	BR	Compact Flash: Card Enable [2:1] Compact Flash: IDE Mode, Chip Select [1:0]
XREG#	A9	BR	Compact Flash: Register (Attribute) Memory Access Select
XD[7:0]	D4, B7,C6, A8, J2, B8, C7, H3	BR	Compact Flash: Data Bus 16 Bits

GPIO and Miscellaneous (21pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
GPIO[0] / PCLK-A	B6	BU	General Purpose I/O [0] PCLK-A Output
GPIO[1] / PCLK-B	A5	BU	General Purpose I/O [1] PCLK-B Output
GPIO[3]	L6	BU	General Purpose I/O [3]
GPIO[10] / HCLK / XCLK	C3	BU	General Purpose I/O [10] HCLK for SD 2nd Host Interface Alternate Slave SD Device CLK signal
GPIO[11] / HCMD / XCMD	A1	BU	General Purpose I/O [11] HCMD for SD 2nd Host Interface Alternate Slave SD Device CMD signal
GPIO[15:12] / HDAT[3:0] / XDAT[3:0]	B1, C2, B2, D3	BU	General Purpose I/O [15:12] HDAT[3:0] for SD 2nd Host Interface Alternate Slave SD Device XD[3:0]
XIN	C4	I	Reference frequency input from ext. crystal or a clock source.
XOUT	A6	O	Oscillator output to a crystal. This pin is left unconnected if an external clock source is employed.
RST	B3	IS	Reset In. This pin is active high to reset W99688 chip.

Power and Ground (33 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VDDB	D11, J6, L2, J1, G2, C1, A3, A7, C10	P	I/O Pad Buffer Power Supply. Provide isolated power to the I/O buffers for improved noise immunity. +3.3V ±0.3V.
VSSB (GND)	E11, J10, L7, L3, L1, H1, D2, A2, C5, C11	G	I/O Pad Buffer Ground.
VDDI	J11, L5, G1	P	Internal Core Logic Power Supply. +2.5V ± 0.25V.
VSSI	H8, K1, K2	G	Internal Core Logic Ground.
AVDDP	B4	P	PLL Power Supply. +2.5V ±0.25V.
AVSSP	A4	G	PLL Ground.
USBVDD	E1	P	USB Power Supply. +3.3V ±0.3V.
USBVSS	D1	G	USB Ground.
GND-D	F3	G	Embedded SDRAM Ground-1.
VD33-D	G3	P	Embedded SDRAM Power Supply-1. +3.3V ±0.3V.
GND-F	B5	G	Embedded Flash ROM Ground.
VD33-F	K6	P	Embedded Flash ROM Power Supply. +3.3V ±0.3V.

4.2 Pin Assignment – Top View

A1 CORNER

	1	2	3	4	5	6	7	8	9	10	11
A	GPIO11 /SPI_ CMD	GND-3	VD33-3	AVSSP	GPIO1	XOUT	VD33-2	FD4	FREG#	FIRQ /FRB#	FA2
B	GPIO15 /DAT3 /SPI_ CS#	GPIO13 /DAT1	RESET	AVDDP	GND-F	GPIO0	FD6	FD2	FIOWR#	FIORD#	FA0
C	VD33-4	GPIO14 /DAT2	GPIO10 /SPI_ CLK	XIN	GND-2	FD5	FD1	FCE2#	FCE1#	VD33-1	GND-1
D	USBVSS	GND-4	GPIO12 /DAT0 /GPIO2	FD7				FA1	SDO	FRST	VD33-9
E	USBVDD	DM	DP						SDA	SCLK	GND-10
F	P31	P30	GND-D						SD8	SPCLK	SD9
G	VD25-1	VD33-5	VD33-D						SD5	SD4	SD6
H	GND-5	GND25-1	FD0	SCK				GND25-3	SD0	SD3	SD2
J	VD33-6	FD3	FWAIT#	SVS	SD1	VD33-8	DD4	DD7	DVALID	GND-9	VD25-3
K	GND25-2	FCD#	SHS	SD7	DD1	VD33-F	DD3	DD5	DD6	DOCLK	DHS
L	GND-6	VD33-7	GND-7	MD1	VD25-2	GPIO3	GND-8	DD2	DD0	DFULL	DVS

4.3 Power-On Reset Initialization

During power-on reset, the states of MD[15:0]] are latched into the W99688′s internal configuration registers (CR0000 and CR0001) as device configuration information. Since each pin of MD[15:0] has internally pulled-up. If the application needs to set the configuration to “0”, some proper pull-down resistors must be added into some pins of MD[15:0]. Table 4.2 describes the power-on reset configuration definitions.

Power-on Reset Configuration Definitions

PINS	VALUE	DEFINITION	CONT’L REG
MD1	0	Disable internal 4KB ROM (EA# = 0)	CR0000_1
	1	Enable internal 4KB ROM (EA# = 1)	

5. SYSTEM OVERVIEW

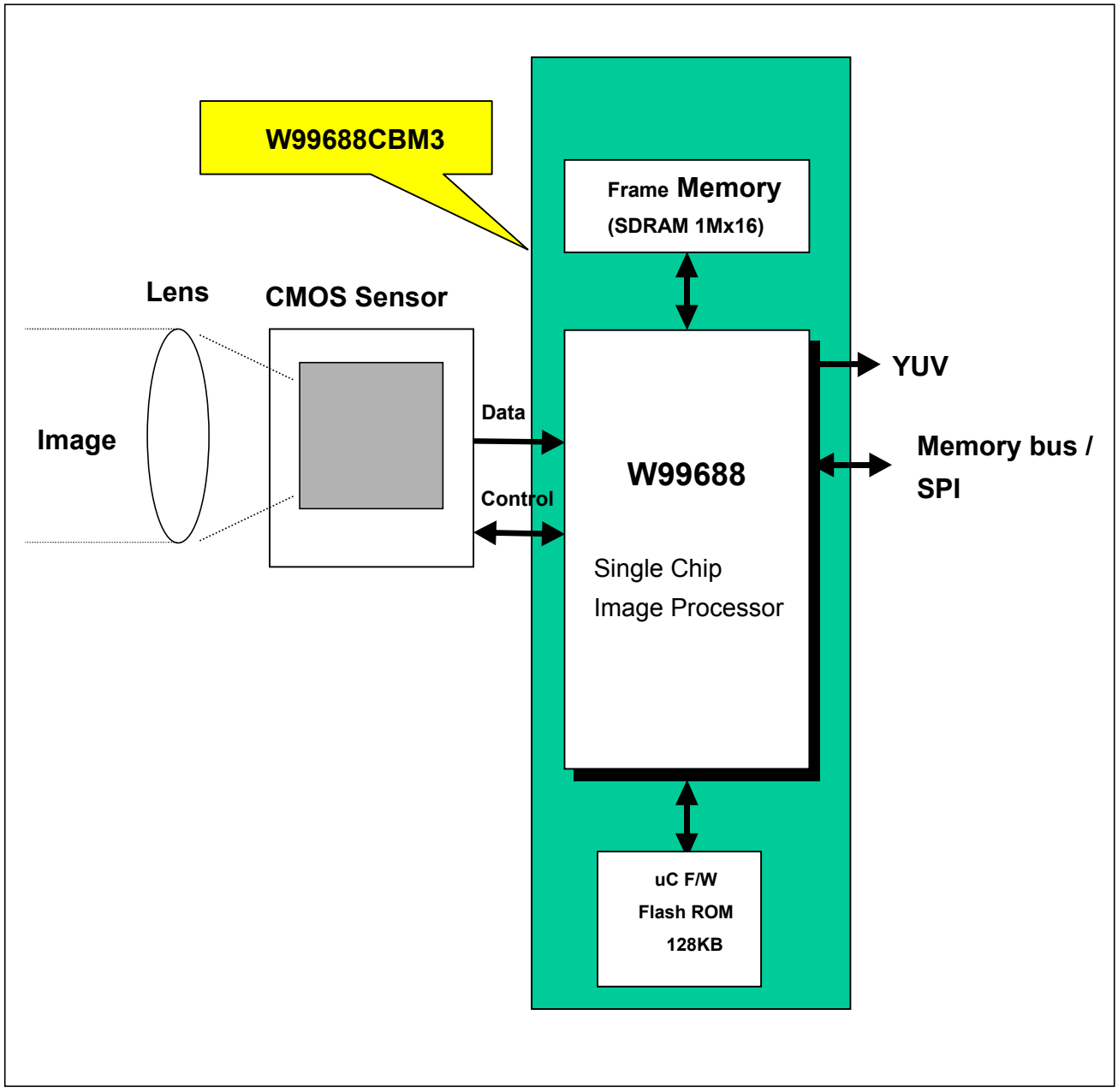


Figure 5.1 W99688 Based DSC System Diagram

5.1 Operation Modes

The W99688 provides seven operation modes:

- *Preview Mode* Real-time capture and display the images (video) on the LCD (W99688 Only).
- *Record Mode* Capture/compress/store a still image (or video) on flash memory or SDRAM
- *Playback Mode* Restore/decompress/display the stored images (single-image or thumbnails) on the LCD.
- *Power Down* System enters power down mode to reduce the power consumption. It can be waked up from power down mode by reset or INT1_ event.

5.2 Address Mapping

INDEX	µC ADDRESS	DESCRIPTION
1	0000H – 7FFFH	Mapping to Frame Buffer SDRAM or SRAM
1	8000H – 97FFH	6KBytes Data RAM
1	A000H – A20FH	528Bytes Flash Memory Buffer-1
1	A400H – A60FH	528Bytes Flash Memory Buffer-2
2	B000H – B6FFH	Control and Status Registers

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient temperature	0	70	°C
Storage temperature	-40	125	°C
DC supply voltage (2.5V)	0	3.5	V
DC supply voltage (3.3V)	0	4.6	V
I/O pin voltage with respect to VSS	– 0.3	5.25	V

Table 6- 1

6.2 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
VDDB	Power Supply for I/O Pads		3.0	3.6	V
USBVDD	POWER SUPPLY FOR USB TRANSCEIVER		3.0	3.6	V
DACVDDB	Power Supply for DAC Output		3.0	3.6	V
DACVDDYC	Power Supply for DAC Output		3.0	3.6	V
DACVDDI	Power Supply for DAC Internal Circuit		2.25	2.75	V
AVDDP	Power Supply for PLL Analog		2.25	2.75	V
VDDI	Power Supply for Core		2.25	2.75	V
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	5.25	V
V_{OL}	Output Low Voltage	I_{OUT} = 2 mA		VSS +0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -2 mA	2.4		V
I_{IL}	Input Low Leakage Current	V_{IN} = 0.4V		10	μA
I_{IH}	Input High Leakage Current	V_{IN} = 2.4V		-10	μA
I_{UP}	Pull-up Current	V_{IN} = 0V		-500	μA
I_{PD}	Power Down Current			TBD	μA
I_{DD}	Active Current			TBD	mA

Table 6- 2

6.3 DAC DC Characteristics

PARAMETER	MIN.	TYP.	MAX.	UNIT
Integral Linearity Error		0.5	±2	LSB
Differential Linearity Error		0.5	±1	LSB
Gray Scale Error			TBD	%Gray
LSB Size		33.28		μA
DAC-to-DAC Matching		2	5	%
Output Compliance	0	1.278		V
Gray Scale Current Range	2.0	34.08		mA
Output Impedance		TBD		Ω
Output Capacitance (f = 1 MHz; I_{OUT} = 0 mA)			TBD	pF
Monotonicity				Guaranteed
Internal V_{REF}	1.230	1.265	1.272	V
Power Supply Reject Ratio (f = 1 KHz)			TBD	%

Table 6- 3

Note 1. Measured with VREF = 1.235 V, RSET = 386 Ω. RL = 37.5 Ω.

6.4 AC Characteristics

6.4.1 USB Transceiver AC Characteristics

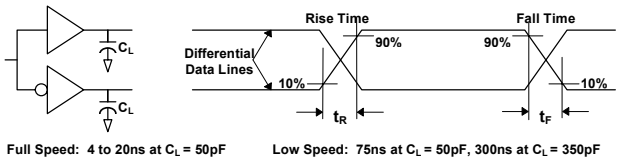


Figure 6.1 Data Signal Rise and Fall Time

USB Transceiver AC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_R	Rise Time	CL = 50 pF	4	20	nS
T_F	Fall Time	CL = 50 pF	4	20	nS
T_{RFM}	Rise/Fall Time Matching		90	110	%
T_{DRATE}	Full Speed Data Rate	Average bit rate (12 Mb/s ±0.25%)	11.97	12.03	Mbps
	Source Differential Driver Jitter				
T_{DJ1}	To Next Transition		-3.5	3.5	nS
T_{DJ2}	For Paired Transitions		-4.0	4.0	nS
T_{EOPT}	Source EOP Width		160	175	nS
T_{DEOP}	Differential to EOP Transition Skew		-2	5	nS
	Receiver Data Jitter Tolerance				
T_{JR1}	To Next Transition		-18.5	18.5	nS
T_{JR2}	For Paired Transitions		-9	9	nS
	EOP Width at Receiver				
T_{EOPR1}	Must Reject as EOP		40		nS
T_{EOPR2}	Must Accept as EOP		82		nS

Table 6.4

6.4.2 RESET Timing AC Characteristics

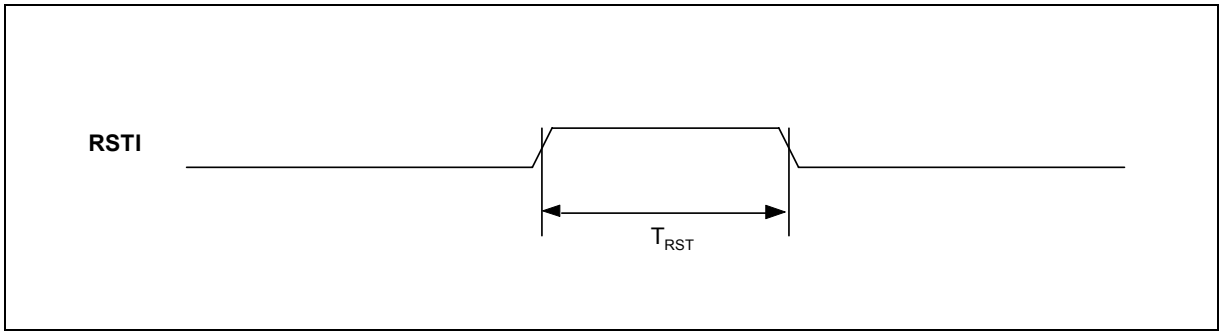


Figure 6.2 RESET Timing

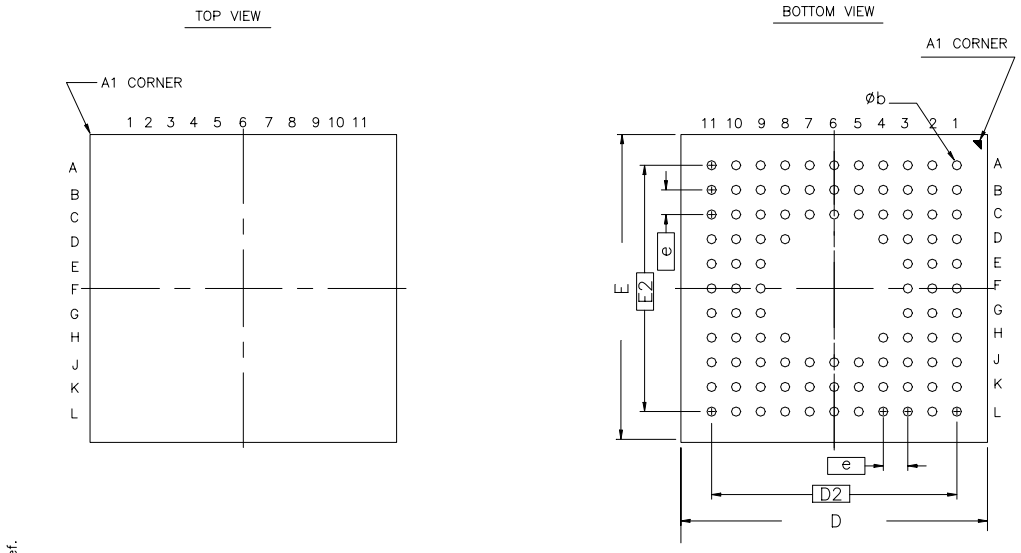
RESET Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{RST}	Reset Pulse Width		100	-	nS

Table 6.5

7. PACKAGE DIMENSION

100L LFBGA (10x10 mm, Ball pitch: 0.8 mm, Ø = 0.4 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.27	–	0.37	0.011	–	0.015
D	9.95	10.00	10.05	0.392	0.394	0.396
D2	8.00 BASIC			0.315 BASIC		
E	9.95	10.00	10.05	0.392	0.394	0.396
E2	8.00 BASIC			0.315 BASIC		
y	0.12 BASIC			0.005 BASIC		
øb	0.37	–	0.47	0.015	–	0.019
e	0.80 BASIC			0.032 BASIC		

8. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 17, 2003	-	Initial Issue

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