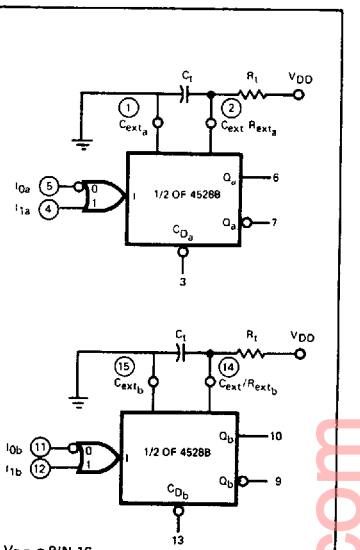
GD4528B
DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

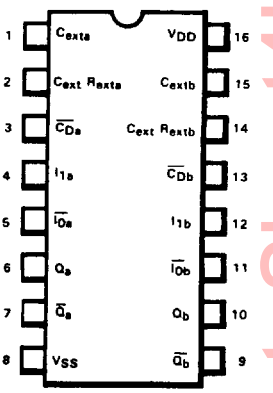
DESCRIPTION — The 4528B is a Dual Retriggerable Resettable Monostable Multivibrator. Each Multivibrator has an active LOW Input ($\overline{I_0}$), an active HIGH Input (I_1), an active LOW Clear Direct Input ($\overline{C_D}$), an Output (Q), its Complement ($\overline{Q}$) and two pins for connecting the external timing components (C_{ext}, C_{ext}/R_{ext}). An external timing capacitor must be connected between C_{ext} and C_{ext}/R_{ext} and an external resistor must be connected between C_{ext}/R_{ext} and V_{DD}.

A HIGH-to-LOW transition on the $\overline{I_0}$ Input when the I_1 Input is LOW or a LOW-to-HIGH transition on the I_1 Input when the $\overline{I_0}$ Input is HIGH produces a positive pulse (L → H → L) on the Q Output and a negative pulse (H → L → H) on the $\overline{Q}$ Output if the Clear Direct Input ($\overline{C_D}$) is HIGH. A LOW on the Clear Direct Input ($\overline{C_D}$) forces the Q Output LOW, the $\overline{Q}$ Output HIGH and inhibits any further pulses until the Clear Direct Input ($\overline{C_D}$) is HIGH.

- **RECOMMENDED OPERATING VOLTAGE, V_{DD} = 4.5 TO 15 V**
- **TYPICAL OUTPUT PULSE WIDTH VARIATION ± 3% AT V_{DD} = 15 V FROM DEVICE TO DEVICE**
- **TYPICAL OUTPUT PULSE WIDTH STABILITY ± 1% OVER -40°C TO +85°C TEMPERATURE RANGE AT V_{DD} = 10 V**
- **TYPICAL OUTPUT PULSE WIDTH STABILITY ± 1% AT V_{DD} = 10 V ±0.25 V RESETTABLE**
- **TRIGGER ON EITHER A HIGH-TO-LOW TRANSITION ON $\overline{I_0}$ OR A LOW-TO-HIGH TRANSITION ON I_1**
- **COMPLEMENTARY OUTPUTS AVAILABLE**
- **BROAD TIMING RESISTOR RANGE, 5 kΩ TO 2 MΩ**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE WITH A WIDE 26 ns TO ∞ RANGE**



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

$\overline{I_{0a}}$, $\overline{I_{0b}}$	Input (H→L Triggered)
I_{1a}, I_{1b}	Input (L→H Triggered)
$\overline{C_{Da}}$, $\overline{C_{Db}}$	Clear Direct (Active LOW) Input
Q_a, Q_b	Output
$\overline{Q_a}$, $\overline{Q_b}$	Complimentary (Active LOW) Output
C_{exta}, C_{extb}	External Capacitor Connections
C_{ext}/R_{exta}, C_{ext}/R_{extb}	External Capacitor/Resistor Connections

TRUTH TABLE

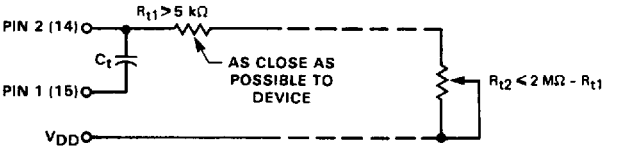
$\overline{I_0}$	I_1	$\overline{C_D}$	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Level
L = LOW Level
H→L = HIGH-to-LOW Transition
L→H = LOW-to-HIGH Transition
X = Don't Care

OPERATING RULES

Timing

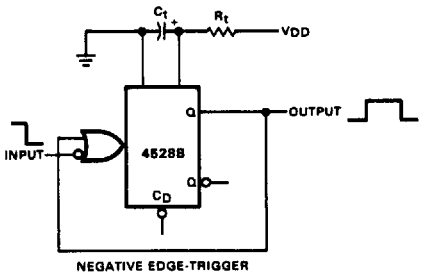
1. An external resistor (R_t) and external capacitor (C_t) are required as shown in the Logic Diagram. The value of R_t may vary from 5 kΩ to 2 MΩ.
2. The value of C_t may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{DD}/R_t the timing diagrams may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 2 (14) and the (-) terminal to pin 1 (15). Pin 2 (14) will remain positive with respect to pin 1 (15).
4. The output pulse width can be determined from the pulse width versus C_t or R_t graphs (Figures 1 and 2).
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



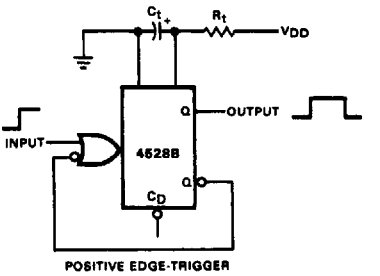
6. Under any operating condition, C_t and R_t (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. V_{DD} and ground wiring should conform to good high frequency standards so that switching transients on V_{DD} and ground pins do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{DD} and ground located near the 4528B is recommended.
8. To minimize noise problems, it is recommended that pin 1 and pin 15 be tied externally to V_{SS}.

Triggering

1. The minimum negative pulse width into $\overline{I_0}$ is 32 ns at V_{DD} = 10 V and the minimum positive pulse width into I_1 is 32 ns at V_{DD} = 10 V.
2. When non-retriggerable operation is required, *i.e.*, when input triggers are to be ignored during a quasi-stable state, input latching is used to inhibit retriggering. The device does not retrigger if an additional trigger input occurs while the capacitor is discharging in response to the initial trigger input.



NEGATIVE EDGE-TRIGGER



POSITIVE EDGE-TRIGGER

3. An overriding active LOW level Clear Direct ($\overline{C_D}$) is provided on each multivibrator. By applying a LOW to the $\overline{C_D}$, any timing cycle can be terminated or any new cycle inhibited until the LOW Clear Input is removed. Trigger inputs will not produce spikes in the output when the Clear Direct Input is held LOW. A new cycle initiated less than 200 ns after removal of a Clear Direct Input ($\overline{C_D}$) will not have a standard output pulse width.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (see Note 4)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN. 25°C	Cext/Rext = V_{DD} All other inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN. 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{I_0}$ to Q		205	335		90	130		60	104	ns	C_L = 50 pF, R_L = 200 kΩ, Input Transition Times ≤ 20 ns; R_t = 5 kΩ to 2 MΩ Any C_t
	Propagation Delay, $\overline{I_0}$ to $\overline{Q}$		205	335		90	130		60	104		
t_{PLH} t_{PHL}	Propagation Delay, I_1 to Q		205	335		90	130		60	104	ns	
	Propagation Delay, I_1 to $\overline{Q}$		205	335		90	130		60	104		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{C_D}$ to Q		145	230		60	85		40	68	ns	
	Propagation Delay, $\overline{C_D}$ to $\overline{Q}$		145	230		60	85		40	68		
t_{TLH} t_{THL}	Output Transition Time		70	135		32	70		22	45	ns	
			70	135		32	70		22	45		
t_{rec}	$\overline{C_D}$ Recovery Time (Note 1)	−50	−90		−20	−37		0	−25		ns	
$t_w\overline{Q}$	$\overline{I_0}$ Minimum Pulse Width (LOW)	70	45		32	24		26	20		ns	
t_wI_1	I_1 Minimum Pulse Width (HIGH)	70	45		32	24		26	20		ns	
$t_w\overline{C_D}$	$\overline{C_D}$ Minimum Pulse Width	65	45		32	26		26	21		ns	
t_wQ	Q Minimum Output Pulse Width		300	500		200	400		150	300	ns	
		R_t = 5 kΩ, C_t = 15 pF										
t_wQ	Q Output Pulse Width	4.35	6.25	8	4	5.3	6.6	4	5	6	μs	
		R_t = 10 kΩ, C_t = 1000 pF										
Δt	Change in Q Output Pulse Width over Temperature		±2	±10		±1	±7		±1	±5	%	
		T_A = −40°C to +85°C										
Δt	Change in Q Output Pulse Width over V_{DD}		±2	±4		±1	±2		±1	±2	%	
		V_{DD} = 5 V ±.25 V			V_{DD} = 10 V ±.25 V			V_{DD} = 15 V ± 25 V				
t_s	Set-Up Time, $\overline{C_D}$ to $\overline{I_0}$ or I_1 (To prevent change in output)	20	5		−25	−45		−25	−35		ns	
R_t	External Timing Resistor Any V_{DD}				5		2000				kΩ	
C_t	External Timing Capacitor	No Limits									μF	

Notes:
1. The 4528B device does not retrigger if an additional trigger input occurs while the capacitor is discharging in response to the initial trigger input.
2. A new cycle initiated less than 200 ns after removal of a Clear Direct Input ($\overline{C_D}$) will not have a standard output pulse width.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. Additional D. C. Characteristics are listed in this section under Goldstar 4000B Series CMOS Family Characteristics.
5. To minimize power dissipation unused multivibrators should have the Cextl Rext Connection tied to VDD, the Cext Connection tied to V_{SS} and all other inputs tied to either V_{DD} or V_{SS}.
6. It is recommended that Input Rise and Fall Times to inputs $\overline{I_0}$ and I_1 be less than 15 μs at V_{DD} = 5V, 4 μs at V_{DD} = 10V and 3 μs at V_{DD} = 15V.

TYPICAL ELECTRICAL CHARACTERISTICS

TYPICAL OUTPUT PULSE WIDTH VERSUS R_t AND C_t

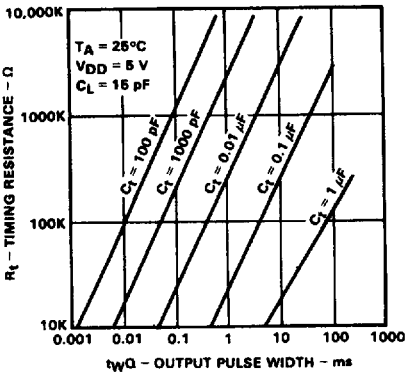


FIGURE 1.

TYPICAL OUTPUT PULSE WIDTH VERSUS R_t AND C_t

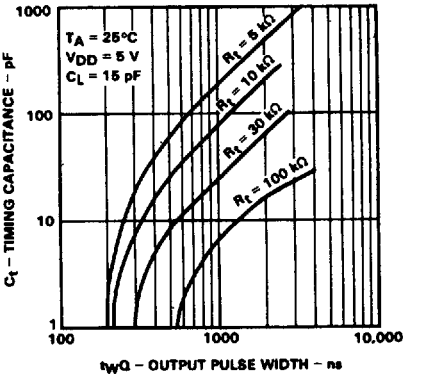
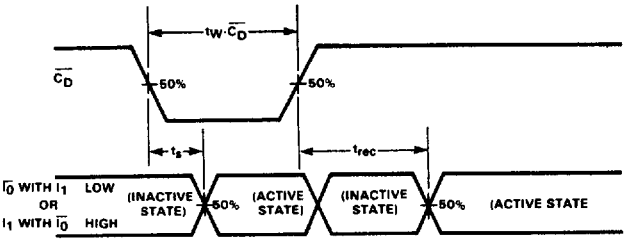
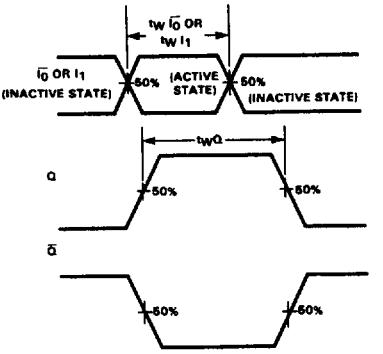


FIGURE 2.

AC WAVEFORMS



Set up Time, $\overline{CD}$ to $\overline{I_0}$ or I_1, Recovery Time for $\overline{CD}$ and Minimum $\overline{CD}$ Pulse Width



Minimum $\overline{I_0}$ or I_1 Pulse Width and Minimum Output Pulse Width

NOTE Set-up Time and Recovery Time are shown as Positive values, but may specified as Negative values

APPLICATIONS

The 4528B Monostable Multivibrator has its pulse width determined by an externally supplied Resistor-Capacitor network. A two step procedure is suggested for determing the proper R_tC_t combination (Equation 1) for a specific pulse width.

The first step is to choose a capacitor. Figure 1 shows pulse width versus resistor value with the capacitor value as the running parameter. A capacitor value is chosen so that the approximate resistor value is between 20 kΩ and 2 MΩ. Once the capacitor is determined, the timing constant (K) is found from Figure 3 for a specific V_{DD}. The resistor value is then determined from Equation 2. If the resistor value is less than 20 kΩ the timing constant should be increased by 20% and the resistor value re-calculated. The resistor must be larger than 5 kΩ.

No upper limit on the capacitor is required. If a large value of R_t and C_t are to be used the timing between pulses or duty cycle, must be sufficiently low that the capacitor fully charges to V_{DD}. Large capacitor values must be sufficiently low in leakage that the resistor value can supply the leakage of the capacitor and still charge the capacitor close to V_{DD}.

EXAMPLE:

Three pulse widths of 0.1, 1, and 10 ms are to be generated with the 4528B using a single capacitor.

From Figure 1 a capacitor value between 0.01 and .1 uF would be reasonable. A 0.022 μF capacitor is the only capacitor that is available.

The timing constant for a 0.022 μF at 10 V V_{DD} is found from Figure 3 to be approximately 0.3.

The resistor values are then calculated:

Pulse Width	R_t
0.1 ms	15.1 kΩ
1 ms	151.1 kΩ
10 ms	1.51 MΩ

The 15.1 kΩ is less than 20 kΩ so add 20% to the K value and recalculate

Pulse Width	R_t	
0.1 ms	12.5 kΩ	K = .36

Equation 1: $P.W. = KR_tC_t$

Equation 2: $P.W. = \frac{R_t}{KC_t}$

P.W.	=	Pulse Width (seconds)
K	=	Timing Constant
C_t	=	Capacitance (Farads)
R_t	=	Resistance (ohms)

TIMING CONSTANT VERSUS TIMING CAPACITANCE

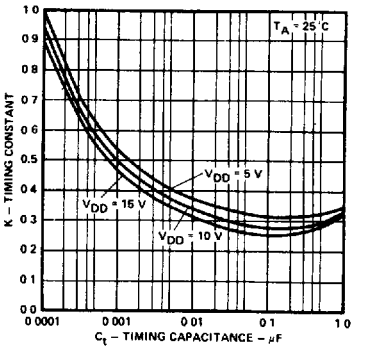


Fig. 3.