19-0666; Rev 0; 10/06

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

General Description

The MAX16818 pulse-width modulation (PWM) LED driver controller provides high-output-current capability in a compact package with a minimum number of external components. The MAX16818 is suitable for use in synchronous and nonsynchronous step-down (buck) topologies, as well as in boost, buck-boost, SEPIC, and Cuk LED drivers. The MAX16818 is the first LED driver controller that enables Maxim's patent-pending technology for fast LED current transients of up to 20A/µs and 30kHz dimming frequency.

This device utilizes average-current-mode control that enables optimal use of MOSFETs with optimal charge and on-resistance characteristics. This results in the minimized need for external heatsinking even when delivering up to 30A of LED current. True differential sensing enables accurate control of the LED current. A wide dimming range is easily implemented to accommodate an external PWM signal. An internal regulator enables operation over a wide input voltage range: 4.75V to 5.5V or 7V to 28V and above with a simple external biasing device. The wide switching frequency range, up to 1.5MHz, allows for the use of small inductors and capacitors.

The MAX16818 features a clock output with 180° phase delay to control a second out-of-phase LED driver to reduce input and output filter capacitors size or to minimize ripple currents. The MAX16818 offers programmable hiccup, overvoltage, and overtemperature protection.

The MAX16818ETI+ is rated for the extended temperature range (-40°C to +85°C) and the MAX16818ATI+ is rated for the automotive temperature range (-40°C to +125°C). This LED driver controller is available in a lead-free, 0.8mm high, 5mm x 5mm 28-pin TQFN package with exposed paddle.

Applications

Front Projectors/Rear Projection TVs

Portable and Pocket Projectors

Automotive, Bus/Truck Exterior Lighting

LCD TVs and Display Backlight

Automotive Emergency Lighting and Signage

Typical Operating Circuit and Pin Configuration located at end of data sheet.

Features

- **High-Current LED Driver Controller IC, Up to 30A Output Current**
- **Average-Current-Mode Control**
- **True-Differential Remote-Sense Input**
- **4.75V to 5.5V or 7V to 28V Input Voltage Range**
- **Programmable Switching Frequency or External Synchronization from 125kHz to 1.5MHz**
- **Clock Output for 180° Out-of-Phase Operation**
- **Integrated 4A Gate Drivers**
- **Output Overvoltage and Hiccup Mode Overcurrent Protection**
- **Thermal Shutdown**
- **Thermally Enhanced 28-Pin Thin QFN Package**
- **-40°C to +125°C Operating Temperature Range**

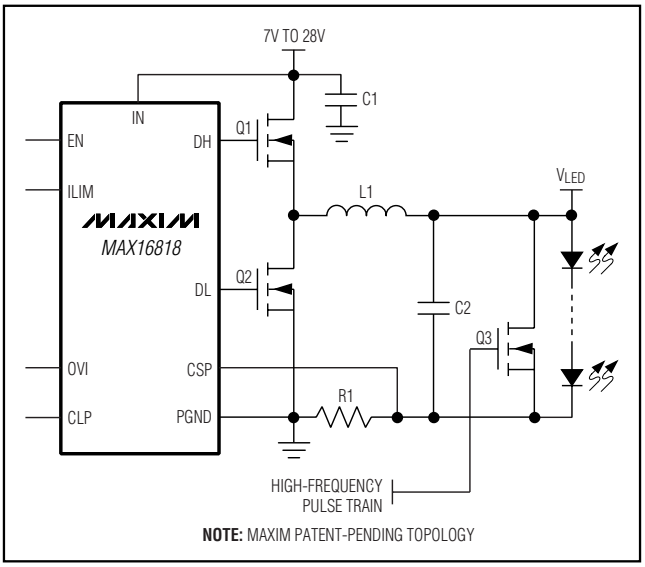
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX16818ATI+	-40°C to +125°C	28 TQFN-EP*	T2855-3
MAX16818ETI+	-40°C to +85°C	28 TQFN-EP*	T2855-3

+Denotes lead-free package.

**EP = Exposed paddle.*

Simplified Diagram



NOTE: MAXIM PATENT-PENDING TOPOLOGY

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

ABSOLUTE MAXIMUM RATINGS

IN to SGND .....-0.3V to +30V
BST to SGND .....-0.3V to +35V
BST to LX .....-0.3V to +6V
DH to LX .....-0.3V to [(V_{BST} - $V_{LX\_}$) + 0.3V]
DL to PGND .....-0.3V to (V_{DD} + 0.3V)
V_{CC} to SGND .....-0.3V to +6V
V_{CC}, V_{DD} to PGND .....-0.3V to +6V
SGND to PGND .....-0.3V to +0.3V
All Other Pins to SGND.....-0.3V to (V_{CC} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range
MAX16818ATI+.....-40°C to +125°C
MAX16818ETI+.....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V_{IN}		7		28	V
		Short IN and V_{CC} together for 5V input operation	4.75		5.50	
Quiescent Supply Current	I_Q	EN = V_{CC} or SGND, not switching		2.7	5.5	mA
LED CURRENT REGULATOR						
SENSE+ to SENSE- Accuracy (Note 2)		No load, V_{IN} = 4.75V to 5.5V, f_{SW} = 500kHz	0.594	0.6	0.606	V
		No load, V_{IN} = 7V to 28V, f_{SW} = 500kHz	0.594	0.6	0.606	
Soft-Start Time	t_{SS}			1024		Clock Cycles
STARTUP/INTERNAL REGULATOR						
V_{CC} Undervoltage Lockout	UVLO	V_{CC} rising	4.1	4.3	4.5	V
V_{CC} Undervoltage Hysteresis				200		mV
V_{CC} Output Voltage		V_{IN} = 7V to 28V, I_{SOURCE} = 0 to 60mA	4.85	5.1	5.30	V
MOSFET DRIVERS						
Output Driver Impedance	R_{ON}	Low or high output, $I_{SOURCE/SINK}$ = 20mA		1.1	3.0	Ω
Output Driver Source/Sink Current	I_{DH},I_{DL}			4		A
Nonoverlap Time	t_{NO}	$C_{DH/DL}$ = 5nF		35		ns
OSCILLATOR						
Switching Frequency Range			125		1500	kHz
Switching Frequency	f_{SW}	R_T = 500kΩ	121	125	129	kHz
Switching Frequency		R_T = 120kΩ	495	521	547	
Switching Frequency		R_T = 39.9kΩ	1515	1620	1725	
Switching Frequency Accuracy		120kΩ ≤ R_T ≤ 500kΩ	-5		+5	%
		40kΩ ≤ R_T ≤ 120kΩ	-8		+8	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLKOUT Phase Shift	ϕ_CLKOUT	With respect to DH, f_{SW} = 125kHz		180		Degrees
CLKOUT Output Low Level	$V_{CLKOUTL}$	I_{SINK} = 2mA			0.4	V
CLKOUT Output High Level	$V_{CLKOUTH}$	I_{SOURCE} = 2mA	4.5			V
SYNC Input-High Pulse Width	t_{SYNC}		200			ns
SYNC Input Clock High Threshold	V_{SYNCH}		2.0			V
SYNC Input Clock Low Threshold	V_{SYNCL}				0.4	V
SYNC Pullup Current	I_{SYNC_OUT}	$V_{RT/SYNC}$ = 0V		250	750	µA
SYNC Power-Off Level	V_{SYNC_OFF}				0.4	V
INDUCTOR CURRENT LIMIT						
Average Current-Limit Threshold	V_{CL}	CSP to CSN	24.0	26.9	28.2	mV
Reverse Current-Limit Threshold	V_{CLR}	CSP to CSN	-3.2	-2.3	-0.1	mV
Cycle-by-Cycle Current Limit		CSP to CSN		60		mV
Cycle-by-Cycle Overload		V_{CSP} to V_{CSN} = 75mV		260		ns
Hiccup Divider Ratio		LIM to V_{CM}, no switching	0.547	0.558	0.565	V/V
Hiccup Reset Delay				200		ms
LIM Input Impedance		LIM to SGND		55.9		kΩ
CURRENT-SENSE AMPLIFIER						
CSP or CSN Input Resistance	R_{CS}			4		kΩ
Common-Mode Range	$V_{CMR(CS)}$	V_{IN} = 7V to 28V	0		5.5	V
Input Offset Voltage	$V_{OS(CS)}$			0.1		mV
Amplifier Gain	$A_{V(CS)}$			34.5		V/V
3dB Bandwidth	f_{3dB}			4		MHz
CURRENT-ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)						
Transconductance	g_m			550		µS
Open-Loop Gain	$A_{VOL(CE)}$	No load		50		dB
DIFFERENTIAL VOLTAGE AMPLIFIER FOR LED CURRENT (DIFF)						
Common-Mode Voltage Range	$V_{CMR(DIFF)}$		0		+1.0	V
DIFF Output Voltage	V_{CM}	V_{SENSE+} = V_{SENSE-} = 0V		0.6		V
Input Offset Voltage	$V_{OS(DIFF)}$		-1		+1	mV
Amplifier Gain	$A_{V(DIFF)}$		0.994	1	1.006	V/V
3dB Bandwidth	f_{3dB}	C_{DIFF} = 20pF		3		MHz
Minimum Output-Current Drive	$I_{OUT(DIFF)}$		4			mA
SENSE+ to SENSE- Input	R_{VS}	V_{SENSE-} = 0V	50	100		kΩ
V_IOUT AMPLIFIER						
Gain-Bandwidth Product		V_{V_IOUT} = 2.0V		4		MHz
3dB Bandwidth		V_{V_IOUT} = 2.0V		1		MHz
Output Sink Current			30			µA
Output Source Current			90			µA

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{DD} = V_{CC}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Load Capacitance				50		pF
V_IOUT Output to I_{OUT} Transfer Function		R_{SENSE} = 1mΩ, 100mV ≤ V_IOUT ≤ 5.5V	132.3	135	137.7	mV/A
Offset Voltage				1		mV
VOLTAGE-ERROR AMPLIFIER (EAOUT)						
Open-Loop Gain	A_{VOLEA}			70		dB
Unity-Gain Bandwidth	f_{GBW}			3		MHz
EAN Input Bias Current	$I_{B(EA)}$	V_{EAN} = 2.0V	-0.2	+0.03	+0.2	µA
Error Amplifier Output Clamping Voltage	$V_{CLAMP(EA)}$	With respect to V_{CM}	883	930	976	mV
POWER-GOOD AND OVERVOLTAGE PROTECTION						
PGOOD Trip Level	V_{UV}	PGOOD goes low when V_{OUT} is below this threshold	87.5	90	92.5	%V_{OUT}
PGOOD Output Low Level	V_{PGLO}	I_{SINK} = 4mA			0.4	V
PGOOD Output Leakage Current	I_{PG}	PGOOD = V_{CC}			1	µA
OVI Trip Threshold	OVP_{TH}	With respect to SGND	1.244	1.276	1.308	V
OVI Input Bias Current	I_{OVI}			0.2		µA
ENABLE INPUT						
EN Input High Voltage	V_{EN}	EN rising	2.437	2.5	2.562	V
EN Input Hysteresis				0.28		V
EN Pullup Current	I_{EN}		13.5	15	16.5	µA
THERMAL SHUTDOWN						
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis				30		°C

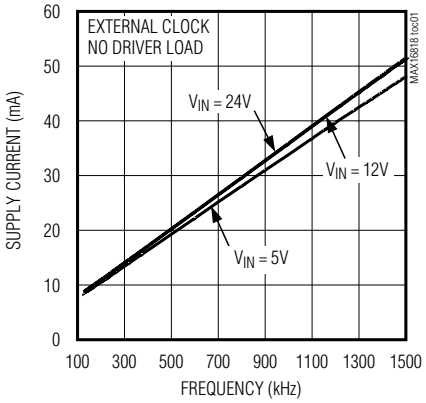
Note 1: Specifications at T_A = +25° are 100% tested. Specifications over the temperature range are guaranteed by design.
Note 2: Does not include an error due to finite error amplifier gain. See the *Voltage-Error Amplifier (EAOUT)* section.

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

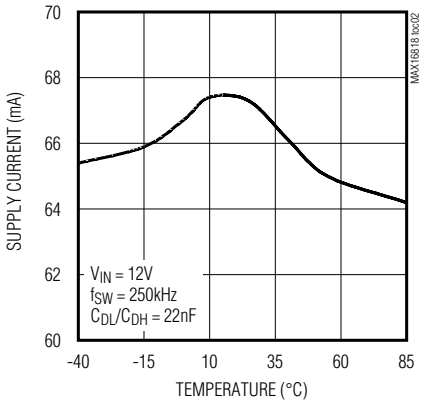
Typical Operating Characteristics

(T_A = +25°C, using Figure 5, unless otherwise noted.)

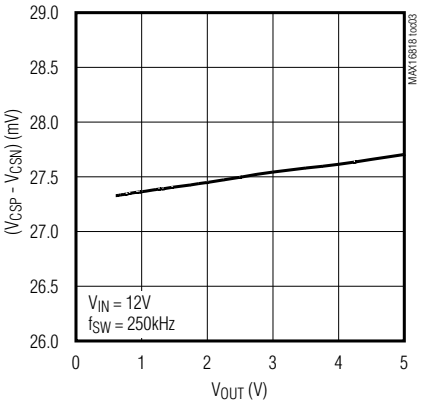
SUPPLY CURRENT (I_Q) vs. FREQUENCY



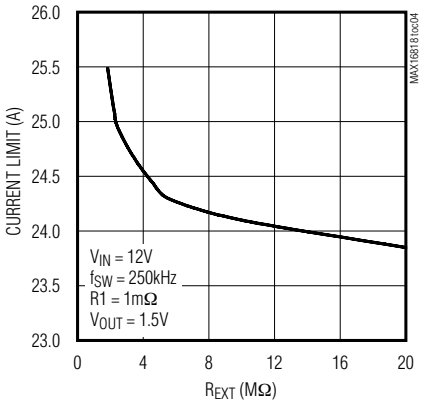
SUPPLY CURRENT vs. TEMPERATURE



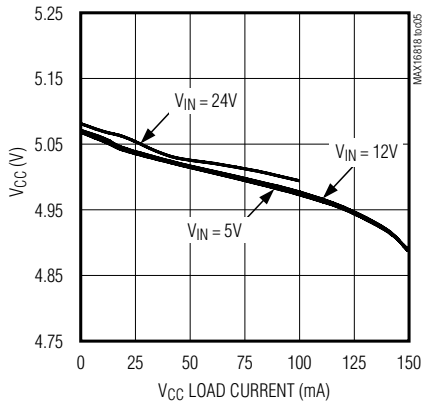
CURRENT-SENSE THRESHOLD vs. OUTPUT VOLTAGE



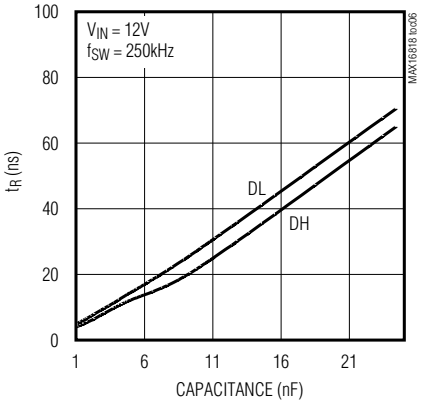
HICCUP CURRENT LIMIT vs. R_{EXT}



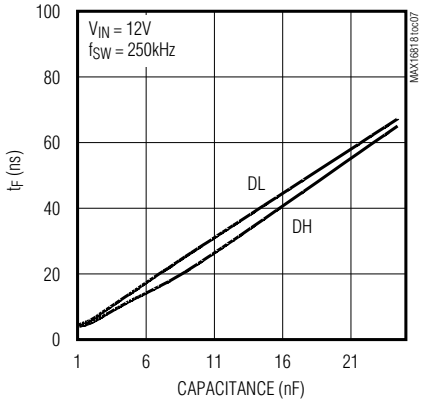
V_{CC} LOAD REGULATION vs. INPUT VOLTAGE



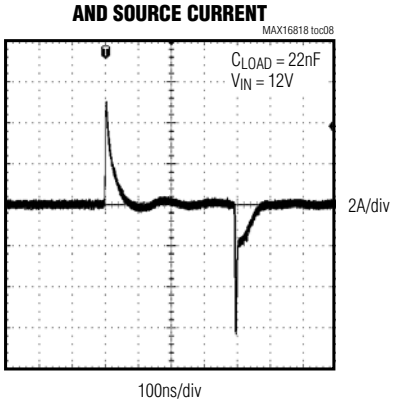
DRIVER RISE TIME vs. DRIVER LOAD CAPACITANCE



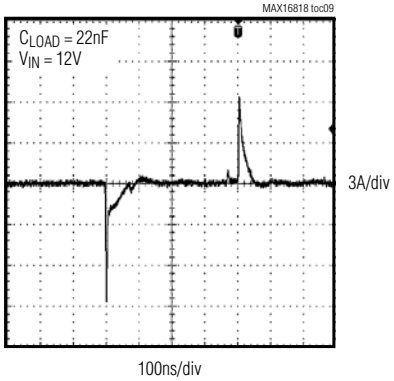
DRIVER FALL TIME vs. DRIVER LOAD CAPACITANCE



HIGH-SIDE DRIVER (DH) SINK AND SOURCE CURRENT



LOW-SIDE DRIVER (DL) SINK AND SOURCE CURRENT

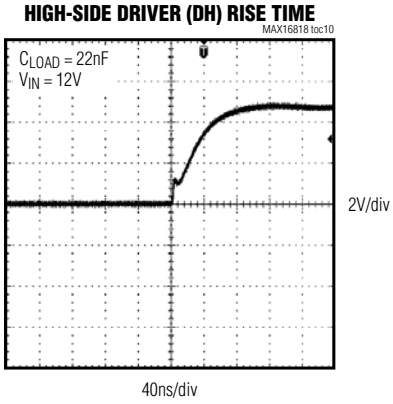


1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

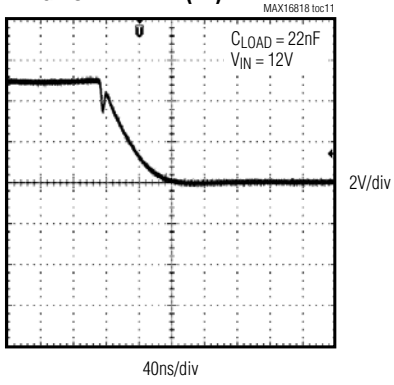
Typical Operating Characteristics (continued)

(T_A = +25°C, using Figure 5, unless otherwise noted.)

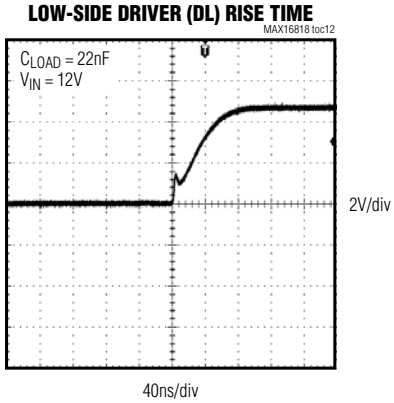
HIGH-SIDE DRIVER (DH) RISE TIME



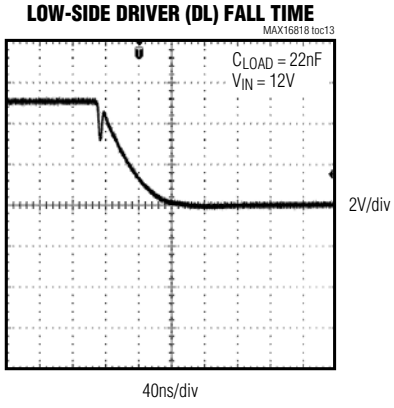
HIGH-SIDE DRIVER (DH) FALL TIME



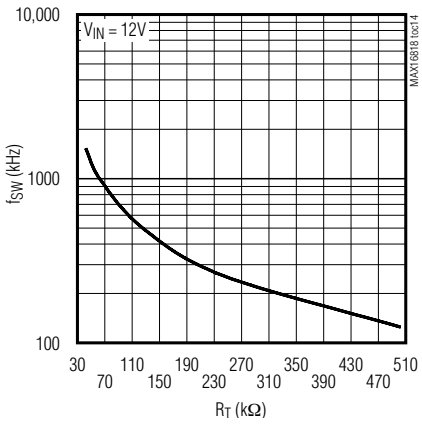
LOW-SIDE DRIVER (DL) RISE TIME



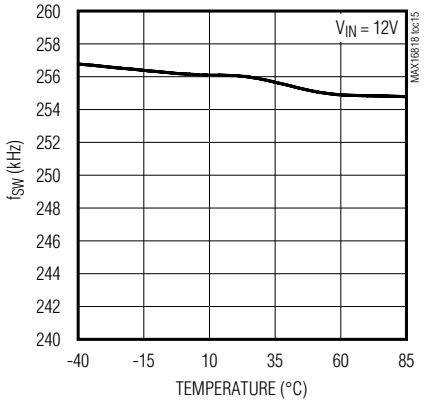
LOW-SIDE DRIVER (DL) FALL TIME



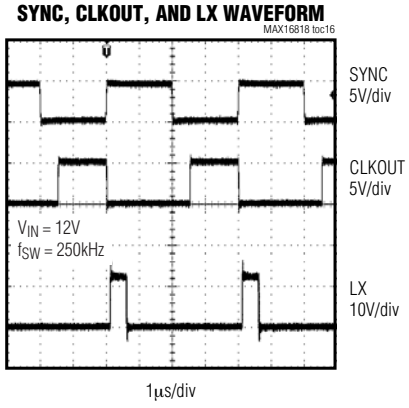
FREQUENCY vs. R_T



FREQUENCY vs. TEMPERATURE



SYNC, CLKOUT, AND LX WAVEFORM



Pin Description

PIN	NAME	FUNCTION
1	PGND	Power-Supply Ground
2, 7	N.C.	No Connection. Not internally connected.
3	DL	Low-Side Gate Driver Output
4	BST	Boost Flying Capacitor Connection. Reservoir capacitor connection for the high-side MOSFET driver supply. Connect a ceramic capacitor between BST and LX.
5	LX	Source connection for the high-side MOSFET.
6	DH	High-Side Gate Driver Output. Drives the gate of the high-side MOSFET.
8, 22, 25	SGND	Signal Ground. Ground connection for the internal control circuitry. Connect SGND and PGND together at one point near the IC.
9	CLKOUT	Oscillator Output. Rising edge of CLKOUT is phase-shifted from the rising edge of DH by 180°.
10	PGOOD	Power-Good Output
11	EN	Output Enable. Drive high or leave unconnected for normal operation. Drive low to shut down the power drivers. EN has an internal 15µA pullup current. Connect a capacitor from EN to SGND to program the hiccup-mode duty cycle.
12	RT/SYNC	Switching Frequency Programming and Chip-Enable Input. Connect a resistor from RT/SYNC to SGND to set the internal oscillator frequency. Drive RT/SYNC to synchronize the switching frequency with external clock.
13	V_IOUT	Voltage Source Output Proportional to the Inductor Current. The voltage at V_IOUT = 135 x I_{LED} x R_S.
14	LIM	Current-Limit Setting Input. Connect a resistor from LIM to SGND to set the hiccup current-limit threshold. Connect a capacitor from LIM to SGND to ignore short output overcurrent pulses.
15	OVI	Overvoltage Protection. Connect OVI to DIFF. When OVI exceeds 12.7% above the programmed output voltage, DH is latched low and DL is latched high. Toggle EN or recycle the input power to reset the latch.
16	CLP	Current-Error Amplifier Output. Compensate the current loop by connecting an RC network to ground.
17	EAOUT	Voltage-Error Amplifier Output. Connect to the external compensation network.
18	EAN	Voltage-Error Amplifier Inverting Input
19	DIFF	Differential Remote-Sense Amplifier Output. DIFF is the output of a precision unity-gain amplifier whose inputs are SENSE+ and SENSE-.
20	CSN	Current-Sense Differential Amplifier Negative Input. The differential voltage between CSN and CSP is amplified internally by the current-sense amplifier (gain = 34.5) to measure the inductor current.

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

Pin Description (continued)

PIN	NAME	FUNCTION
21	CSP	Current-Sense Differential Amplifier Positive Input. The differential voltage between CSN and CSP is amplified internally by the current-sense amplifier (gain = 34.5) to measure the inductor current.
23	SENSE-	Differential LED Current-Sensing Negative Input. SENSE- is used to sense the LED current. Connect SENSE- to the negative side of the LED current-sense resistor.
24	SENSE+	Differential LED Current-Sensing Positive Input. SENSE+ is used to sense the LED current. Connect SENSE+ to the positive side of the LED current-sense resistor.
26	IN	Supply Voltage Connection. Connect IN to V_{CC} for a +5V system.
27	V_{CC}	Internal +5V Regulator Output. V_{CC} is derived from the IN voltage. Bypass V_{CC} to SGND with 4.7µF and 0.1µF ceramic capacitors.
28	V_{DD}	Supply Voltage for Low-Side and High-Side Drivers. Connect a parallel combination of 0.1µF and 1µF ceramic capacitors to PGND and a 1Ω resistor to V_{CC} to filter out the high peak currents of the driver from internal circuitry.
—	EP	Exposed Paddle. Connect the exposed paddle to a copper pad (SGND) to improve power dissipation.

Typical Application Circuits

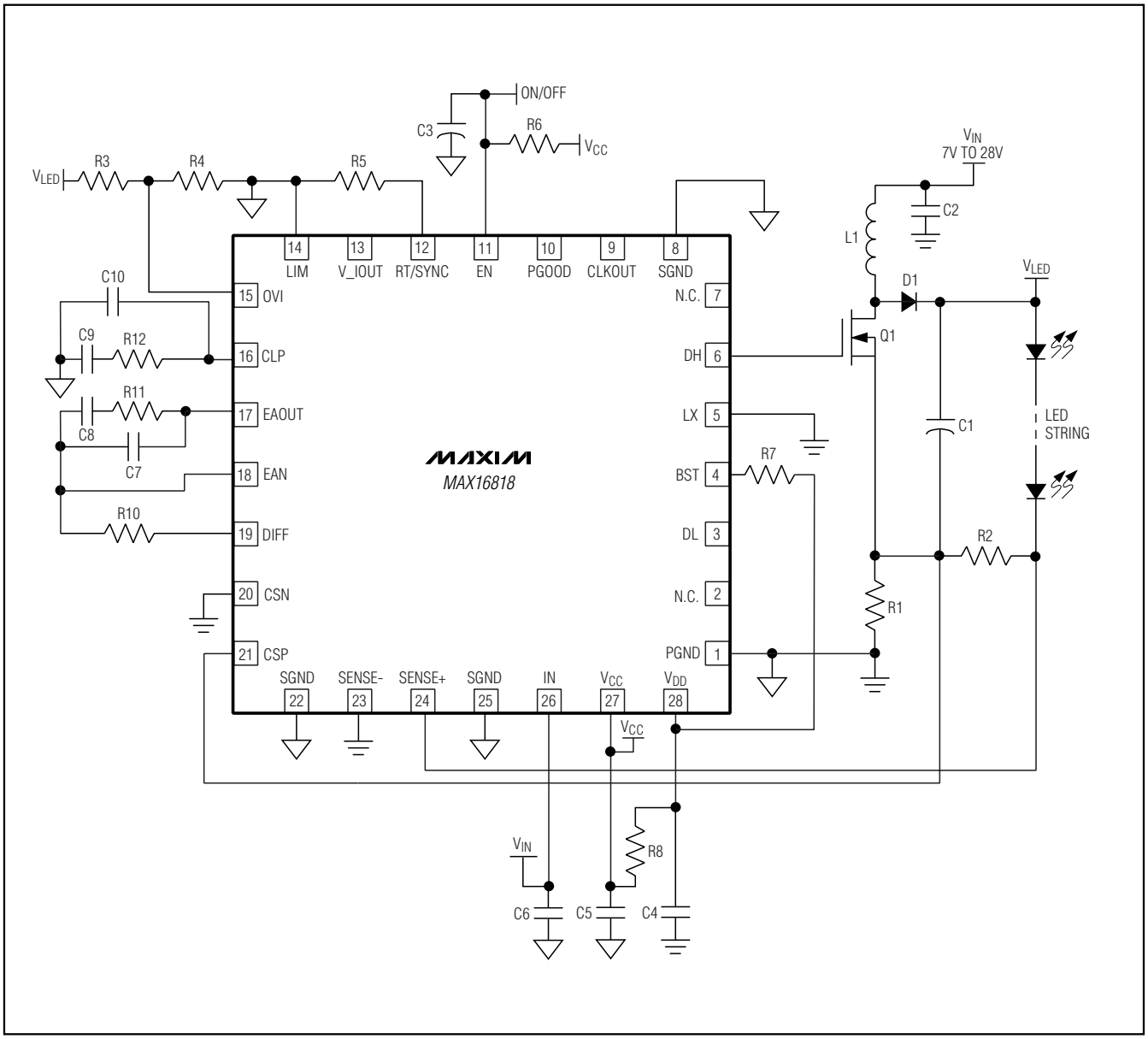


Figure 1. Typical Application Circuit for a Boost LED Driver (Nonsynchronous)

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

Typical Application Circuits (continued)

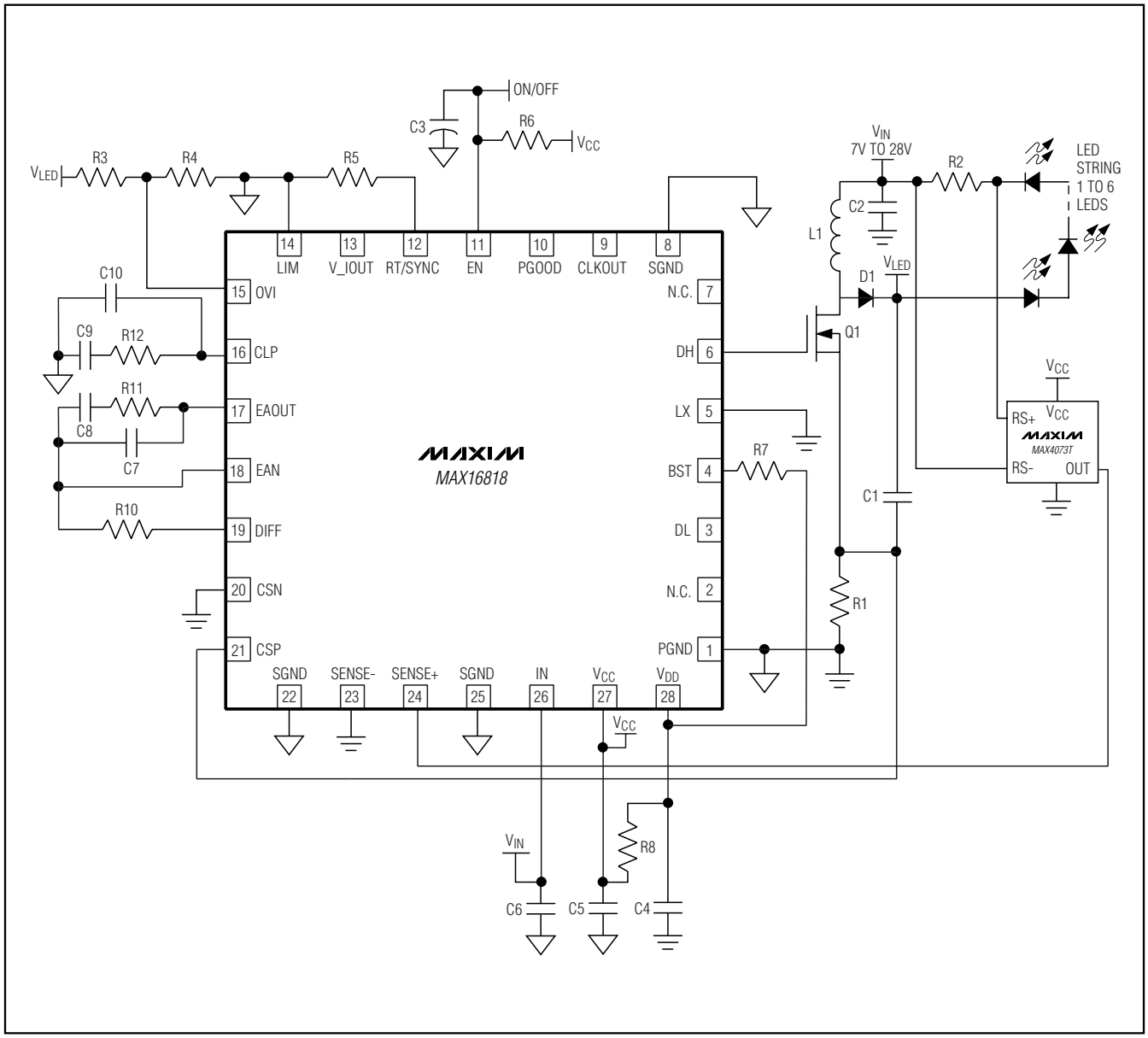


Figure 2. Typical Application Circuit for an Input-Referred Buck-Boost LED Driver (Input: 7V to 28V, Output: 1 to 6 LEDs in Series)

Typical Application Circuits (continued)

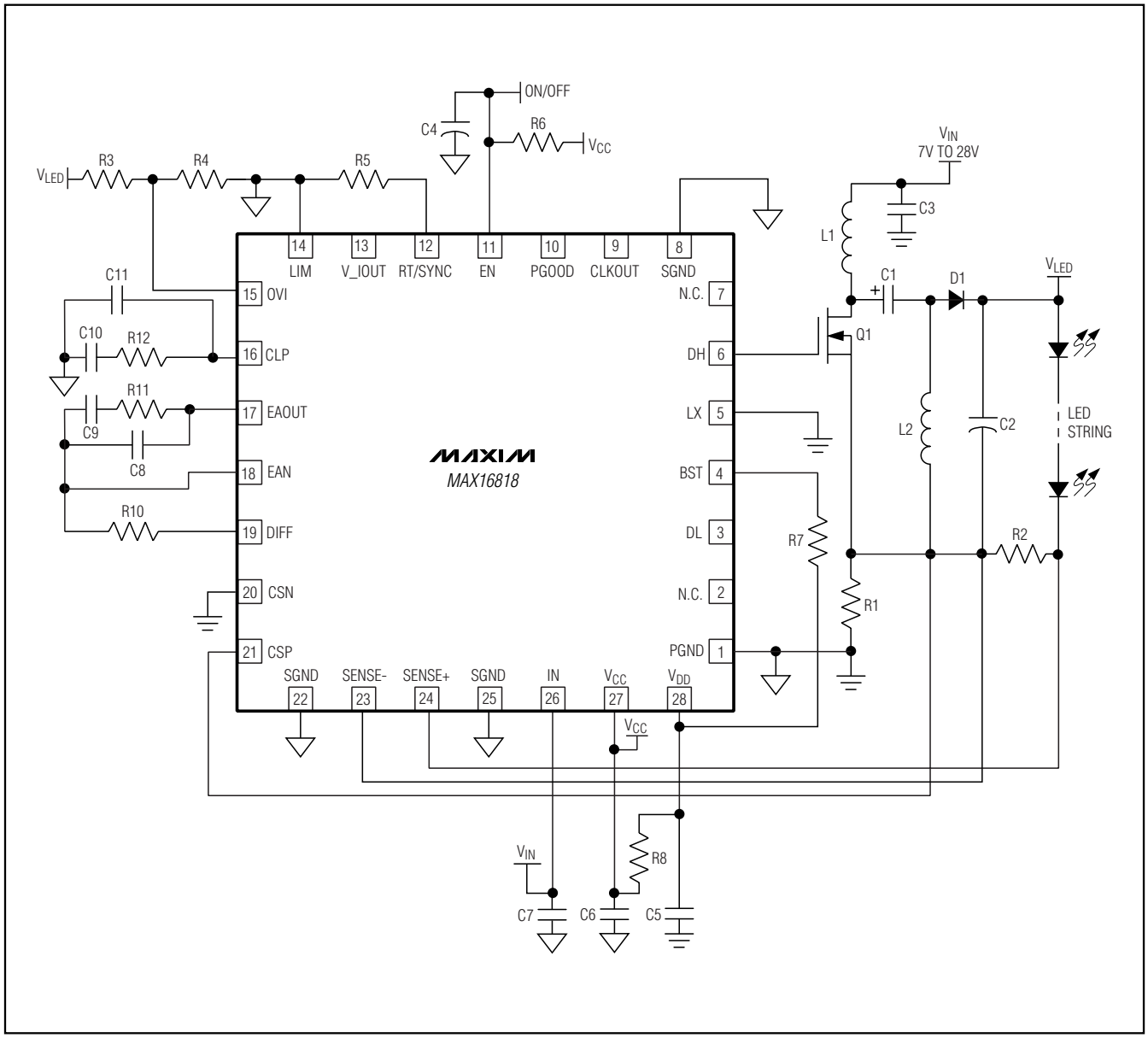


Figure 3. Typical Application Circuit for a SEPIC LED Driver

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

Typical Application Circuits (continued)

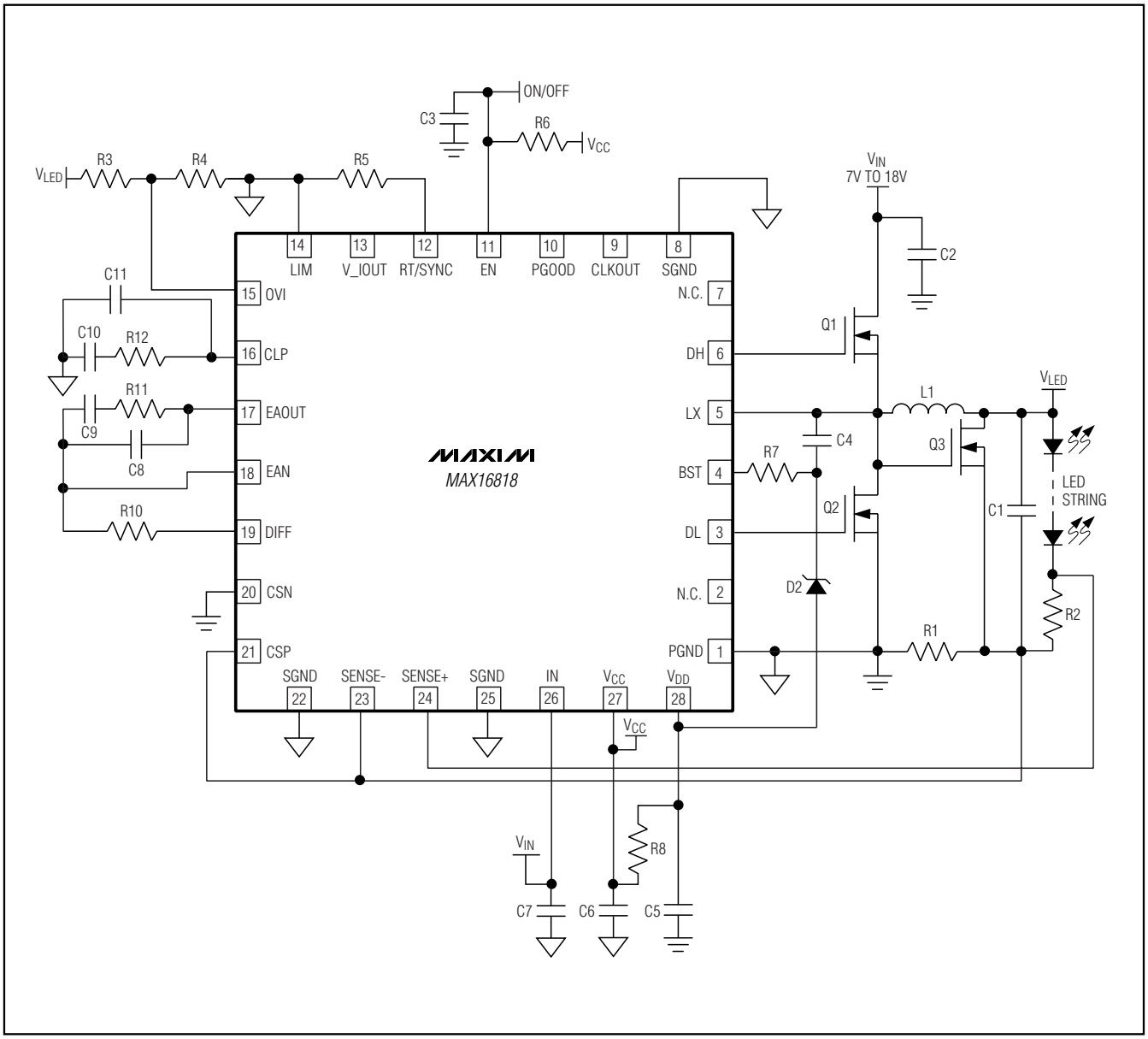


Figure 4. Application Circuit for a Ground-Referred Buck-Boost LED Driver

Typical Application Circuits (continued)

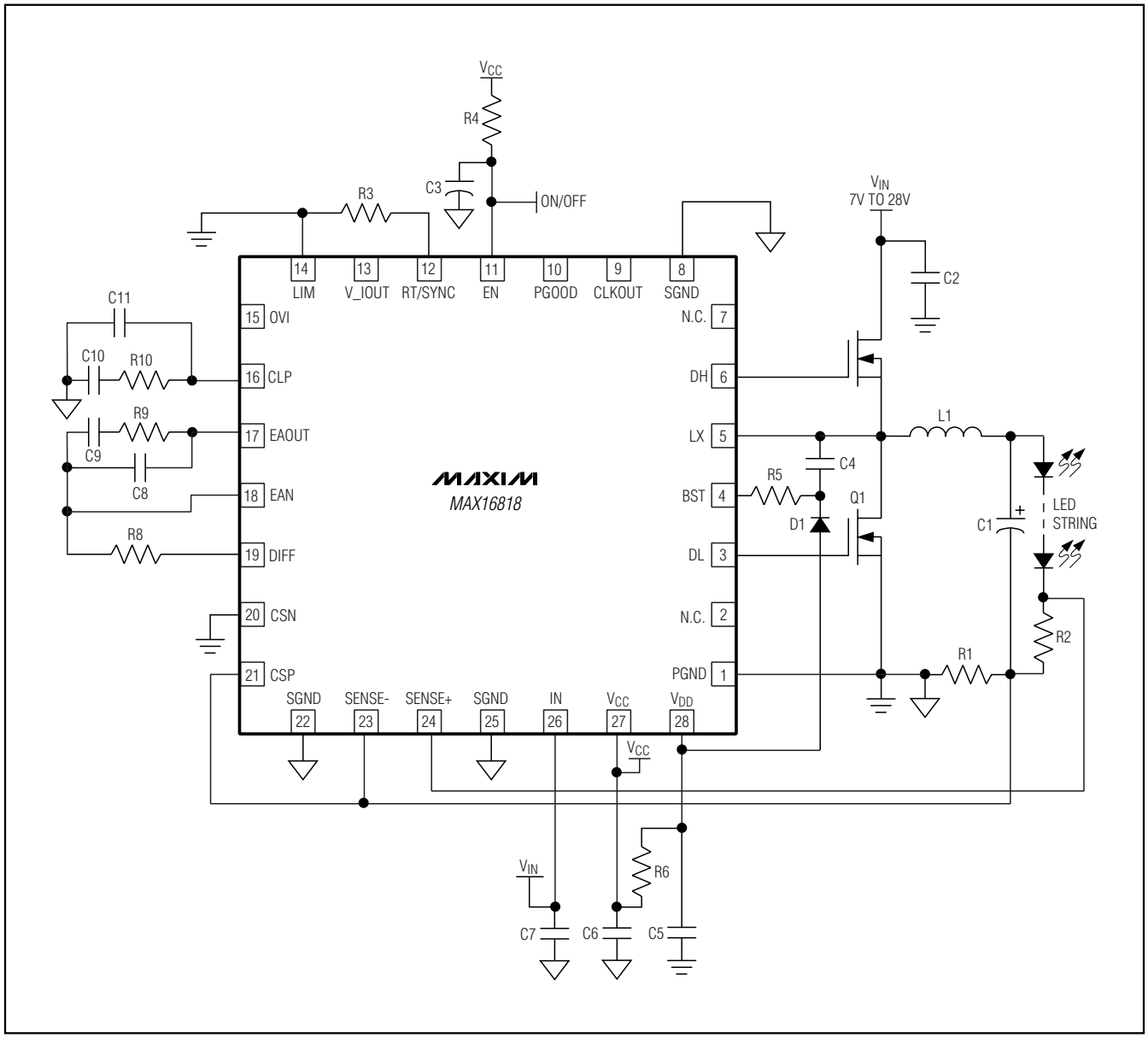


Figure 5. Application Circuit for a Buck LED Driver

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

Functional Diagram

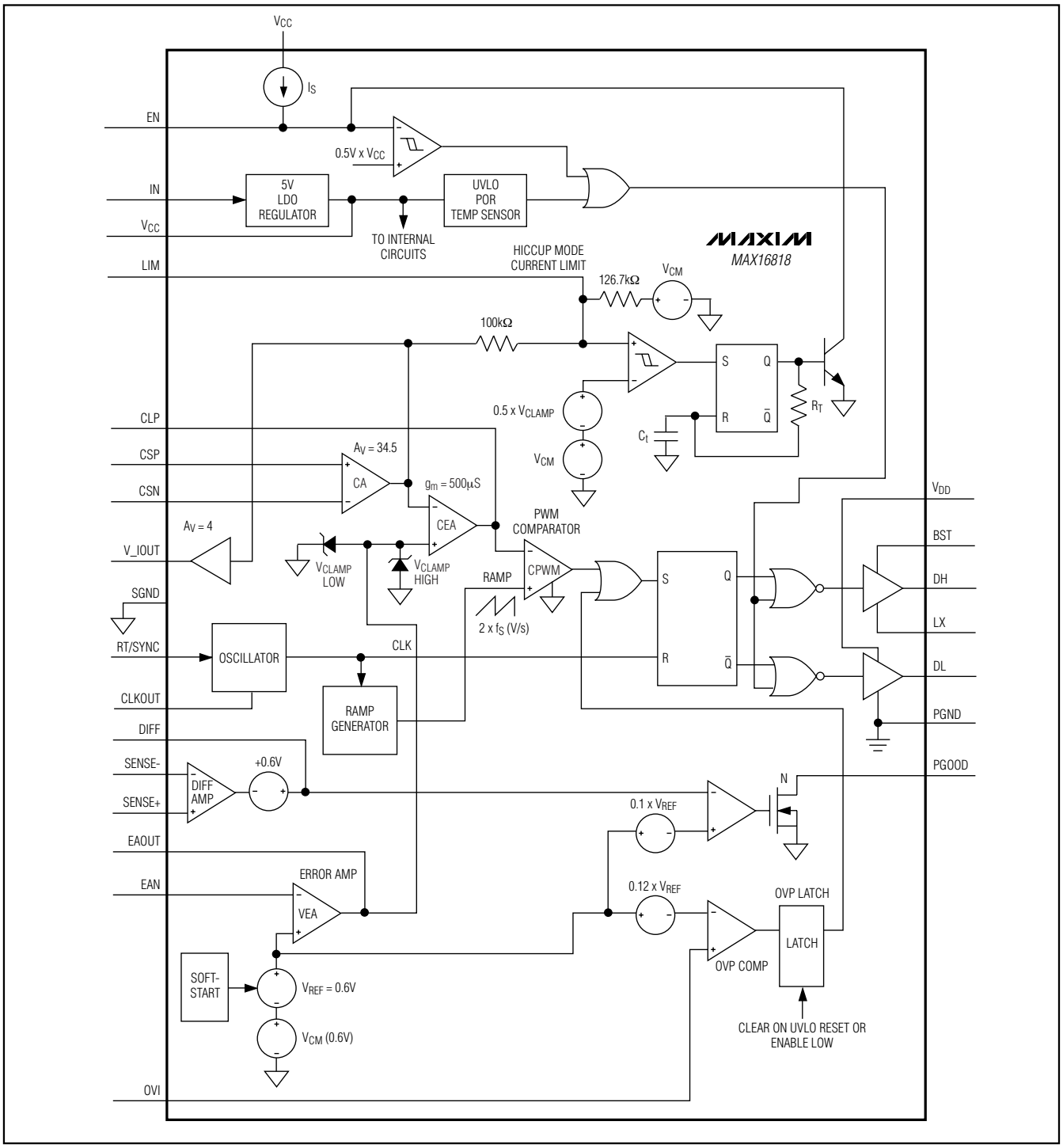


Figure 6. MAX16818 Functional Diagram

Detailed Description

The MAX16818 is a high-performance average-current-mode PWM controller for high-power, high-brightness LEDs (HBLEDs). Average current-mode control is the ideal method for driving HBLEDs. This technique offers inherently stable operation, reduces component derating and size by accurately controlling the inductor current. The device achieves high efficiency at high current (up to 30A) with a minimum number of external components. The high- and low-side drivers source and sink up to 4A for lower switching losses while driving high-gate-charge MOSFETs. The MAX16818's CLKOUT output is 180° out-of-phase with respect to the high-side driver. CLKOUT drives a second MAX16818 LED driver out of phase, reducing the input-capacitor ripple current.

The MAX16818 consists of an inner average current loop representing inductor current and an outer voltage loop voltage-error amplifier (VEA) that directly controls LED current. The combined action of the two loops results in a tightly regulated LED current. The inductor current is sensed across a current-sense resistor. The differential amplifier senses LED current through a sense resistor in series with the LEDs and the resulting sensed voltage is compared against an internal 0.6V reference at the error-amplifier input. The MAX16818 will adjust the LED current to within 1% accuracy to maintain emitted spectrum of the light in HBLEDs.

IN, V_{CC}, and V_{DD}

The MAX16818 accepts either a 4.75V to 5.5V or 7V to 28V input voltage range. All internal control circuitry operates from an internally regulated nominal voltage of 5V (V_{CC}). For input voltages of 7V or greater, the internal V_{CC} regulator steps the voltage down to 5V. The V_{CC} output voltage is a regulated 5V output capable of sourcing up to 60mA. Bypass the V_{CC} to SGND with 4.7µF and 0.1µF low-ESR ceramic capacitors for high-frequency noise rejection and stable operation.

The MAX16818 uses V_{DD} to power the low-side and high-side drivers. Isolate V_{DD} from V_{CC} with a 1Ω resistor and put a 1µF capacitor in parallel with a 0.1µF capacitor to ground to prevent high-current noise spikes created by the driver from disrupting internal circuitry.

The TQFN is a thermally enhanced package and can dissipate up to 2.7W. The high-power packages allow the high-frequency, high-current converter to operate from a 12V or 24V bus. Calculate power dissipation in the MAX16818 as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate-drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC}$$

$$I_{CC} = I_Q + [f_{SW} \times (Q_{G1} + Q_{G2})]$$

where Q_{G1} and Q_{G2} are the total gate charge of the low-side and high-side external MOSFETs at V_{GATE} = 5V, I_Q is 3.5mA (typ), and f_{SW} is the switching frequency of the converter.

Undervoltage Lockout (UVLO)

The MAX16818 includes an undervoltage lockout with hysteresis and a power-on-reset circuit for converter turn-on. The UVLO rising threshold is internally set at 4.35V with a 200mV hysteresis. Hysteresis at UVLO eliminates chattering during startup.

Most of the internal circuitry, including the oscillator, turns on when the input voltage reaches 4V. The MAX16818 draws up to 3.5mA of current before the input voltage reaches the UVLO threshold.

Soft-Start

The MAX16818 has an internal digital soft-start for a monotonic, glitch-free rise of the output current. Soft-start is achieved by the controlled rise of the error amplifier dominant input in steps using a 5-bit counter and a 5-bit DAC. The soft-start DAC generates a linear ramp from 0 to 0.7V. This voltage is applied to the error amplifier at a third (noninverting) input. As long as the soft-start voltage is lower than the reference voltage, the system converges to that lower reference value. Once the soft-start DAC output reaches 0.6V, the reference takes over and the DAC output continues to climb to 0.7V, assuring that it does not interfere with the reference voltage.

Internal Oscillator

The internal oscillator generates a clock with the frequency proportional to the inverse of R_T. The oscillator frequency is adjustable from 125kHz to 1.5MHz with better than 8% accuracy using a single resistor connected from RT/SYNC to SGND. The frequency accuracy avoids the over-design, size, and cost of passive filter components like inductors and capacitors. Use the following equation to calculate the oscillator frequency:

For 120kΩ ≤ R_T ≤ 500kΩ:

$$R_T = \frac{6.25 \times 10^{10}}{f_{SW}}$$

For 40kΩ ≤ R_T ≤ 120kΩ:

$$R_T = \frac{6.40 \times 10^{10}}{f_{SW}}$$

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The oscillator also generates a $2V_{P-P}$ voltage-ramp signal for the PWM comparator and a 180° out-of-phase clock signal for CLKOUT to drive a second LED regulator out-of-phase.

Synchronization

The MAX16818 can be easily synchronized by connecting an external clock to RT/SYNC. If an external clock is present, then the internal oscillator is disabled and the external clock is used to run the device. If the external clock is removed, the absence of clock for 32µs is detected and the circuit starts switching from the internal oscillator. Pulling RT/SYNC to ground for at least 50µs disables the converter. Use an open-collector transistor to synchronize the MAX16818 with the external system clock.

Control Loop

The MAX16818 uses an average-current-mode control scheme to regulate the output current (Figure 7). The main control loop consists of an inner current loop for controlling the inductor current and an outer current loop for regulating the LED current. The inner current loop absorbs the inductor pole reducing the order of the outer current loop to that of a single-pole system. The current loop consists of a current-sense resistor (R_S), a current-sense amplifier (CA), a current-error amplifier (CEA), an oscillator providing the carrier ramp, and a PWM comparator (CPWM) (Figure 7). The precision CA amplifies the sense voltage across R_S by a factor of 34.5. The inverting input to the CEA senses the CA output. The CEA output is the difference between the voltage-error amplifier output (EAOUT) and the amplified voltage from the CA. The RC compensation network connected to CLP provides external frequency compensation for the CEA. The start of every clock cycle enables the high-side drivers and initiates a PWM on-cycle. Comparator CPWM compares the output voltage from the CEA with a 0V to 2V ramp from the oscillator. The PWM on-cycle terminates when the ramp voltage exceeds the error voltage. Compensation for the outer LED current loop varies based upon the topology.

The MAX16818 outer LED current control loop consists of the differential amplifier (DIFF AMP), reference voltage, and VEA. The unity-gain differential amplifier provides true differential remote sensing of the voltage across the LED current set resistor, R_{LS}. The differential amplifier output connects to the inverting input (EAN) of the VEA. The DIFF AMP is bypassed and the inverting input is available to the pin for direct feedback. The noninverting input of the VEA is internally connected to an internal precision reference voltage, set to 0.6V. The VEA controls the inner current loop (Figure 6). A feedback network compensates the outer loop using the EAOUT and EAIN pins.

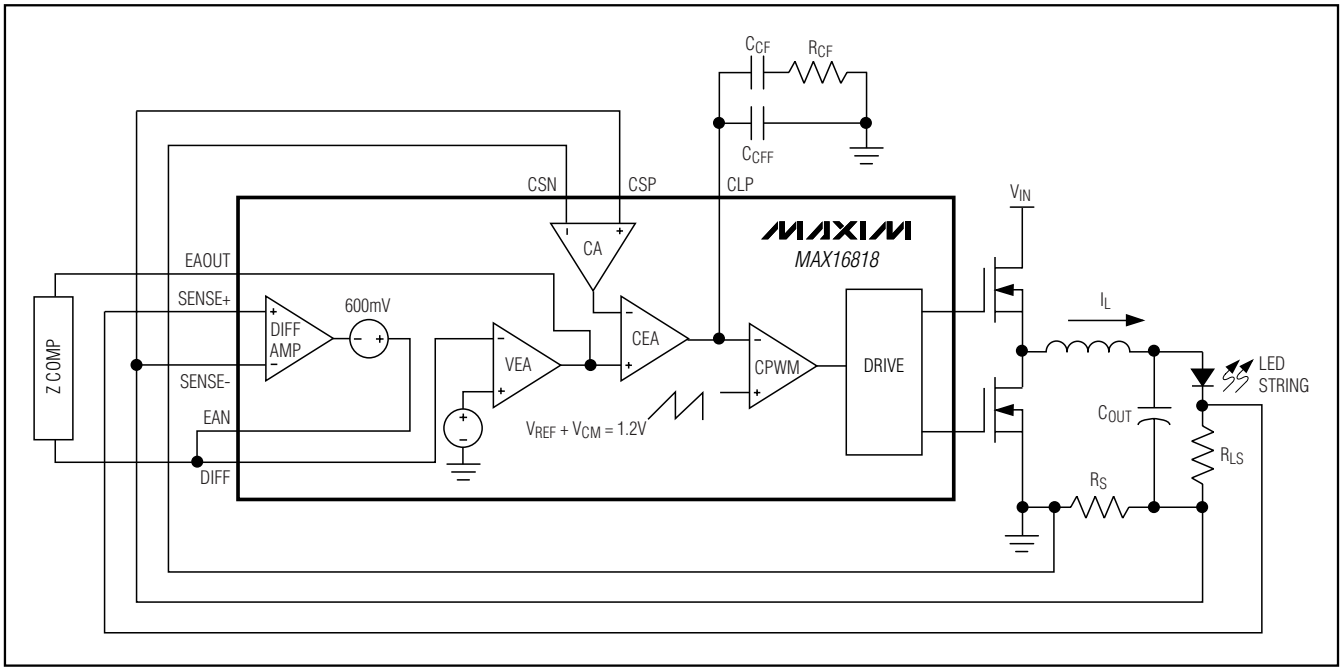

Figure 7. MAX16818 Control Loop

Inductor Current-Sense Amplifier

The differential current-sense amplifier (CA) provides a DC gain of 34.5. The maximum input offset voltage of the current-sense amplifier is 1mV and the common-mode voltage range is 0 to 5.5V (IN = 7V to 28V). The current-sense amplifier senses the voltage across a current-sense resistor. The maximum common-mode voltage is 3.6V when V_{IN} = 5V.

Inductor Peak-Current Comparator

The peak-current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions, such as an inductor malfunction (Figure 8). Note the average current-limit threshold of 26.9mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an inductor with a saturation current specification greater than the average current limit. Proper inductor selection ensures that only the extreme conditions trip the peak-current comparator, such as an inductor with a shorted turn. The 60mV threshold for triggering the peak-current limit is twice the full-scale average current-limit voltage threshold. The peak-current comparator has only a 260ns delay.

Current-Error Amplifier (For Inductor Currents)

The MAX16818 has a transconductance current-error amplifier (CEA) with a typical g_m of 550µS and 320µA output sink- and source-current capability. The current-error amplifier output CLP serves as the inverting input to the PWM comparator. CLP is externally accessible to provide frequency compensation for the inner current loops (Figure 7). Compensate (CEA) so the inductor current negative slope, which becomes the positive slope to the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM) sets the duty cycle for each cycle by comparing the output of the current-error amplifier to a $2V_{P-P}$ ramp. At the start of each clock cycle, an R-S flip-flop resets and the high-side driver (DH) goes high. The comparator sets the flip-flop as soon as the ramp voltage exceeds the CLP voltage, thus terminating the on-cycle (Figure 8).

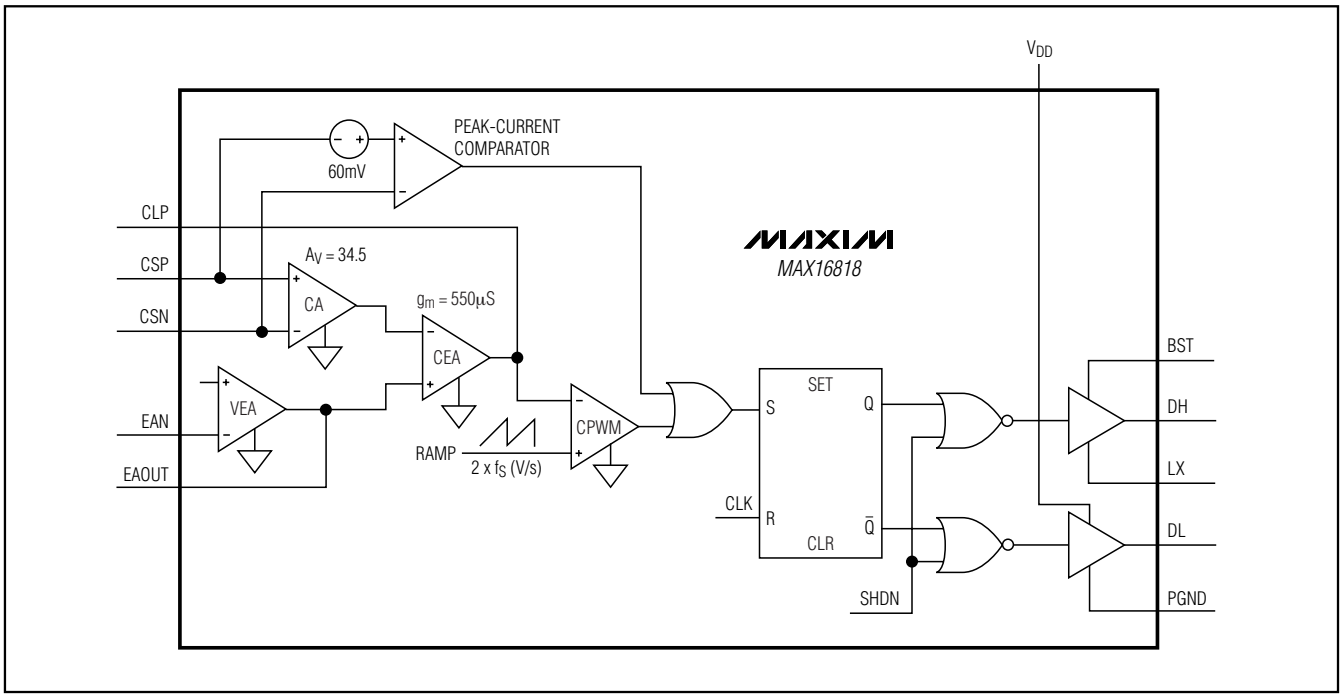

Figure 8. MAX16818 Phase Circuit

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Differential Amplifier

The DIFF AMP facilitates remote sensing at the load (Figure 7). It provides true differential LED current (through the R_{LS} sense resistor) sensing while rejecting the common-mode voltage errors due to high-current ground paths. The VEA provides the difference between the differential amplifier output (DIFF) and the desired LED current-sense voltage. The differential amplifier has a bandwidth of 3MHz. The difference between SENSE+ and SENSE- is regulated to 0.6V. Connect SENSE+ to the positive side of the LED current-sense resistor and SENSE- to the negative side of the LED current-sense resistor (which is often PGND).

MOSFET Gate Drivers (DH, DL)

The high-side (DH) and low-side (DL) drivers drive the gates of external n-channel MOSFETs (Figures 1–5). The drivers' 4A peak sink- and source-current capability provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced cross-conduction losses. Due to physical realities, extremely low gate charges and $R_{DS(ON)}$ resistance of MOSFETs are typically exclusive of each other. MOSFETs with very low $R_{DS(ON)}$ will have a higher gate charge and vice versa. Choosing the high-side MOSFET (Q1) becomes a trade-off between these two attributes. Applications where the input voltage is much higher than the output voltage result in a low duty cycle where conduction losses are less important than switching losses. In this case, choose a MOSFET with very low gate charge and a moderate $R_{DS(ON)}$. Conversely, for applications where the output voltage is near the input voltage resulting in duty cycles much greater than 50%, the $R_{DS(ON)}$ losses become at least equal, or even more important than the switching losses. In this case, choose a MOSFET with very low $R_{DS(ON)}$ and moderate gate charge. Finally, for the applications where the duty cycle is near 50%, the two loss components are nearly equal, and a balanced MOSFET with moderate gate charge and $R_{DS(ON)}$ work best.

In a buck topology, the low-side MOSFET (Q2) typically operates in a zero voltage switching mode, thus it does not have switching losses. Choose a MOSFET with very low $R_{DS(ON)}$ and moderate gate charge.

Size both the high-side and low-side MOSFETs to handle the peak and RMS currents during overload conditions. The driver block also includes a logic circuit that provides an adaptive nonoverlap time to prevent shoot-through currents during transition. The typical nonoverlap time between the high-side and low-side MOSFETs is 35ns.

BST

The MAX16818 uses V_{DD} to power the low- and high-side MOSFET drivers. The high-side driver derives its power through a bootstrap capacitor and V_{DD} supplies power internally to the low-side driver. Connect a 0.47µF low-ESR ceramic capacitor between BST and LX. Connect a Schottky rectifier from BST to V_{DD}. Keep the loop formed by the boost capacitor, rectifier, and IC small on the PCB.

Protection

The MAX16818 includes output overvoltage protection (OVP). During fault conditions when the load goes to high impedance (opens), the controller attempts to maintain LED current. The OVP protection disables the MAX16818 whenever the voltage exceeds the threshold, protecting the external circuits from undesirable voltages.

Current Limit

The VEA output is clamped to 930mV with respect to the common-mode voltage (V_{CM}). Average-current-mode control has the ability to limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the VEA output clamps to 930mV with respect to the common-mode voltage (0.6V) to limit the maximum current sourced by the converter to I_{LIMIT} = 26.9mV / R_S. The hiccup current limit overrides the average current limit. The MAX16818 includes hiccup current-limit protection to reduce the power dissipation during a fault condition. The hiccup current-limit circuit derives inductor current information from the output of the current amplifier. This signal is compared against one half of $V_{CLAMP(EA)}$. With no resistor connected from the LIM pin to ground, the hiccup current limit is set at 90% of the full-load average current limit. Use R_{EXT} to increase the hiccup current limit from 90% to 100% of the full load average limit. The hiccup current limit can be disabled by connecting LIM to SGND. In this case, the circuit follows the average current-limit action during overload conditions.

Overvoltage Protection

The OVP comparator compares the OVI input to the overvoltage threshold. A detected overvoltage event latches the comparator output forcing the power stage into the OVP state. In the OVP state, the high-side MOSFET turns off and the low-side MOSFET latches on. Connect OVI to the center tap of a resistor-divider from V_{LED} to SGND. In this case, the center tap is compared against 1.276V. Add an RC delay to reduce the sensitivity of the overvoltage circuit and avoid nuisance tripping of the converter. Disable the overvoltage function by connecting OVI to SGND.

Applications Information

Application Circuit Descriptions

This section provides some detail regarding the application circuits in the *Simplified Diagram* and Figures 1–5. The discussion includes some description of the topology as well as basic attributes.

High-Frequency LED Current Pulser

The *Simplified Diagram* shows the MAX16818 providing high-frequency, high-current pulses to the LEDs. The basic topology must be a buck, since the inductor always connects to the load in that configuration (in all other topologies, the inductor disconnects from the load at one time or another). The design minimizes the current ripple by oversizing the inductor, which allows for a very small (0.01µF) output capacitor. When MOSFET Q3 turns on, it diverts the current around the LEDs at a very fast rate. Q3 also discharges the output capacitor, but since the capacitor is so small, it does not stress the MOSFET. Resistor R1 senses the LED/Q3 current and there is no reaction to the short that Q3 places across the LEDs. This design is superior in that it does not attempt to actually change the inductor current at high frequencies and yet the current in the LEDs varies from zero to full in very small periods of time. The efficiency of this technique is very high. Q3 must be able to dissipate the LED current applied to its $R_{DS(ON)}$ at some maximum duty cycle. If the circuit needs to control extremely high currents, use paralleled MOSFETs. PGOOD is low during LED pulsed-current operation.

Boost LED Driver

In Figure 1, the external components configure the MAX16818 as a boost converter. The circuit applies the input voltage to the inductor during the on-time, and then during the off-time the inductor, which is in series with the input capacitor, charges the output capacitor. Because of the series connection between the input voltage and the inductor, the output voltage can never go lower than the input voltage. The design is nonsynchronous, and since the current-sense resistor connects to ground, the power supply can go to any output voltage (above the input) as long as the components are rated appropriately. R2 again provides the sense voltage the MAX16818 uses to regulate the LED current.

Input-Referenced LED Driver

The circuit in Figure 2 shows a step-up/step-down regulator. It is similar to the boost converter in Figure 1 in that the inductor is connected to the input and the MOSFET is essentially connected to ground. However, rather than going from the output to ground, the LEDs span from the output to the input. This effectively removes the boost-only restriction of the regulator in Figure 1, allowing the voltage across the LEDs to be greater than or less than the input voltage. LED current sensing is not ground-referenced, so a high-side current-sense amplifier is used to measure current.

SEPIC LED Driver

Figure 3 shows the MAX16818 configured as a SEPIC LED driver. While buck topologies require the output to be lesser than the input, and boost topologies require the output to be greater than the input, a SEPIC topology allows the output voltage to be greater than, equal to, or less than the input. In a SEPIC topology, the voltage across C1 is the same as the input voltage, and L1 and L2 are the same inductance. Therefore, when Q1 conducts (on-time), both inductors ramp up current at the same rate. The output capacitor supports the output voltage during this time. During the off-time, L1 current recharges C1 and combines with L2 to provide current to recharge C2 and supply the load current. Since the voltage waveform across L1 and L2 are exactly the same, it is possible to wind both inductors on the same core (a coupled inductor). Although voltages on L1 and L2 are the same, RMS currents can be quite different so the windings may have a different gauge wire. Because of the dual inductors and segmented energy transfer, the efficiency of a SEPIC converter is somewhat lower than standard bucks or boosts. As in the boost driver, the current-sense resistor connects to ground, allowing the output voltage of the LED driver to exceed the rated maximum voltage of the MAX16818.

Ground-Referenced Buck/Boost LED Driver

Figure 4 depicts a buck/boost topology. During the on-time with this circuit, the current flows from the input capacitor, through Q1, L1, and Q3 and back to the input capacitor. During the off-time, current flows up through Q2, L1, D1, and to the output capacitor C1. This topology resembles a boost in that the inductor sits between the input and ground during the on-time. However, during the off-time the inductor resides between ground and the output capacitor (instead of between the input and output capacitors in boost topologies), so the output voltage can be any voltage less than, equal to, or greater than the input voltage. As compared to the SEPIC topology, the buck/boost does not require two inductors or a series capacitor, but it does require two additional MOSFETs.

Buck Driver with Synchronous Rectification

In Figure 5, the input voltage can go from 7V to 28V and, because of the ground-based current-sense resistor, the

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output voltage can be as high as the input. The synchronous MOSFET keeps the power dissipation to a minimum, especially when the input voltage is large when compared to the voltage on the LED string. It is important to keep the current-sense resistor, R1, inside the LC loop, so that ripple current is available. To regulate the LED current, R2 creates a voltage that the differential amplifier compares to 0.6V. If power dissipation is a problem in R2, add a noninverting amplifier and reduce the value of the sense resistor accordingly.

Inductor Selection

The switching frequencies, peak inductor current, and allowable ripple at the output determine the value and size of the inductor. Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency. The charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs create switching losses. The situation worsens at higher input voltages, since switching losses are proportional to the square of the input voltage. The MAX16818 can operate up to 1.5MHz, however for V_{IN} > +12V, use lower switching frequencies to limit the switching losses.

The following discussion is for buck or continuous boost-mode topologies. Discontinuous boost, buck-boost, and SEPIC topologies are quite different in regards to component selection.

Use the following equations to determine the minimum inductance value:

Buck regulators:

$$L_{MIN} = \frac{(V_{INMAX} - V_{LED}) \times V_{LED}}{V_{INMAX} \times f_{SW} \times \Delta I_L}$$

Boost regulators:

$$L_{MIN} = \frac{(V_{LED} - V_{INMAX}) \times V_{INMAX}}{V_{LED} \times f_{SW} \times \Delta I_L}$$

where V_{LED} is the total voltage across the LED string. As a first approximation choose the ripple current, ΔI_L, equal to approximately 40% of the output current. Higher ripple current allows for smaller inductors, but it also increases the output capacitance for a given voltage ripple requirement. Conversely, lower ripple current increases the inductance value, but allows the output capacitor to reduce in size. This trade-off can be altered once standard inductance and capacitance values are chosen. Choose inductors from the standard surface-mount inductor series available from various manufacturers.

For example, for a buck regulator and 2 LEDs in series, calculate the minimum inductance at $V_{IN(MAX)}$ = 13.2V, V_{LED} = 7.8V, ΔI_L = 400mA, and f_{SW} = 330kHz:

Buck regulators:

$$L_{MIN} = \frac{(13.2 - 7.8) \times 7.8}{13.2 \times 330k \times 0.4} = 24.2\mu H$$

For a boost regulator with four LEDs in series, calculate the minimum inductance at $V_{IN(MAX)}$ = 13.2V, V_{LED} = 15.6V, ΔI_L =400mA, and f_{SW} = 330kHz:

Boost regulators:

$$L_{MIN} = \frac{(15.6 - 13.2) \times 13.2}{15.6 \times 330k \times 0.4} = 15.3\mu H$$

The average-current-mode control feature of the MAX16818 limits the maximum peak inductor current and prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current. Use the following equation to determine the worst-case inductor current:

$$L_{LPEAK} = \frac{V_{CL}}{R_S} + \frac{\Delta I_{CL}}{2}$$

where R_S is the inductor sense resistor and V_{CL} = 0.0282V.

Switching MOSFETs

When choosing a MOSFET for voltage regulators, consider the total gate charge, $R_{DS(ON)}$, power dissipation, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications.

The average current from the MAX16818 gate-drive output is proportional to the total capacitance it drives at DH and DL. The power dissipated in the MAX16818 is proportional to the input voltage and the average drive current. See the *IN, V_{CC}, and V_{DD}* section to determine the maximum total gate charge allowed from the combined driver outputs. The gate-charge and drain-capacitance (CV^2) loss, the cross-conduction loss in the upper MOSFET due to finite rise/fall times, and the I^2R loss due to RMS current in the MOSFET $R_{DS(ON)}$ account for the total losses in the MOSFET.

Buck Regulator

Estimate the power loss ($PD_{MOS\_}$) caused by the high-side and low-side MOSFETs using the following equations:

$$PD_{MOS-HI} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{2}\right) + (R_{DS(ON)} \times I_{RMS-HI}^2)$$

where Q_G, $R_{DS(ON)}$, t_R, and t_F are the upper-switching MOSFET's total gate charge, on-resistance at maximum operating temperature, rise time, and fall time, respectively.

$$I_{RMS-HI} = \sqrt{(I_{VALLEY}^2 + I_{PK}^2 + I_{VALLEY} \times I_{PK}) \times \frac{D}{3}}$$

For the buck regulator, $D = V_{LEDs} / V_{IN}$, $I_{VALLEY} = (I_{OUT} - \Delta I_L / 2)$ and $I_{PK} = (I_{OUT} + \Delta I_L / 2)$.

$$PD_{MOS-LO} = (Q_G \times V_{DD} \times f_{SW}) + (R_{DS(ON)} \times I_{RMS-LO}^2)$$

$$I_{RMS-LO} = \sqrt{(I_{VALLEY}^2 + I_{PK}^2 + I_{VALLEY} \times I_{PK}) \times \frac{(1-D)}{3}}$$

For example, from the typical specifications in the *Applications Information* section with V_{OUT} = 7.8V, the high-side and low-side MOSFET RMS currents are 0.77A and 0.63A, respectively, for a 1A buck regulator. Ensure that the thermal impedance of the MOSFET package keeps the junction temperature at least +25°C below the absolute maximum rating. Use the following equation to calculate the maximum junction temperature: $T_J = (PD_{MOS} \times \theta_{JA}) + T_A$, where θ_{JA} and T_A are the junction-to-ambient thermal impedance and ambient temperature, respectively.

To guarantee that there is no shoot-through from V_{IN} to PGND, the MAX16818 produces a nonoverlap time of 35ns. During this time, neither high- nor low-side MOSFET is conducting, and since the output inductor must maintain current flow, the intrinsic body diode of the low-side MOSFET becomes the conduction path. Since this diode has a fairly large forward voltage, a Schottky diode (in parallel to the low-side MOSFET) diverts current flow from the MOSFET body diode because of its lower forward voltage, which, in turn, increases efficiency.

Boost Regulator

Estimate the power loss ($PD_{MOS\_}$) caused by the MOSFET using the following equations:

$$PD_{FET} = (Q_G \times V_{DD} \times f_{SW}) + \left(\frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{2}\right) + (R_{DS(ON)} \times I_{RMS-HI}^2)$$

$$I_{RMS-HI} = \sqrt{(I_{VALLEY}^2 + I_{PK}^2 + I_{VALLEY} \times I_{PK}) \times \frac{D}{3}}$$

For a boost regulator in continuous mode, $D = V_{LEDs} / (V_{IN} + V_{LEDs})$, $I_{VALLEY} = (I_{OUT} - \Delta_L / 2)$ and $I_{PK} = (I_{OUT} + \Delta I_L / 2)$.

The voltage across the MOSFET:

$$V_{MOSFET} = V_{LED} + V_F$$

where V_F is the maximum forward voltage of the diode.

The output diode on a boost regulator must be rated to handle the LED series voltage, V_{LED}. It should also have fast reverse-recovery characteristics and should handle the average forward current that is equal to the LED current.

Input Capacitors

For buck regulator designs, the discontinuous input current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. Increasing switching frequency or paralleling out-of-phase converters lowers the peak-to-average current ratio, yielding a lower input capacitance requirement for the same LED current. The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high-ripple-current capability at the input. Assume the contributions from the ESR and capacitor discharge are equal to 30% and 70%, respectively. Calculate the input capacitance and ESR required for a specified ripple using the following equation:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_L}{2}\right)}$$

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Buck:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where I_{OUT} is the output current of the converter. For example, at V_{IN} = 13.2V, V_{LED} = 7.8V, I_{OUT} = 1A, ΔI_L = 0.4A, and f_{SW} = 330kHz, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 25mΩ and 10µF.

For boost regulator designs, the input-capacitor current waveform is dominated by the inductor, a triangle wave a magnitude of ΔI_L. For simplicity's sake, the current waveform can be approximated by a square wave with a magnitude that is half that of the triangle wave. Calculate the input capacitance and ESR required for a specified ripple using the following equation:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{\Delta I_L}$$

Boost:

$$C_{IN} = \frac{\frac{\Delta I_L}{2} \times D}{\Delta V_Q \times f_{SW}}$$

Duty cycle, D, for a boost regulator is equal to (V_{OUT} - V_{IN}) / V_{OUT}. As an example, at V_{IN} = 13.2V, V_{LED} = 15.6V, I_{OUT} = 1A, ΔI_L = 0.4A, and f_{SW} = 330kHz, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less yielding an ESR and capacitance value of 250mΩ and 1µF, respectively.

Output Capacitor

For buck converters, the inductor always connects to the load, so the inductance controls the ripple current. The output capacitance shunts a fraction of this ripple current and the LED string absorbs the rest. The capacitor reactance (which includes the capacitance and ESR) and the dynamic impedance of the LED diode string form a conductance divider that splits the ripple current between the LEDs and the capacitor. In many cases, the capacitor is very large as compared to the ESR, and this divider reduces to the ESR and the LED resistance.

Boost converters place a harsher requirement on the output capacitors as they must sustain the full load during the on-time of the MOSFET and are replenished during the off-time. The ripple current in this case is the full load current, and the holdup time is equal to the duty cycle times the switching period.

Current Limit

In addition to the average current limit, the MAX16818 also has hiccup current limit. The hiccup current limit is set to 10% below the average current limit to ensure that the circuit goes in hiccup mode during continuous output short circuit. Connecting a resistor from LIM to ground increases the hiccup current limit, while shorting LIM to ground disables the hiccup current-limit circuit.

Average Current Limit

The average-current-mode control technique of the MAX16818 accurately limits the maximum output current. The MAX16818 senses the voltage across the sense resistor and limit the peak inductor current (I_{L-PK}) accordingly. The on-cycle terminates when the current-sense voltage reaches 25.5mV (min). Use the following equation to calculate the maximum current-sense resistor value:

$$R_S = \frac{0.0255}{I_{OUT}}$$

$$PD_R = \frac{0.75 \times 10^{-3}}{R_S}$$

where PD_R is the dissipation in the series resistors. Select a 5% lower value of R_S to compensate for any parasitics associated with the PCB. Also, select a non-inductive resistor with the appropriate power rating.

Hiccup Current Limit

The hiccup current-limit value is always 10% lower than the average current-limit threshold, when LIM is left unconnected. Connect a resistor from LIM to SGND to increase the hiccup current-limit value from 90% to 100% of the average current-limit value. The average current-limit architecture accurately limits the average output current to its current-limit threshold. If the hiccup current limit is programmed to be equal or above the average current-limit value, the output current does not reach the point where the hiccup current limit can trigger. Program the hiccup current limit at least 5% below the average current limit to ensure that the hiccup current-limit circuit triggers during overload. See the Hiccup Current Limit vs. R_{EXT} graph in the *Typical Operating Characteristics*.

Compensation

The main control loop consists of an inner current loop (inductor current) and an outer LED current loop. The MAX16818 uses an average current-mode control scheme to regulate the LED current (Figure 7). The VEA output provides the controlling voltage for the current source. The inner current loop absorbs the inductor pole reducing the order of the LED current loop to that of a single-pole system.

The major consideration when designing the current control loop is making certain that the inductor downslope (which becomes an upslope at the output of the CEA) does not exceed the internal ramp slope. This is a necessary condition to avoid subharmonic oscillations similar to those in peak current mode with insufficient slope compensation. This requires that the gain at the output of the CEA be limited based on the following equation (Figure 6):

Buck:

$$R_{CF} \le \frac{V_{RAMP} \times f_{SW} \times L}{A_V \times R_S \times V_{OUT} \times g_m}$$

$$R_{CF} \le 105 \frac{f_{SW} \times L}{R_S \times V_{OUT}}$$

where V_{RAMP} = 2V, g_m = 550µs, A_V = 34.5.

Boost:

$$R_{CF} \le \frac{V_{RAMP} \times f_{SW} \times L}{A_V \times R_S \times (V_{OUT} - V_{IN}) \times g_m}$$

$$R_{CF} \le 105 \frac{f_{SW} \times L}{R_S \times (V_{OUT} - V_{IN})}$$

Solving for the gain of the CEA amplifier,

Buck:

$$g_m \times R_{CF} = \frac{\Delta V_{CEA}}{\Delta V_{CA}} = \frac{V_{RAMP} \times f_{SW} \times L}{V_{OUT} \times R_S \times A_V}$$

Boost:

$$g_m \times R_{CF} = \frac{\Delta V_{CEA}}{\Delta V_{CA}} = \frac{V_{RAMP} \times f_{SW} \times L}{(V_{OUT} - V_{IN}) \times R_S \times A_V}$$

In order to choose C_{CF}, the external loop gain must be considered. The following equation describes the overall loop gain for a buck regulator, which is the ratio of a small-signal change in the output of amplifier CA to the output of amplifier CEA:

External Loop Buck:

$$\frac{\Delta V_{CA}}{\Delta V_{CEA}} = \frac{R_S \times V_{IN} \times A_V}{V_{RAMP} \times sL}$$

where A_V is the gain of the current amplifier (34.5) and V_{RAMP} is voltage peak (2V) of the internal ramp. Multiplying the external loop gain with the CEA amplifier gain gives the total loop equation and solves for the frequency that yields a gain of 1 results in:

Total Loop Buck:

$$f_{CMAX} = \frac{V_{IN} \times f_{SW}}{2\pi V_{OUT}}$$

To be stable, the gain of the CEA amplifier must have a zero placed before f_{CMAX}. C_{CF} creates a pole at the origin and the combination of R_{CF} and C_{CF} creates the zero. Lower frequency zeros result in less bandwidth, but greater phase margin. The pole created by C_{CFF} (in conjunction with R_{CF}) is for noise reduction and can be placed well past the crossover frequency.

The following equation describes the external loop gain for a boost regulator:

External Loop Boost:

$$\frac{\Delta V_{CA}}{\Delta V_{CEA}} = \frac{R_S \times V_{OUT} \times A_V}{V_{RAMP} \times sL}$$

To get the total loop gain for a boost regulator, multiply the external loop gain with the gain of the CEA amplifier to arrive at the following:

Total Loop Boost:

$$f_{CMAX} = \frac{f_{SW} \times V_{OUT}}{2\pi (V_{OUT} - V_{IN})}$$

As in the buck regulator, the zero created by R_{CF} and C_{CF} sits at a frequency lower than f_{CMAX} to maintain stable operation.

1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

Power Dissipation

The TQFN is a thermally enhanced package and can dissipate about 2.7W. The high-power package makes the high-frequency, high-current LED driver possible to operate from a 12V or 24V bus. Calculate power dissipation in the MAX16818 as a product of the input voltage and the total V_{CC} regulator output current (I_{CC}). I_{CC} includes quiescent current (I_Q) and gate drive current (I_{DD}):

$$P_D = V_{IN} \times I_{CC}$$

$$I_{CC} = I_Q + \left[f_{SW} \times (Q_{G1} + Q_{G2})\right]$$

where Q_{G1} and Q_{G2} are the total gate charge of the low-side and high-side external MOSFETs at V_{GATE} = 5V, I_Q is estimated from the Supply Current (I_Q) vs. Frequency graph in the *Typical Operating Characteristics*, and f_{SW} is the switching frequency of the LED driver. For boost drivers, only consider one gate charge, Q_{G1}.

Use the following equation to calculate the maximum power dissipation (P_{DMAX}) in the chip at a given ambient temperature (T_A):

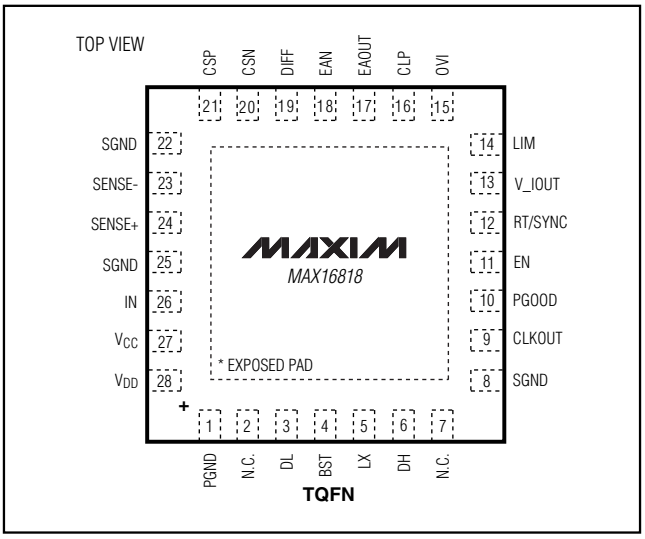
$$P_{DMAX} = 34.5 \times (150 - T_A)\ mW.$$

PCB Layout Guidelines

Use the following guidelines to layout the switching voltage regulator:

1) Place the IN, V_{CC}, and V_{DD} bypass capacitors close to the MAX16818.
2) Minimize the area and length of the high current loops from the input capacitor, upper switching MOSFET, inductor, and output capacitor back to the input capacitor negative terminal.
3) Keep short the current loop formed by the lower switching MOSFET, inductor, and output capacitor.
4) Place the Schottky diodes close to the lower MOSFETs and on the same side of the PCB.
5) Keep the SGND and PGND isolated and connect them at one single point.
6) Run the current-sense lines CSP and CSN very close to each other to minimize the loop area. Similarly, run the remote voltage-sense lines SENSE+ and SENSE- close to each other. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of the current-sense resistors.
7) Avoid long traces between the V_{DD} bypass capacitors, the driver output of the MAX16818, the MOSFET gates, and PGND. Minimize the loop formed by the V_{CC} bypass capacitors, bootstrap diode, bootstrap capacitor, the MAX16818, and the upper MOSFET gate.
8) Distribute the power components evenly across the board for proper heat dissipation.
9) Provide enough copper area at and around the switching MOSFETs, inductor, and sense resistors to aid in thermal dissipation.
10) Use wide copper traces (2oz) to keep trace inductance and resistance low to maximize efficiency. Wide traces also cool heat-generating components.

Pin Configuration



Chip Information

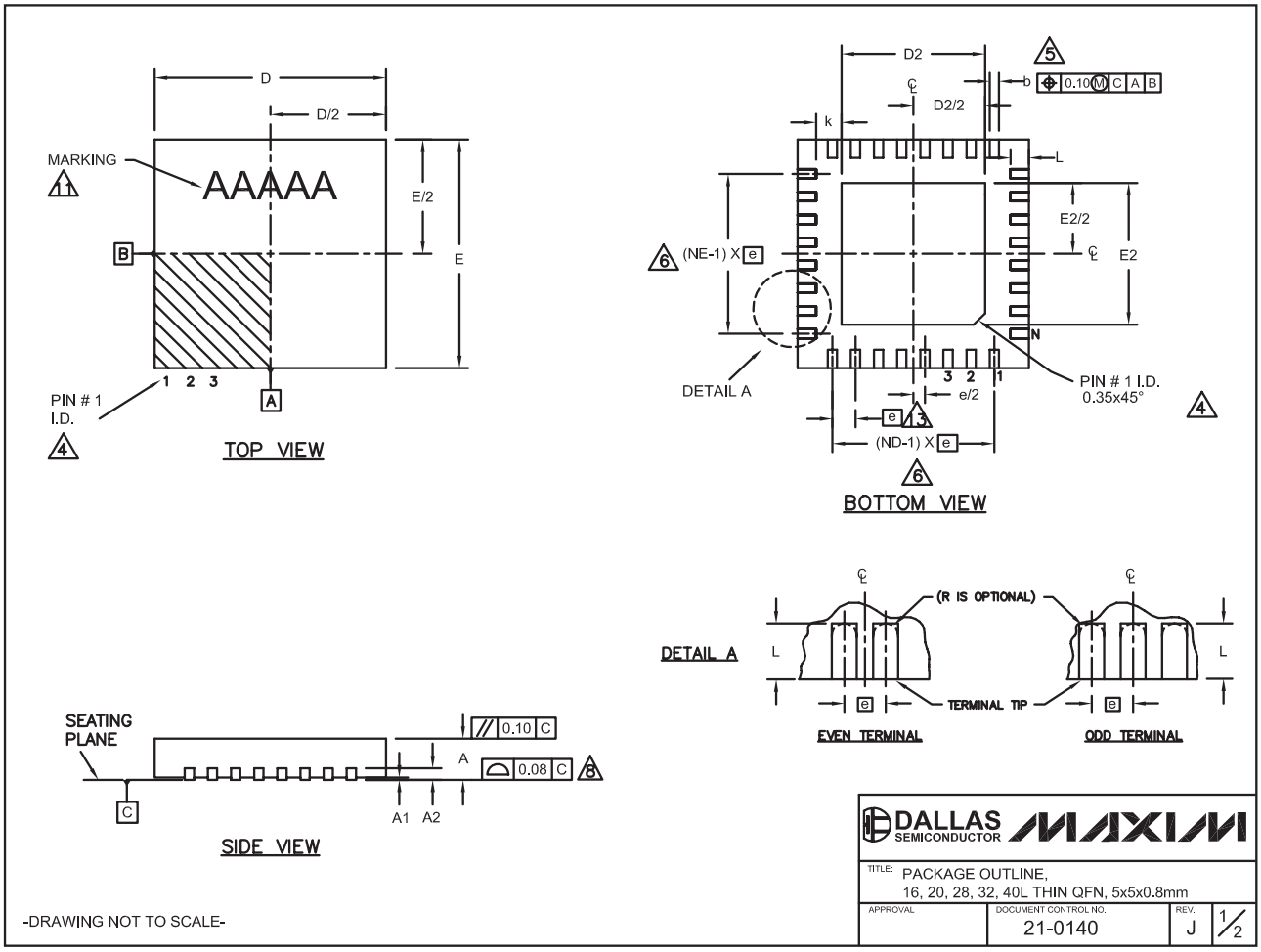
TRANSISTOR COUNT: 5654

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



1.5MHz, 30A High-Efficiency, LED Driver with Rapid LED Current Pulsing

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-—		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	J	2/2