Rail-to-Rail Upstream ADSL Line Driver

AD45048

FEATURES

Dual op amp
Voltage feedback
Wide supply range: from 3.3 V to 24 V
Rail-to-rail output
- **Output swing to within 0.5 V of supply rails @ 230 mA**
- **23 V p-p differential, R_{LOAD} of 50 Ω from 12 V supply**

High output current
Linear output current of 230 mA peak into 25 Ω
–68 dBc MTPR @ 15 dBm (100 Ω telephone line)
Low noise
- **4.5 nV/√Hz voltage noise density @ 100 kHz**
- **1.5 pA/√Hz current noise density @ 100 kHz**

High speed
- **65 MHz bandwidth (A_V = 1, –3 dB)**
- **55 V/µs slew rate (R_{LOAD} = 25 Ω)**

APPLICATIONS

Consumer xDSL modems
Twisted pair line drivers
ADSL CPE applications
- **(Drop in replacement for TS613ID and EL1519CS)**

Audio applications

GENERAL DESCRIPTION

The AD45048 ADSL CPE line driver is a dual operational amplifier capable of driving high output current (230 mA); it features a rail-to-rail output stage that swings to within 0.5 V of the supply rails. The AD45048 rail-to-rail output stage surpasses the output voltage capability of typical emitter-follower output stages and can deliver up to 23 V p-p differentially from a single 12 V supply in ADSL CPE line driving applications. The low distortion, high output current and wide output dynamic range make the AD45048 ideal for driving upstream signals in ADSL CPE applications.

Fabricated with ADI's high speed XFCB-HV (eXtra Fast Complementary Bipolar-High Voltage) process, the high bandwidth and fast slew rate of the AD45048 keep distortion to a minimum while dissipating minimum power. The AD45048 is available in a standard 8-lead SOIC package that can operate from –40°C to +85°C.

PIN CONFIGURATION

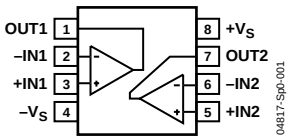

Figure 1. 8-Lead SOIC

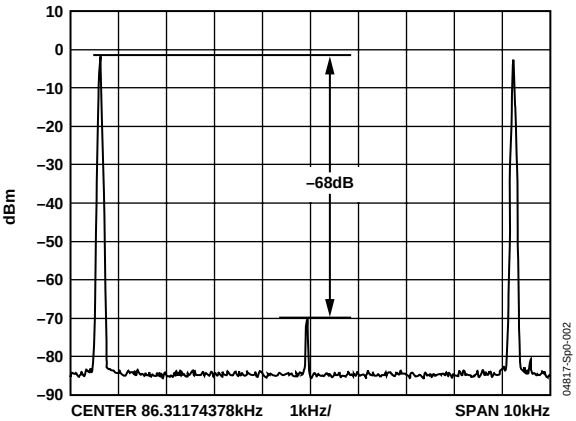

Figure 2. AD45048AR Upstream ADSL MTPR (13 dBm, CF = 5.3)

Rev. A

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Changes to Ordering Guide 8

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±6 V or +12 V (@ T_A = 25°C, G = +10, R_L = 100 Ω, unless otherwise noted).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.1 V p-p, R_{FB} = 0 Ω, R_{LOAD} = 25 Ω		65		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p single-ended, G = +1, R_{LOAD} = 25 Ω		3.35		MHz
Large Signal Bandwidth	V_{OUT} = 1 V p-p single-ended, G = +10, R_{LOAD} = 25 Ω		4.5		MHz
Large Signal Slew Rate	V_{OUT} = 5 V p-p, G = +1, R_{LOAD} = 25 Ω		55		V/µs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 40 kHz, V_{OUT} = 6 V p-p, single-ended, R_{LOAD} = 25 Ω		−80		dBc
Multitone Power Ratio	26 kHz to 134 kHz, Z_{LINE} = 100 Ω, XFMR = 1:2 turns, P_{LINE} = 13 dBm		−68		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1	2.5	mV
	T_{MIN} − T_{MAX}		2.5		mV
Input Offset Voltage Match			1	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} − T_{MAX}		1.3		µA
Input Offset Current			50	300	nA
Open-Loop Gain		85	94		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
OUTPUT CHARACTERISTICS					
Output Resistance	1.4 MHz; G = +1		0.2		Ω
Output Voltage Swing	Maximum swing (differential) V_{OMAX}, R_{LOAD} = 50 Ω differential	11.25	11.5		V diff
	Minimum swing (differential) V_{OMIN}, R_{LOAD} = 50 Ω differential		−11.5	−11.25	V diff
Differential Output Voltage Swing	$\Delta V_{OUT} = V_{OMAX} - V_{OMIN}$	22.5	23		V p-p
Single-Ended +Swing	R_{LOAD} = 25 Ω	5.68	5.76		V_p
Single-Ended -Swing	R_{LOAD} = 25 Ω		−5.67	−5.58	V_p
Single-Ended +Swing	R_{LOAD} = 100 Ω	5.92	5.95		V_p
Single-Ended –Swing	R_{LOAD} = 100 Ω		−5.91	−5.86	V_p
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		7	9	12	mA
Power Supply Rejection Ratio	±0.5 V		−85	−75	dB
Common-Mode Rejection Ratio	±1 V		−86	−79	dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$[1]
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] θ_{JA} = 112.7°C/W for SOIC package in still air based on 2S2P JEDEC PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

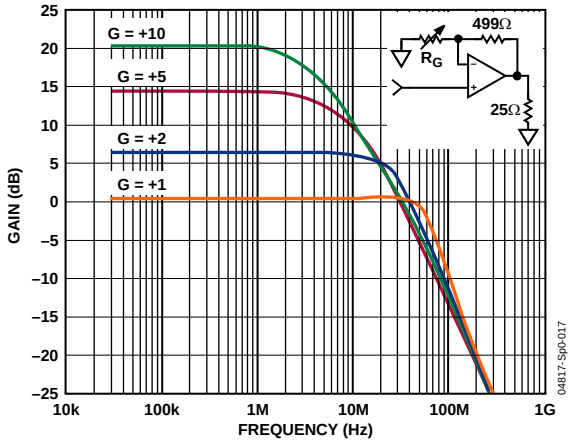


Figure 3. Noninverting Small Signal Bandwidth
(V_S = ±6 V, V_O = 0.1 V p-p, R_L = 25 Ω)

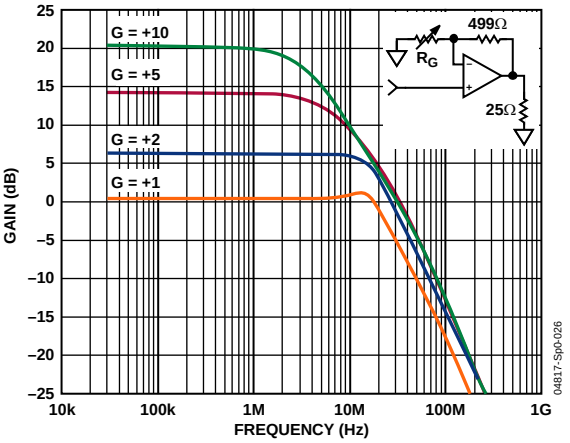


Figure 6. Noninverting Large Signal Bandwidth
(V_S = ±6 V, V_O = 1 V p-p, R_L = 25 Ω)

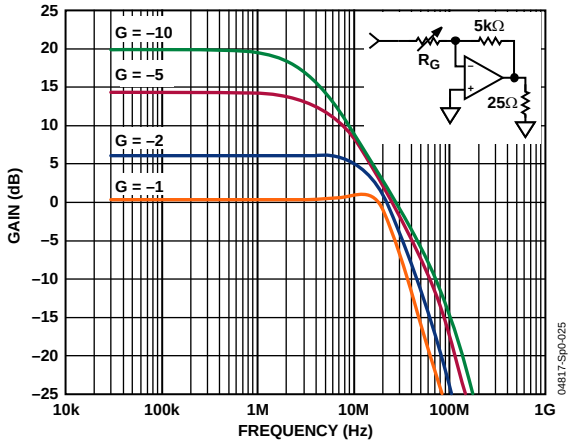


Figure 4. Inverting Small Signal Bandwidth
(V_S = ±6 V, V_O = 0.1 V p-p, R_L = 25 Ω)

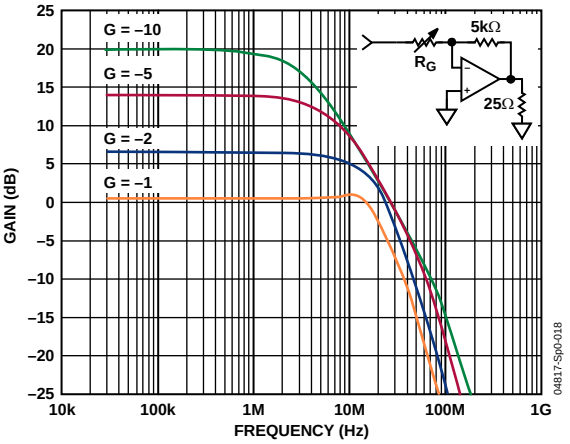


Figure 7. Inverting Large Signal Bandwidth
(V_S = ±6 V, V_O = 1 V p-p, R_L = 25 Ω)

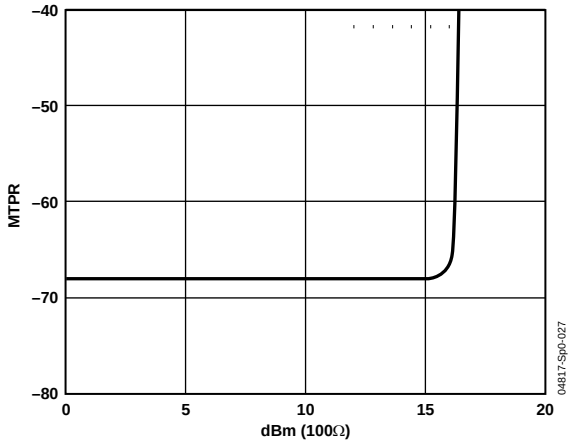


Figure 5. MTPR vs. Line Power (See Schematic in Figure 8)

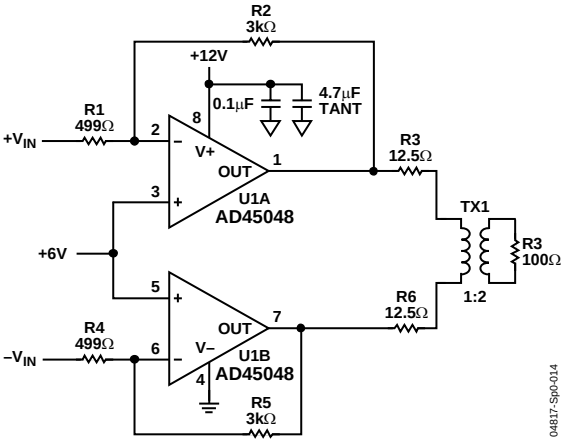


Figure 8. Differential Test Circuit for MTPR

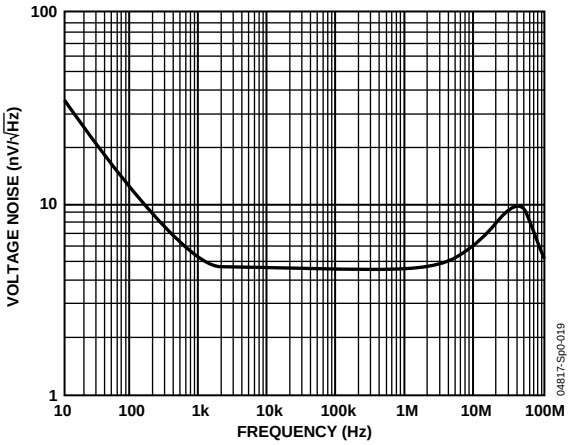


Figure 9. Voltage Noise vs. Frequency, V_S = ±6 V

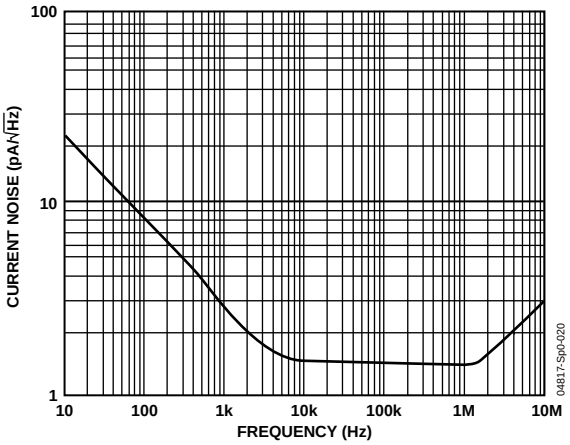


Figure 12. Input Current Noise vs. Frequency, V_S = ±6 V

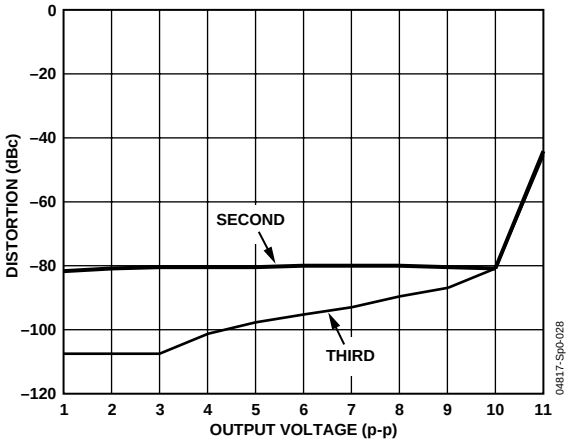


Figure 10. Single-Ended Harmonic Distortion, V_S = ±6 V dc, G = +6, R_F = 499 Ω, R_G = 100 Ω, R_L = 25 Ω, Fundamental Frequency = 40 kHz

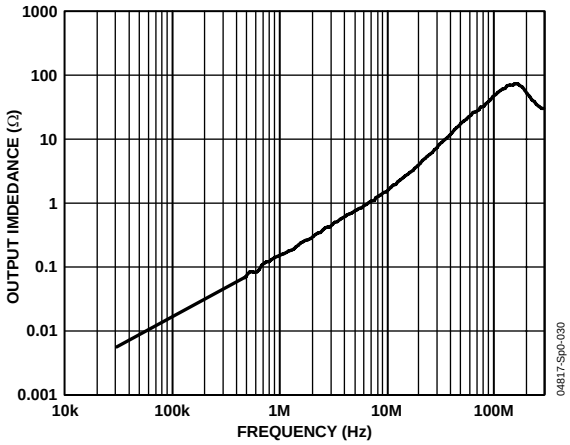


Figure 13. Output Impedance vs. Frequency

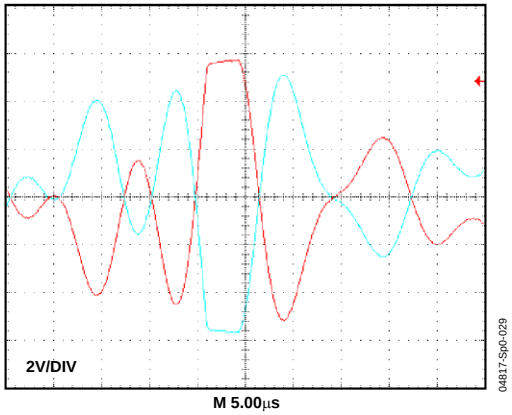


Figure 11. Discrete Multitone Modulation Overdrive Recovery (See Schematic in Figure 8)

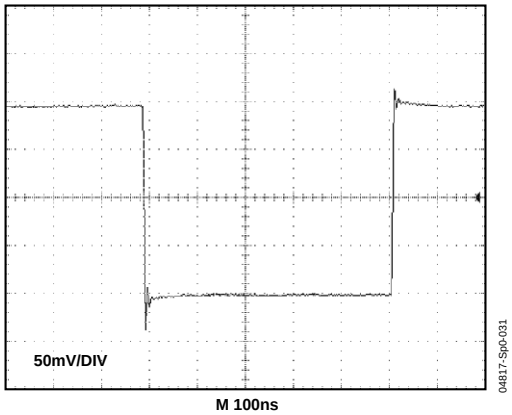


Figure 14. Small Signal Pulse Response R_{LOAD} = 1 kΩ, R_{FB} = 500 Ω

GENERAL DESCRIPTION

The AD45048 is a voltage feedback, rail-to-rail output amplifier with high output current capability. Fabricated on Analog Devices' proprietary high speed eXtra fast complementary bipolar high voltage process (XFCB-HV), the high bandwidth and fast slew rate of the AD45048 keep distortion to a minimum while dissipating minimum power. The XFCB-HV, silicon-on-insulator (SOI) process prevents latch-up problems and enables the construction of high frequency, low distortion amplifiers, such as the AD45048.

POWER SUPPLY AND DECOUPLING

The AD45048 can be powered with a good quality, well regulated, low noise supply anywhere in the range from +3 V to ±12.6 V. In order to optimize the AD45048 in standard ADSL CPE line driver applications (see Figure 8), power the amplifier with a well regulated 12 V supply. Careful attention should be paid to decoupling the power supply. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize the supply voltage ripple and power dissipation. A 0.1 µF MLCC decoupling capacitor(s) should be located no more than 1/8-inch away from the power supply pin(s). A large, usually tantalum, 10 µF to 47 µF capacitor is recommended to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the AD45048 outputs.

LAYOUT CONSIDERATIONS

As is the case with all high speed applications, careful attention to printed circuit board layout details prevents associated board parasitics from becoming problematic. Proper RF layout and printed circuit board design techniques are strongly recommended. The PCB should have a low impedance return path (or ground) to the supply. Removing the ground plane from all layers in the immediate area of the amplifier reduces stray capacitances. The signal routing should be short and direct in order to minimize the parasitic inductance and capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input traces should be kept as far apart as possible from the output traces to minimize coupling (crosstalk) though the board.

Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible in order to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This reduces the radiated energy and makes the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

CPE ADSL APPLICATION

The low cost, high output current dual AD45048 xDSL line driver amplifiers have been specifically designed to drive high fidelity xDSL signals to within 0.5 V of the power rails on a single 12 V supply. The AD45048 can be used in transformer-coupled bridge hybrid circuits designed to drive modulated signals, including discrete multitone (DMT), upstream to the central office.

TRANSFORMER SELECTION

Customer premise ADSL applications require the transmission of a 13 dBm DMT signal (20 mW into 100 Ω). DMT signals can have a crest factor (V peak/V rms ratio) as high as 5.3, requiring the line driver to provide a peak power of 560 mW. The line driver is required to drive a 7.5 V peak onto the 100 Ω telephone line while maintaining about −65 dBc to −70 dBc of MTPR. Since the maximum low distortion output swing available from the AD45048 line driver is approximately 11.5 V on a 12 V supply (depending on the load), and taking into account the power lost in the transformer and termination resistors, a step-up transformer with a minimum turns ratio of 1.5 or greater is needed. In the simplified differential driver circuit shown in Figure 8, the AD45048 is driving a 25 Ω impedance reflected by 1:2 step-up transformer. R3 and R6 are 12.5 Ω each and are back-termination or load-matching resistors whose values can be calculated by

$$(100\ \Omega/(N^2))/2$$

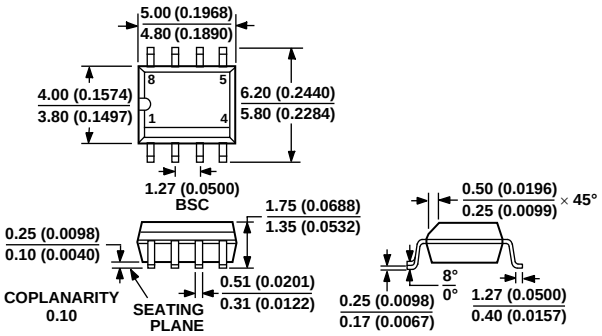
where 100 Ω is the approximate phone line impedance and N is the transformer turns ratio. In Figure 8, the total differential load including the termination resistors is 50 Ω, and under these conditions, the AD45048 is capable of driving low distortion signals to within 0.5 V of the power rails.

RECEIVE CHANNEL CONSIDERATIONS

A step-up transformer of N turns used at the output of the differential line driver increases the differential output voltage to the line (see Figure 8). However, the inverse effect is seen in the receive channel as the amplitude of signal on the driver side of the transformer is divided by N turns. The decision to use a particular transformer turns ratio may be impacted by the ability of the receive circuitry to resolve low level signals in the noisy twisted pair telephone plant. Higher turns ratio transformers reduce the effective receive channel SNR (signal-to-noise ratio) due to the reduction in the received signal strength.

An amplifier with low RTI noise, such as the AD8022 (2.5 nV/√Hz), is recommended for the receive channel. For a complete selection of amplifiers and other related components, see www.analog.com.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 15. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD45048AR	−40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8
AD45048AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8
AD45048AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8
AD45048ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8
AD45048ARZ-REEL[1]	−40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8
AD45048ARZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8

[1] Z = Pb-free part.

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