Revision history

Rev. No.	Approved date	History	Remark (purpose)
A	August 28 2001	Initial issue	Preliminary

Features

- 256Kx8-bit Organization
- Address Access Time:70, 90, 120, 150 ns
- Single 5V ± 10% Power Supply
- Sector Erase Mode Operation
- 16KB Boot Block (lockable)
- 512 bytes per Sector, 512 Sectors
  - Sector-Erase Cycle Time: 10ms (Max)
  - Byte-Write Cycle Time:20μs(Max)
- Minimum 10,000 Erase-Program Cycles
- Low power dissipation
  - Active Read Current:20mA (Typ)
  - Active Program Current:30mA (Typ)
  - Standby Current:100μA(Max).
- Hardware Data Protection
- Low VCC Program Inhibit Below 3.5V
- Self-timed write/erase operations with end-of-cycle detection
- DATA Polling
- Toggle Bit
- CMOS and TTL Interface
- Available version
  - LST28002 (Top Boot Block)

- **Packages**
  - 32-pin Plastic DIP
  - 32-pin TSOP-I
  - 32-pin PLCC

Description

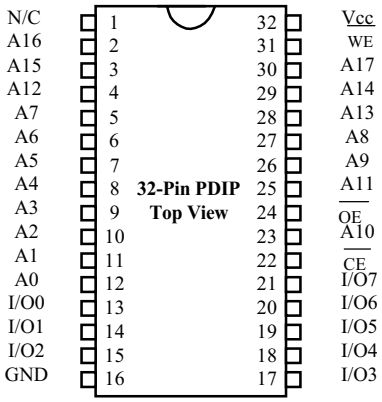
The LST28002 is a high-speed 262,144 × 8 bit CMOS flash memory. Writing or erasing the device is done with a single 5 Volt power supply. The device has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls to eliminate bus contention

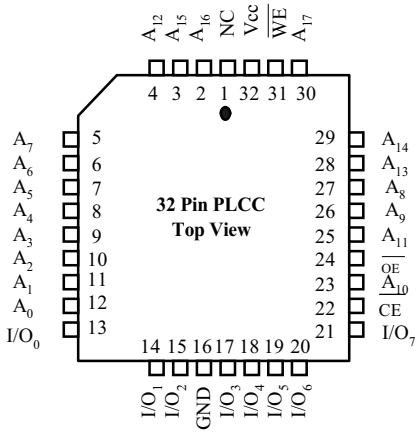
The LST28002 offers a combination of: Boot Black with Sector Erase/ Write Mode. The end of write/erase cycle is detected by $\overline{DATA}$ Polling of I/O_7 or by the Toggle Bit I/O_6.

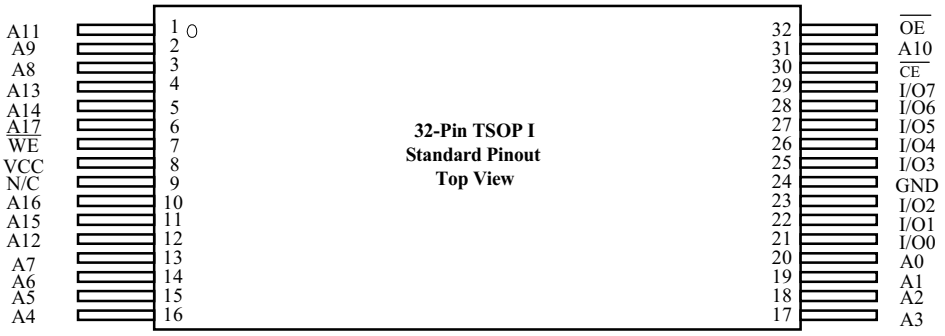
The LST28002 features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. The device also supports full chip erase.

Boot block architecture enables the Device to boot from a protected sector located either at the top (LST28002). All inputs and outputs are CMOS and TTL compatible. The LST28002 is ideal for applications that require updatable code and data storage.

Pin Configurations



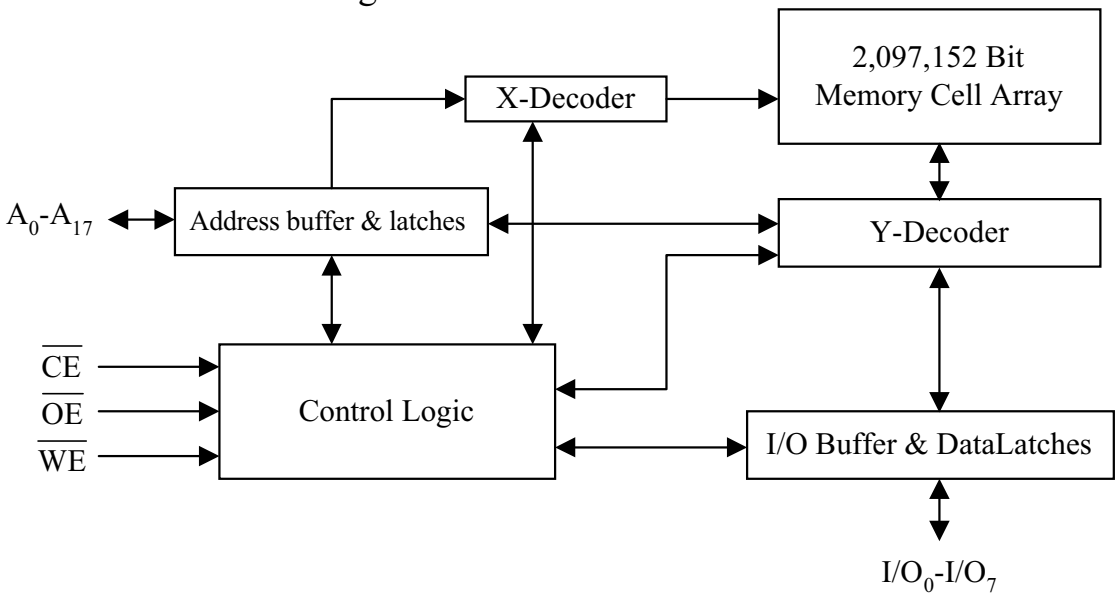




Pin Names

A_0-A_{17}	Address Inputs
I/O_0-I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	5V+10% Power Supply
GND	Ground
NC	No Connect

Functional Block Diagram



Capacitance (1,2)

Symbol	Parameter	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN}=0	8	10	pF

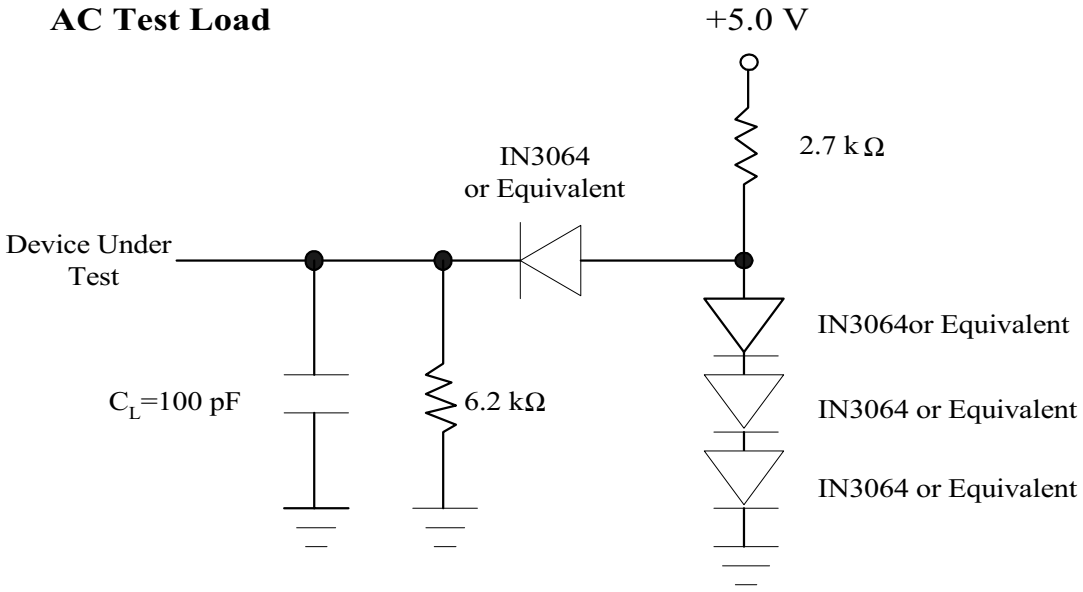
NOTE:
1. Capacitance is sampled and not 100% tested.
2. TA=25℃, V_{CC}=5V±10%, f=1MHz

Latch Up Characteristics(1)

Parameter	Min.	Max.	Unit
Input Voltage with Respect to GND on A_9, $\overline{OE}$	-1	+13	V
Input Voltage with Respect to GND on I/O, address or control pins	-1	Vcc +1	V
Vcc Current	-100	+100	mA

Note:
1. Includes all pins except Vcc. Test conditions:Vcc=5V, one pin at a time.

AC Test Load



Absolute Maximum Rating (1)

Symbol	Parameter	Commercial	Industrial	Unit
V_{IN}	Input Voltage (input or I/O pins)	-2 to +7	-2 to +7	V
V_{IN}	Input Voltage (A9 pin, $\overline{OE}$)	-2 to +13	-2 to +13	V
V_{CC}	Power Supply Voltage	-0.5 to +5.5	-0.5 to +5.5	V
T_{STG}	Storage Temperature (Plastic)	-65 to +125	-65 to +150	℃
T_{OPR}	Operating Temperature	0 to +70	-40 to +85	℃
I_{OUT}	Short Circuit Current(2)	200 (Max.)	200 (Max.)	mA

NOTE:
1. Stresses greater than those listed under "Absolute Maximum Ratings "may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. No more than one output maybe shorted at a time and not exceeding one second long.

DC Electrical Characteristics

(over all temperature ranges, Vcc=5V ±10%)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage(1.2)	Vcc=$Vcc^{Min.}$	-	0.8	V
V_{IH}	Input HIGH Voltage(0)	Vcc=$Vcc^{Max.}$	2	-	V
I_{IL}	Input Leakage Current	V_{IN} = GND to V_{cc} ,Vcc Max.	-	± 1	μA
I_{OL}	Output Leakage Current	V_{out} = GND to Vcc , Vcc = V_{CC} Max.	-5	±10	μA
V_{OL}	Output LOW Voltage	V_{CC}= VccMin , I_{OL} = 2.lmA	-	0.4	V
V_{OH}	Output HIGH Voltage	Vcc = Min ,I_{OH} = -lmA	2.4	-	V
I_{CC1}	Read Current	$\overline{CE}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH},all I/Os open, Address input = V_{IL}/V_{IH}, at f=1/t_{RC} Min., V_{CC}=V_{CC}Max.	-	40	mA
I_{CC2}	Write Current	$\overline{CE}$ = $\overline{WE}$ =VIL, $\overline{OE}$ =V_{IH}, V_{CC}=V_{CC}Max.	-	50	mA
I_{SB}	TTL Standby Current	$\overline{CE}$ = $\overline{OE}$ = $\overline{WE}$ =V_{IH},V_{CC}=V_{CC}Max.	-	2	mA
I_{SB1}	CMOS Standby Current	$\overline{CE}$ = $\overline{OE}$ = $\overline{WE}$ =V_{CC}-0.3V,V_{CC}=V_{CC}Max.	-	100	μA
V_H	Device ID Voltage for A9	$\overline{CE}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH}	11.5	12.5	V
I_H	Device ID Current for A9	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ =V_{IH}, A9=V_HMax	-	50	μA

AC Electrical Characteristics

(over all temperature ranges)

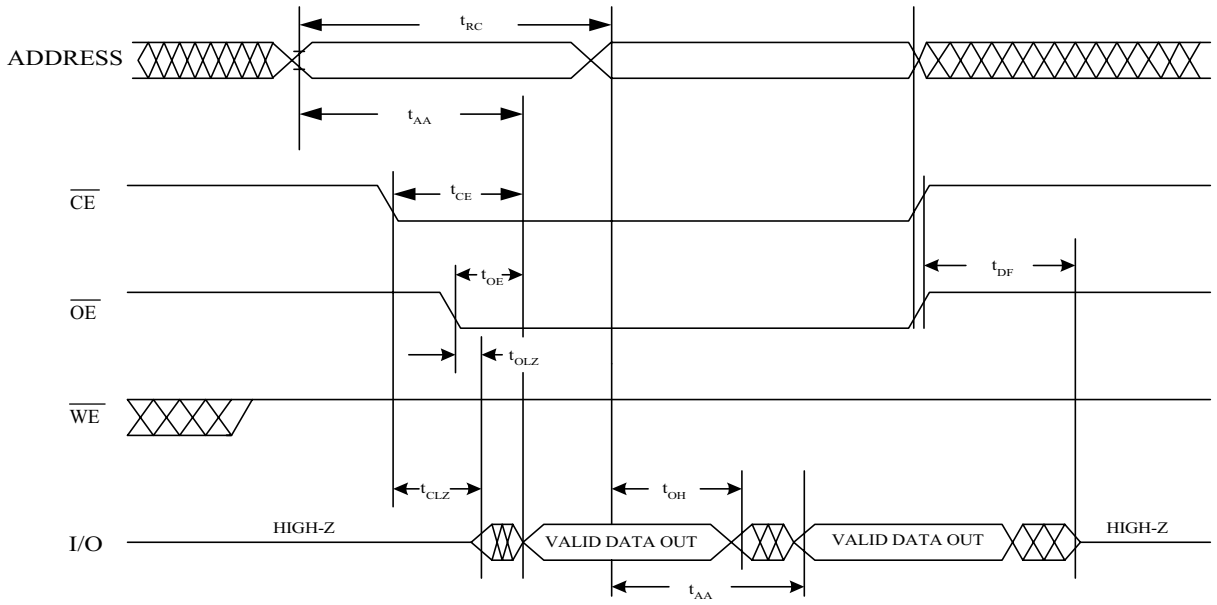
Read Cycle

Parameter Name	Parameter	-70		-90		-120		-150		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70	-	90	-	120	-	150	-	ns
t_{AA}	Address Access Time	-	70	-	90	-	120	-	150	ns
t_{ACS}	Chip Enable Access Time	-	70	-	90	-	120	-	150	ns
t_{OE}	Output Enable to Output Valid	-	35	-	45	-	60	-	75	ns
t_{CLZ}	$\overline{CE}$ Low to Output Active	0	-	0	-	0	-	0	-	ns
t_{OLZ}	$\overline{OE}$ Low to Output Active	0	-	0	-	0	-	0	-	ns
t_{DF}	$\overline{OE}$ or $\overline{CE}$ High to Output in High Z	0	30	0	40	0	50	0	60	ns
t_{OH}	Output Hold from Address Change	0	-	0	-	0	-	0	-	ns

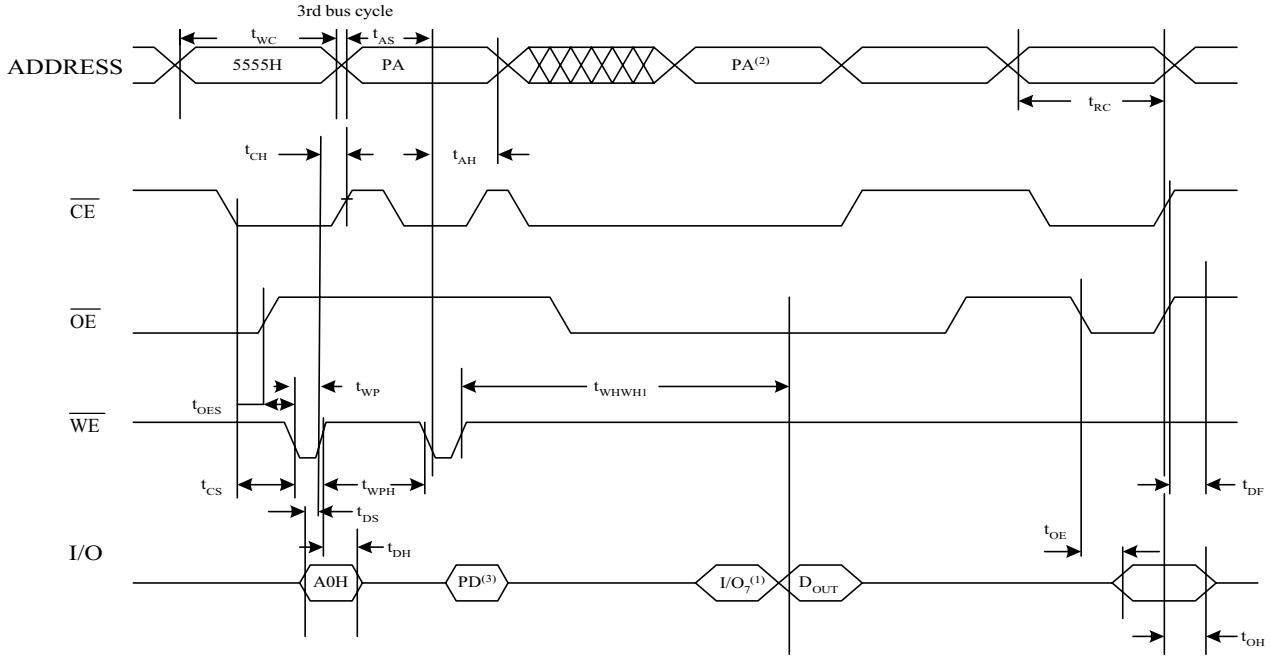
Program (Erase/Program) Cycle

Parameter Name	Parameter	-70			-90			-120			-150			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{WC}	Write Cycle Time	70	-	-	90	-	-	120	-	-	150	-	-	ns
t_{AS}	Address Setup Time	0	-	-	0	-	-	0	-	-	0	-	-	ns
t_{AH}	Address Hold Time	45	-	-	45	-	-	50	-	-	50	-	-	ns
t_{CS}	$\overline{CE}$ Setup Time	0	-	-	0	-	-	0	-	-	0	-	-	ns
t_{CH}	$\overline{CE}$ Hold Time	0	-	-	0	-	-	0	-	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	0			35			40			50			ns
t_{OEH}	$\overline{OE}$ High Hold Time	0	-	-	0	-	-	0	-	-	0	-	-	ns
t_{WP}	$\overline{WE}$ Pulse Width	35	-	-	45	-	-	50	-	-	50	-	-	ns
t_{WPH}	$\overline{WE}$ Pulse Width High	20	-	-	30	-	-	35	-	-	35	-	-	ns
t_{DS}	Data Setup Time	30	-	-	30	-	-	30	-	-	30	-	-	ns
t_{DH}	Data Hold Time	0	-	-	0	-	-	0	-	-	0	-	-	ns
t_{WHWH1}	Programming Cycle	-	-	20	-	-	20	-	-	20	-	-	20	μs
t_{WHWH2}	Sector Erase Cycle	-	-	10	-	-	10	-	-	10	-	-	10	ms
t_{WHWH3}	Chip Erase Cycle	-	2	-	-	2	-	-	2	-	-	2	-	sec

Waveforms of Read Cycle

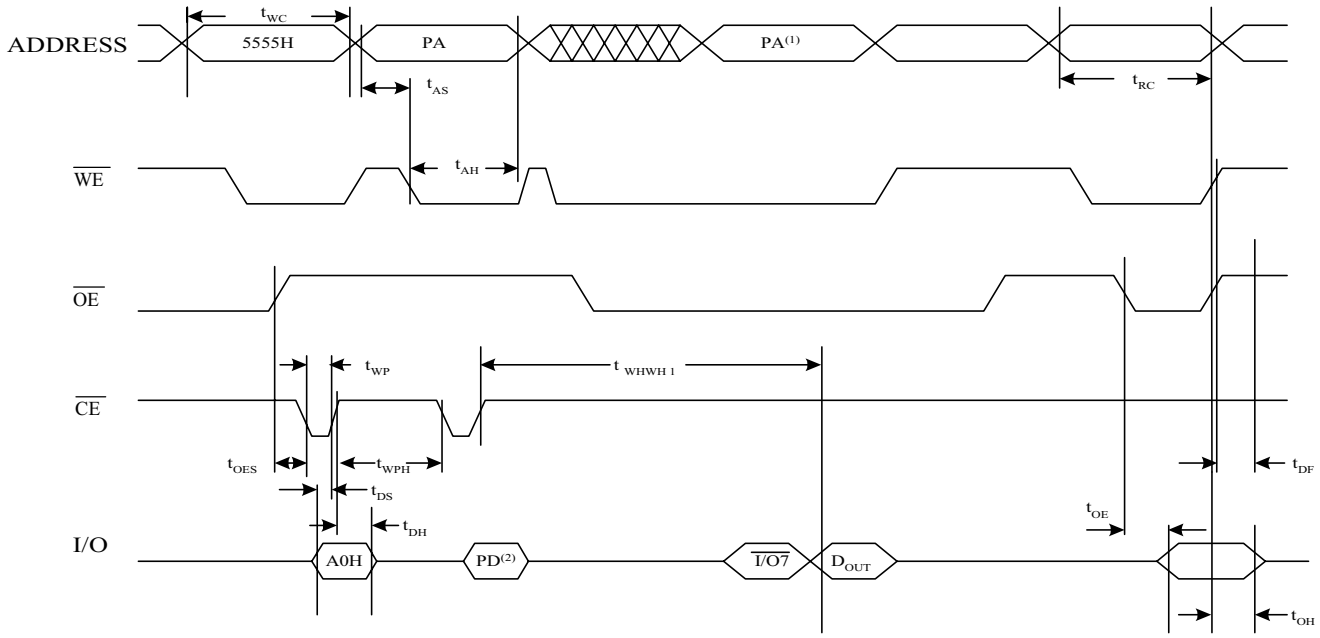


Waveforms of $\overline{WE}$ Controlled-Program Cycle

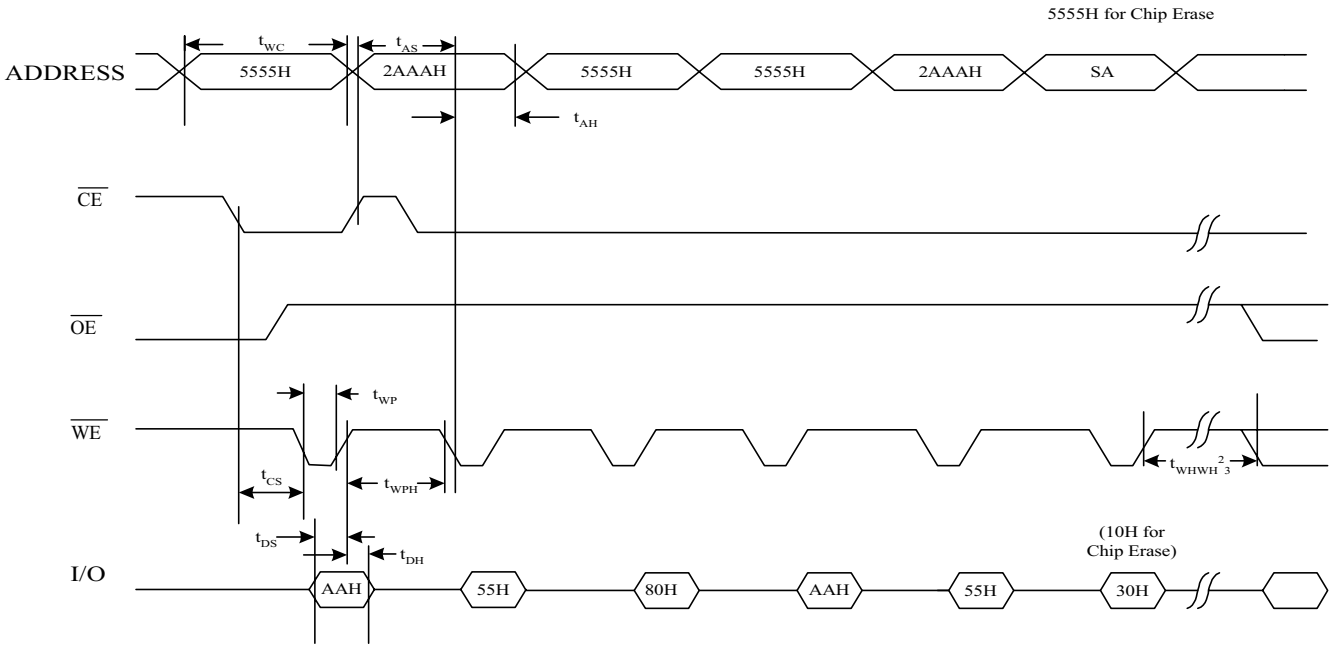


NOTES:
1. I/O_7: The output is the complement of the data written to the device.
2. PA: The address of the memory location to be programmed.
3. PD: The data at the byte address to be programmed.

Waveforms of CE Controlled-Program Cycle

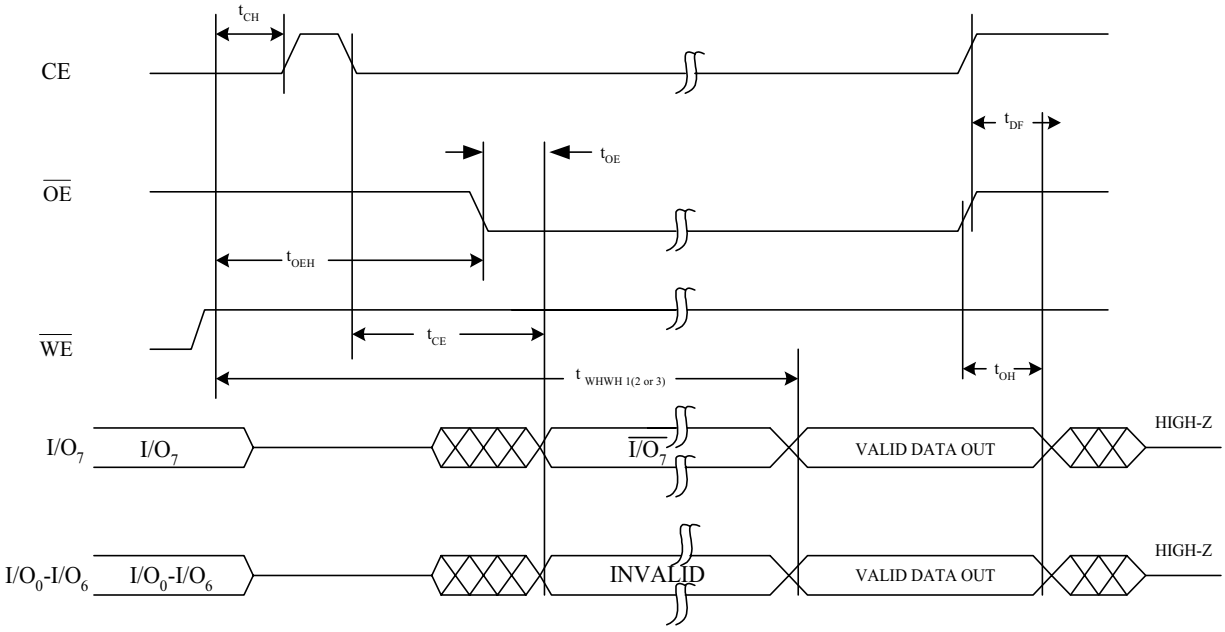


Waveforms of Erase Cycle(1)

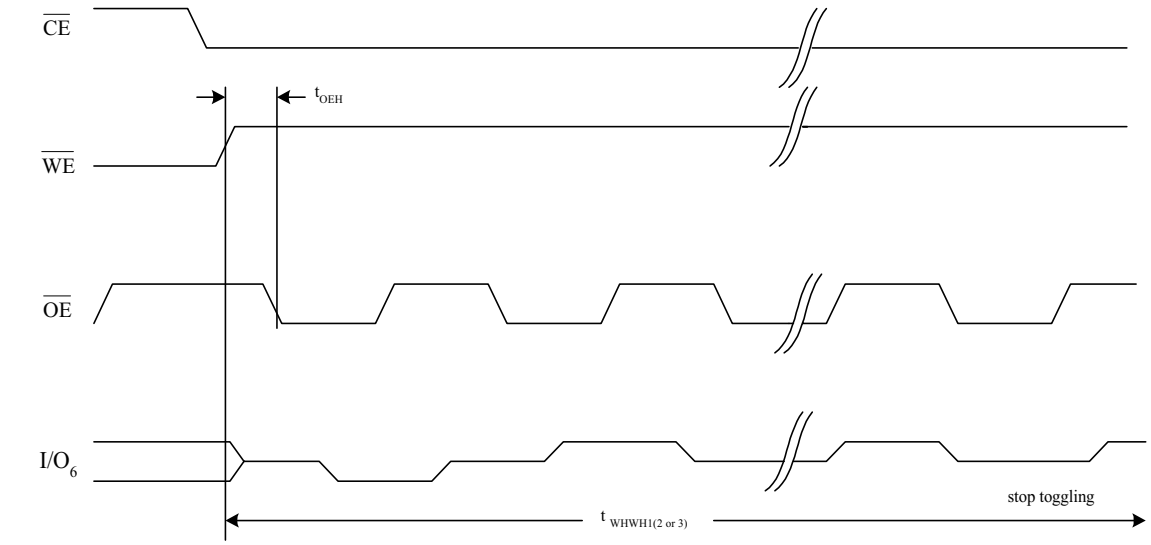


NOTES:
1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.
3. SA: The sector address for Sector Erase.

Waveforms of $\overline{\text{DATA}}$ Polling Cycle



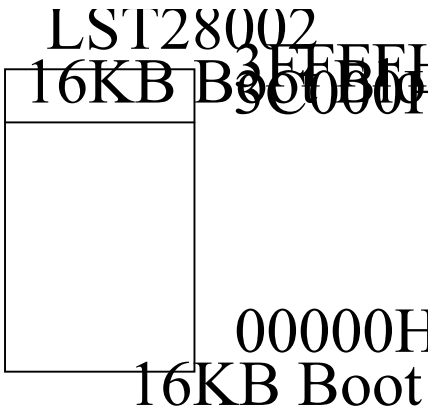
Waveforms of Toggle Bit Cycle



Functional Description

The LST28002 consists of 512 equally-sized sectors of 512 bytes each. The 16KB lockable Boot Block is intended for storage of the system BIOS boot code The boot code is the first piece of code executed each time the system is powered on or rebooted.

The LST28002 is available in the Boot Block address starting from 3C000H to 3FFFFH.



Read Cycle

A read cycle is performed by holding both $\overline{CE}$ and $\overline{OE}$ signals LOW. Data Out becomes valid only when these conditions are met. During a read cycle $\overline{WE}$ must be HIGH prior to $\overline{CE}$ and $\overline{OE}$ going LOW. $\overline{WE}$ must remain HIGH during the read operation for the read to complete (See Table1).

Output Disable

Returning $\overline{OE}$ or $\overline{CE}$ HIGH, whichever occurs first will terminate the read operation and place the I/O pins in the HIGH-Z state.

Standby

The device will enter standby mode when the $\overline{CE}$ signal is HIGH. The I/O pins are placed in the HIGH-Z, independent of the $\overline{OE}$ input state.

Byte Write Cycle

The LST28002 is programmed on a byte-by-byte basis. The byte write operation is initiated by using a specific four-bus-cycle sequence: two unlock program cycles, a program setup command and program data program cycles (see Table 2).

During the byte write cycle, addresses are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever is last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The byte write cycle can be $\overline{CE}$ controlled or $\overline{WE}$ controlled.

Sector Erase Cycle

The LST28002 features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. Sector erase operation is initiated by using a specific six-bus-cycle sequence: Two unlock program cycles, a setup command, two additional unlock program cycles, and the sector erase command (See Table 2). A sector must be first erased before it can be rewritten. While in the internal erase mode, the device ignores any program attempt into the device. The internal erase completion can be determined via DATA polling or toggle bit status.

The LST28002 is shipped fully erased (all bits =1)

Table 1. Operation Modes Decoding

Decoding Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	**A_0**	**A_1**	**A_9**	**I/O**
Read	V_{IL}	V_{IL}	V_{IH}	A_0	A_1	A_9	READ
Byte Write	V_{IL}	V_{IH}	V_{IL}	A_0	A_1	A_9	PD
Standby	V_{IH}	X	X	X	X	X	HIGH-Z
Autoselect Device ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_H	CODE
Autoselect Manufacture ID	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_H	CODE
Enabling Boot Block Protection Lock	V_{IL}	V_H	V_{IL}	X	X	V_H	X
Disabling Boot Block Protection Lock	V_H	V_H	V_{IL}	X	X	V_H	X
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	HIGH-Z

Table 2. Command Codes

Command Sequence	**First Bus Program Cycle**		**Second Bus Program Cycle**		**Third Bus Program Cycle**		**Fourth Bus Program Cycle**		**Fifth BUS Program Cycle**		**Six BUS Program Cycle**	
	Address	**Data**	**Address**	**Data**	**Address**	**Data**	**Address**	**Data**	**Address**	**Data**	**Address**	**Data**
Read	XXXXH	F0H										
Read	5555H	AAH	2AAAH	55H	5555H	F0H	RA(1)	RD(2)				
Autoselect Mode	5555H	AAH	2AAAH	55H	5555H	90H	See table 3 for detail.					
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	PA(3)	PD(4)				
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA(5)	30H

NOTES:

1. RA: Read Address
2. RD: Read Data
3. PA: The address of the memory location to be programmed.
4. PD: The data at the byte address to be programmed.
5. SA(5): Sector Address

Chip Erase Cycle

The LST28002 features a chip erase operation. The chip erase operation is initiated by using a specific six-bus-cycle sequence: two unlock program cycles, a setup command, two additional unlock program cycles, and the chip erase command (see Table 2).

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when the data on DQ7 is "1".

Program Cycle status Detection

There are two methods for determining the state of the LST28002 during a program (erase/write) cycle: $\overline{DATA}$ Polling (I/O_7) and Toggle Bit (I/O_6).

$\overline{DATA}$ Polling (I/O_7)

The LST28002 features $\overline{DATA}$ Polling to indicate the end of a program cycle. When the device is in the program cycle, any attempt to read the device will received the complement of the loaded data on I/O_7. Once the program cycle is completed, I/O_7 will show true data , and the device is then ready for the next cycle.

Boot Block Protection Status

In Autoselect mode, performing a read at address location 3CXX2H (LST28002) will indicate boot block protection status. If the data is 00H, the boot block is unprotected. This is also shown is table 3.

Device ID

In Autoselect mode, performing a read at address XXX1H will determine whether the device is a TOP Boot Block device. The data is 02H, the device is a Top Boot Block. (See Table 3).

Toggle Bit (I/O_6)

The LST28002 also features another method for determining the end of a program cycle. When the device is in the program cycle, any attempt to read the device will result in I/O6 toggling between 1 and 0. Once the program is completed, the toggling will stop. The device is then ready for the next operation. Examining the toggle bit may begin at any time during a program cycle.

Boot Block Protection Enabling/Disabling

The LST28002 features hardware Boot Block Protection. The boot block sector protection is enabled when high voltage (12.5V) is applied to $\overline{OE}$ and A9 pins with $\overline{CE}$ pin LOW and $\overline{WE}$ pin LOW. The sector protection is disabled when high voltage is applied to $\overline{OE}$, $\overline{CE}$ and A9 pins with $\overline{WE}$ pin LOW. Other pins can be HIGH or LOW. This is shown in table 1.

Autoselect Mode

The LST28002 features an Autoselect mode to identify boot block locking status, device ID and manufacturer ID.

Entering Autoselect mode is accomplished by applying a high voltage (VH) to the A9 Pin, or through a sequence of commands (as shown in table 2). Device will exit this mode once high voltage on A9 is removed or another command is loaded into the device.

Manufacturer ID

In Autoselect mode, performing a read at address XXXX0H will determine the manufacturer ID. 40H is the manufacturer code for LinkSmart OEM code.

Hardware Data Protection

Vcc Detection: the program operation is inhibited when VCC is less than 3.5V.

Noise Protection: a CE or WE pulse of less than 5ns will not initiate a program cycle.

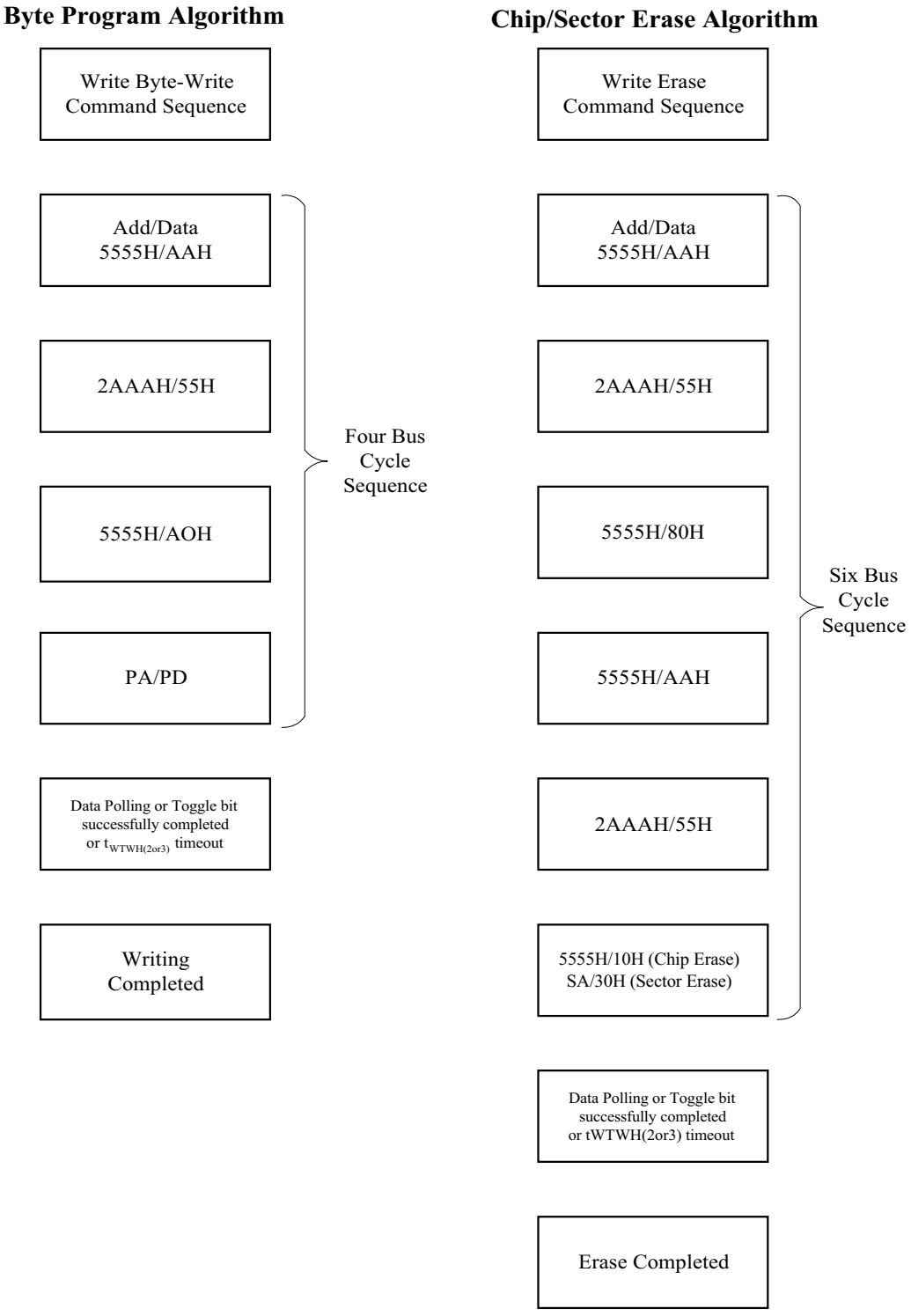
Program Inhibit: Holding any one of $\overline{OE}$ LOW, $\overline{CE}$ HIGH or $\overline{WE}$ HIGH inhibits a program cycle.

Table 3. Autoselect Decoding

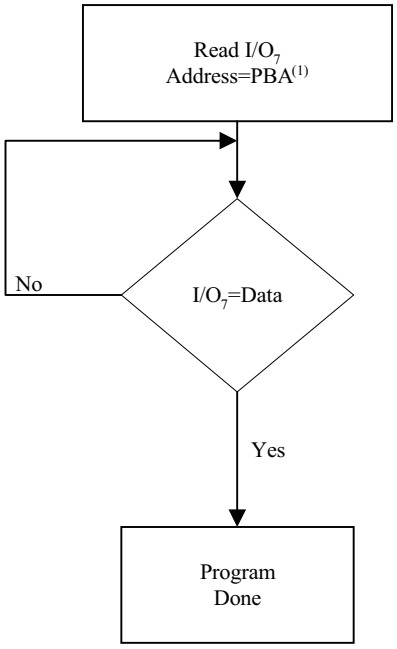
Decoding Mode	Address				Data I/O_0-I/O_7
	A0	A1	A2-A13	A14-A17	
Boot Block Protection	V_{IL}	V_{IH}	X	V_{IH}	01H: protected
Device ID	V_{IH}	V_{IL}	X	X	02H
Manufacture ID	V_{IL}	V_{IL}	X	X	40H

NOTE:

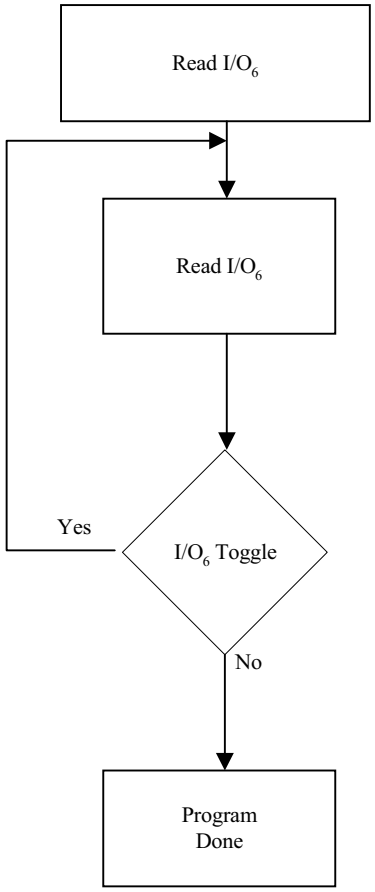
1. X= Don't Care, V_{IH}=HIGH, V_{IL}=LOW.


Byte Program Algorithm
Write Byte-Write Command Sequence
Add/Data 5555H/AAH
2AAAH/55H
5555H/AOH
PA/PD
Four Bus Cycle Sequence
Data Polling or Toggle bit successfully completed or tWTWH(2or3) timeout
Writing Completed
Chip/Sector Erase Algorithm
Write Erase Command Sequence
Add/Data 5555H/AAH
2AAAH/55H
5555H/80H
5555H/AAH
2AAAH/55H
5555H/10H (Chip Erase) SA/30H (Sector Erase)
Six Bus Cycle Sequence
Data Polling or Toggle bit successfully completed or tWTWH(2or3) timeout
Erase Completed

DATA Polling Algorithm

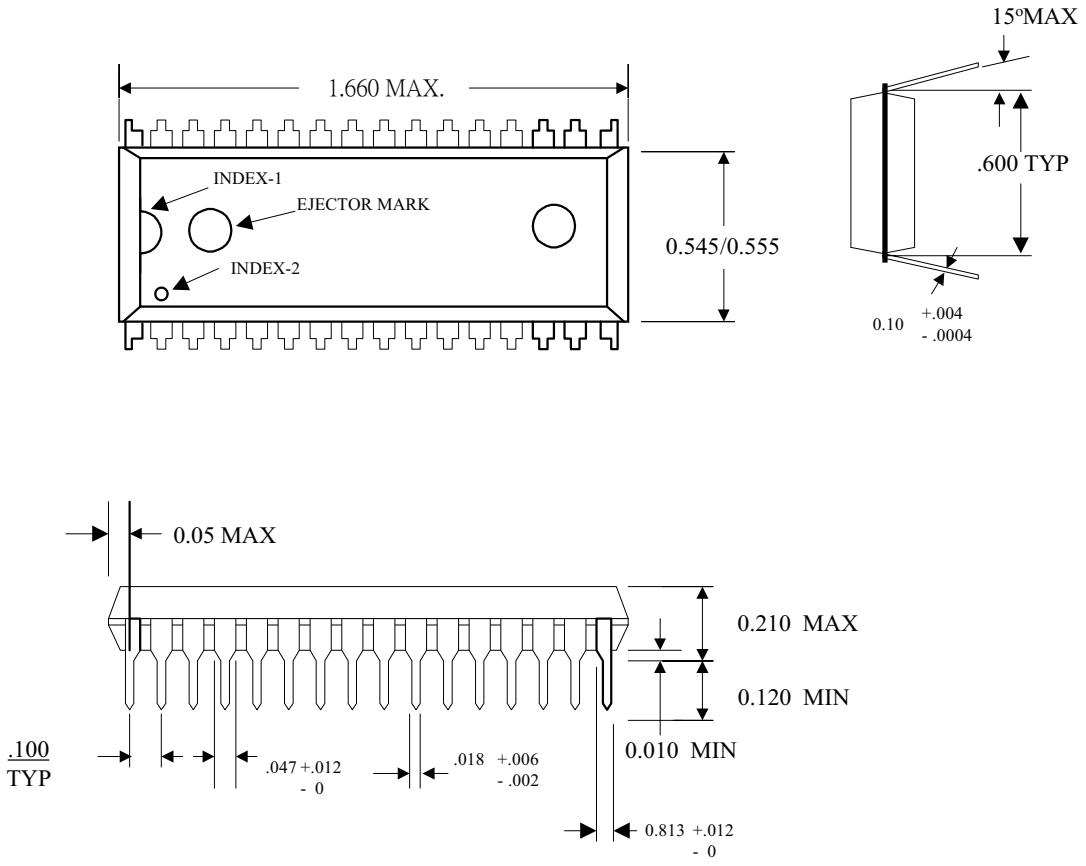


Toggle Bit Algorithm

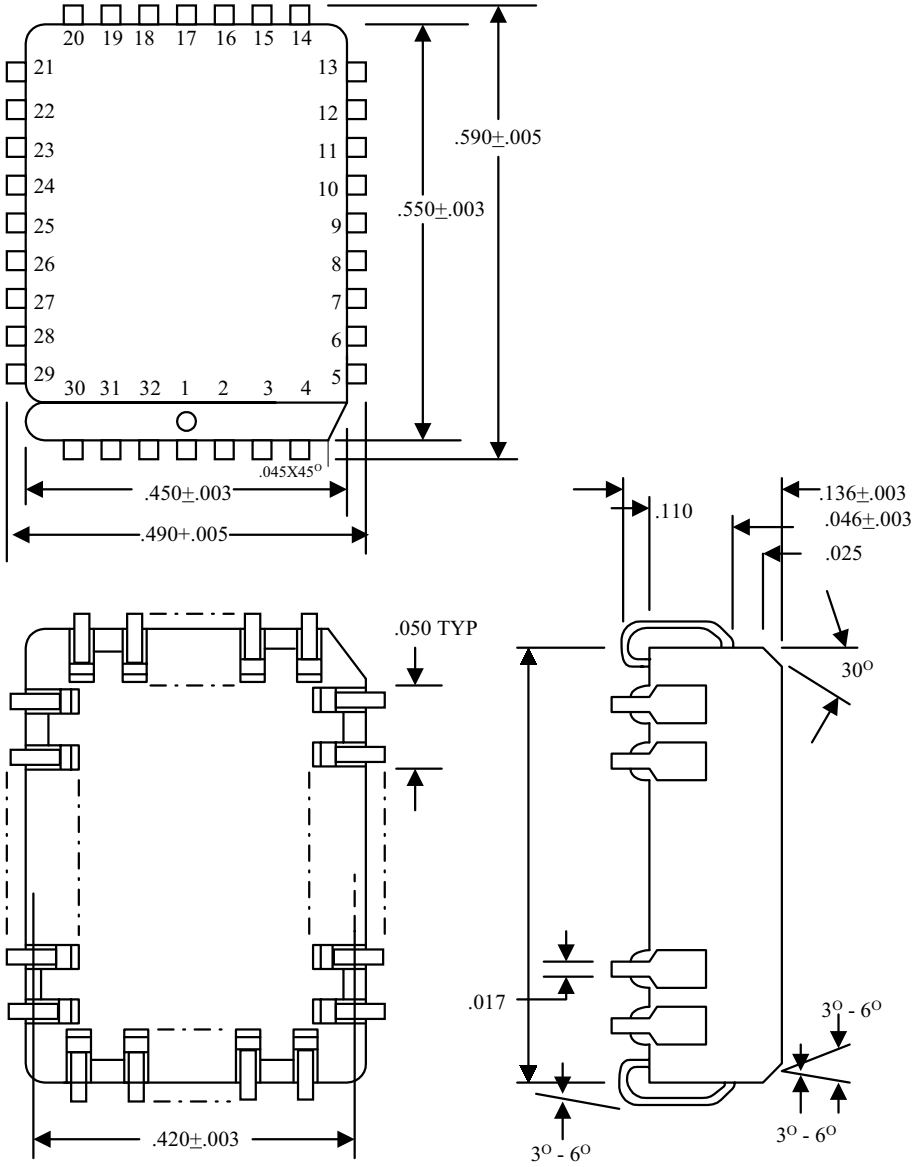


NOTE:
1. PBA: The byte address to be programmed.

32-pin Plastic DIP



32-pin PLCC


20 19 18 17 16 15 14
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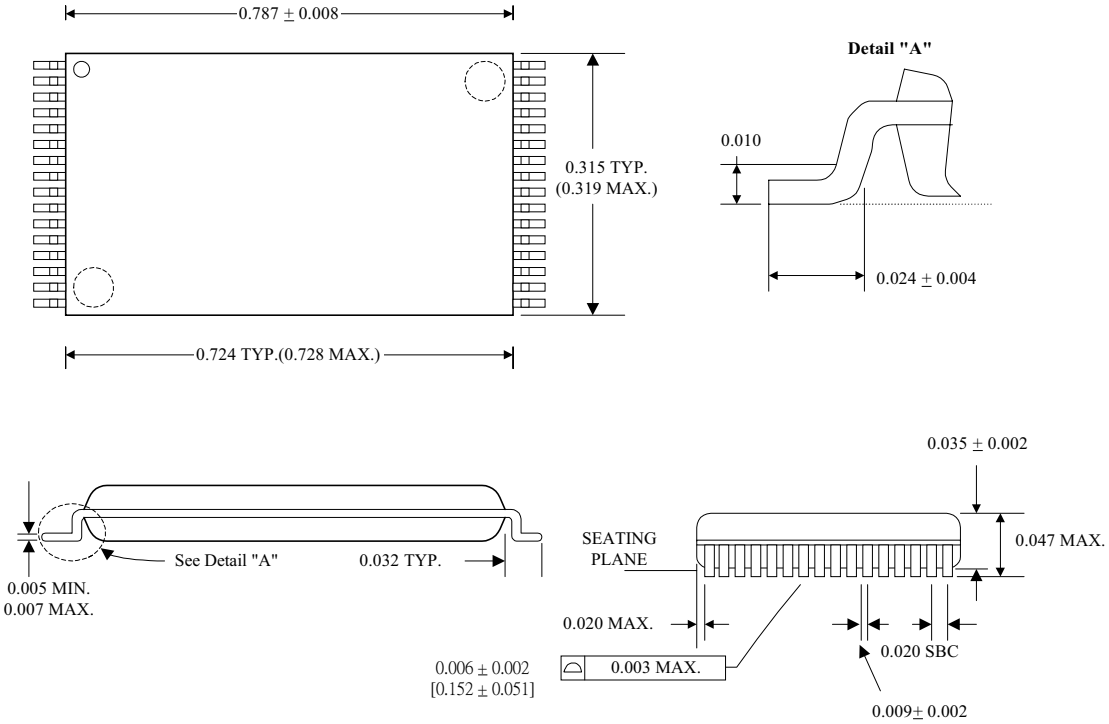
30 31 32 1 2 3 4
.590±.005
.550±.003
.045X45°
.450±.003
.490+.005
.050 TYP
.420±.003
.110
.136±.003
.046±.003
.025
30°
.017
3° - 6°
3° - 6°
3° - 6°

32-Pin TSOP-I

Units in inches [mm]



Part Number Information