Data Sheet

SAA7378GP

Single Chip Digital Servo Processor and Compact Disc Decoder

(CD7)

Preliminary specification: Version 1.0 **May1995**

1. FEATURES

- Single speed mode.
- Full error correction strategy, t = 2 and e = 4.
- All standard decoder functions implemented digitally on chip.
- FIFO overflow concealment for rotational shock resistance.
- Digital audio interface (EBU), audio only.
- 2 - 4 times oversampling integrated digital filter.
- Audio data peak level detection.
- Kill interface for DAC deactivation during digital silence.
- All TDA1301 (DSIC2) digital servo functions, plus extra hi-level functions.
- Low focus noise.
- Communication via TDA1301/SAA7345 compatible bus.
- On chip clock multiplier allows the use of 8.4672MHz crystal.

2. GENERAL DESCRIPTION

CD7 (SAA7378GP) is a single chip combining the functions of a CD decoder IC and Digital Servo IC. The decoder part is based on CD6 (SAA7345GP) with an improved error correction strategy; the servo part is based on DSIC2 (TDA1301T) with improvements incorporated.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	supply voltage	3.4	5.0	5.5	V
I_{DD}	supply current	-	49	-	mA
f_{XTAL}	crystal frequency	8	8.4672	35	MHz
T_{amb}	operating ambient temperature	5	-	+70	°C
T_{stg}	storage temperature	-55	-	+125	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7378GP	64	QFP	plastic	SOT393-1

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the " *Quality Reference Pocketbook*" are followed. The pocketbook can be ordered using the code 9398 510 34011.

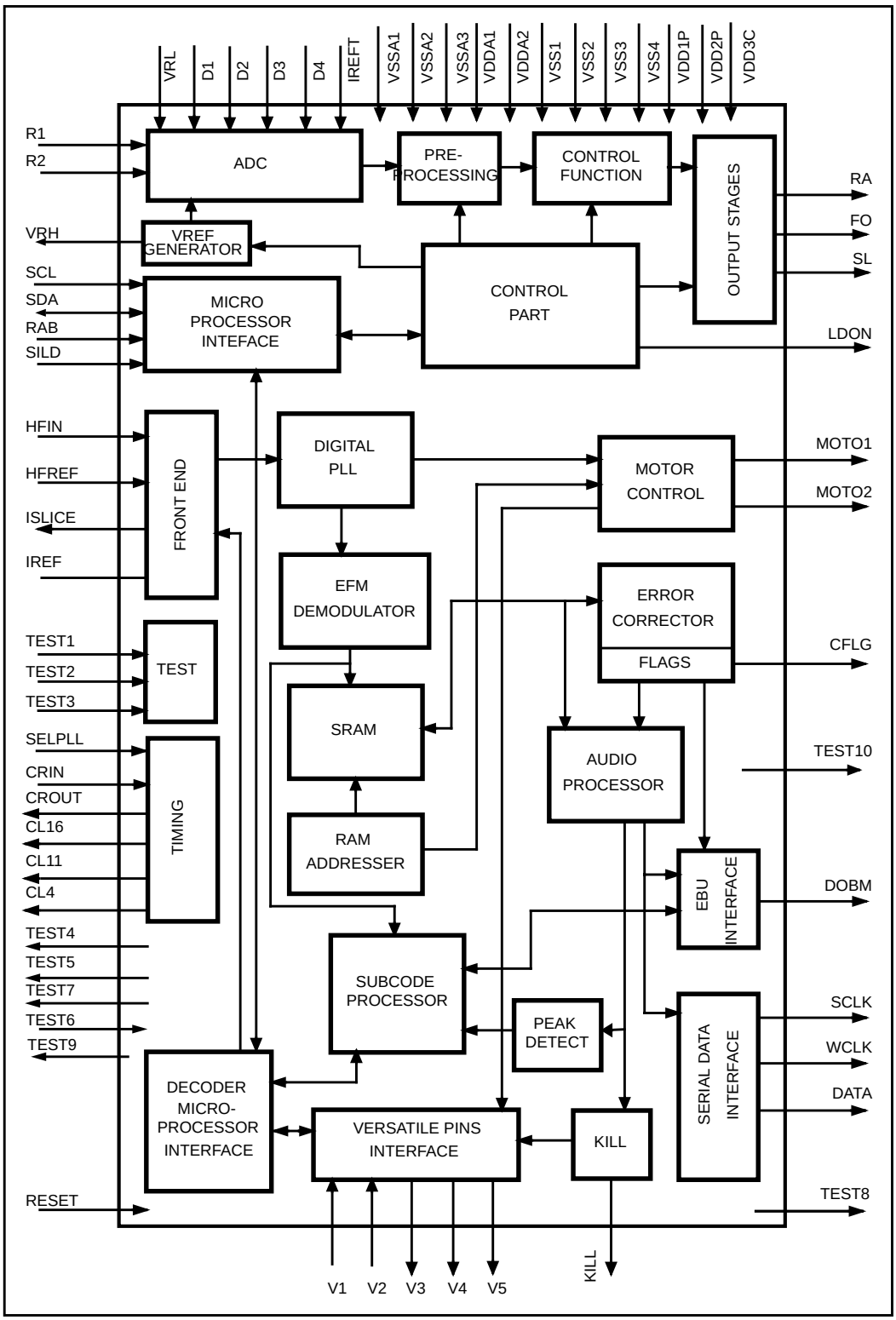


Figure 1 Functional Block Diagram

5. PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
$V_{SSA}1$	1	analogue supply*
$V_{DDA}1$	2	analogue supply*
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
IREFT	10	current reference for calibration ADC
V_{RH}	11	reference output from ADC
$V_{SSA}2$	12	analogue supply*
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback from data slicer
HFIN	15	comparator signal input
$V_{SSA}3$	16	analogue supply*
HFREF	17	comparator common mode input
IREF	18	reference current pin (nominally $V_{DD}/2$)
$V_{DDA}2$	19	analogue supply*
TEST1	20	test control input; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 MHz or 5.6448MHz clock output (tri-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input; this pin should be tied LOW
$V_{DD}1_P$	30	digital supply periphery*
DOBM	31	bi-phase mark output (externally buffered) (tri-state)
$V_{SS}1$	32	digital supply*
MOTO1	33	motor output 1; versatile (tri-state)
MOTO2	34	motor output 2; versatile (tri-state)
TEST4	35	test output pin; this pin should be left unconnected
TEST5	36	test output pin; this pin should be left unconnected

SYMBOL	PIN	DESCRIPTION
TEST6	37	test input; this pin should be tied LOW
TEST7	38	test output pin; this pin should be left unconnected
$V_{SS}2$	39	digital supply*
V5	40	versatile output pin
V4	41	versatile output pin
V3	42	versatile output pin (open drain)
KILL	43	kill output - programmable (open drain)
TEST8	44	test output pin; this pin should be left unconnected
DATA	45	serial data output (tri-state)
WCLK	46	word clock output (tri-state)
$V_{DD}2_P$	47	digital supply periphery*
SCLK	48	serial bit clock output (tri-state)
$V_{SS}3$	49	digital supply*
CL4	50	4.2336 MHz µP clock output
SDA	51	µP interface data I/O line (open drain output)
SCL	52	µP interface clock line
RAB	53	µP interface R/$\overline{W}$ and load control line
SILD	54	µP interface $\overline{R}$/W and load control line
N/C	55	No connection
$V_{SS}4$	56	digital supply*
RESET	57	power-on reset input (active low)
TEST9	58	test output pin; this pin should be left unconnected
$V_{DD}3_C$	59	digital supply core*
TEST10	60	test output pin; this pin should be left unconnected
CFLG	61	correction flag output (open drain)
V1	62	versatile input pin
V2	63	versatile input pin
LDON	64	laser drive on output (open drain)

* Note: All supply pins must be connected to the same external power supply voltage.

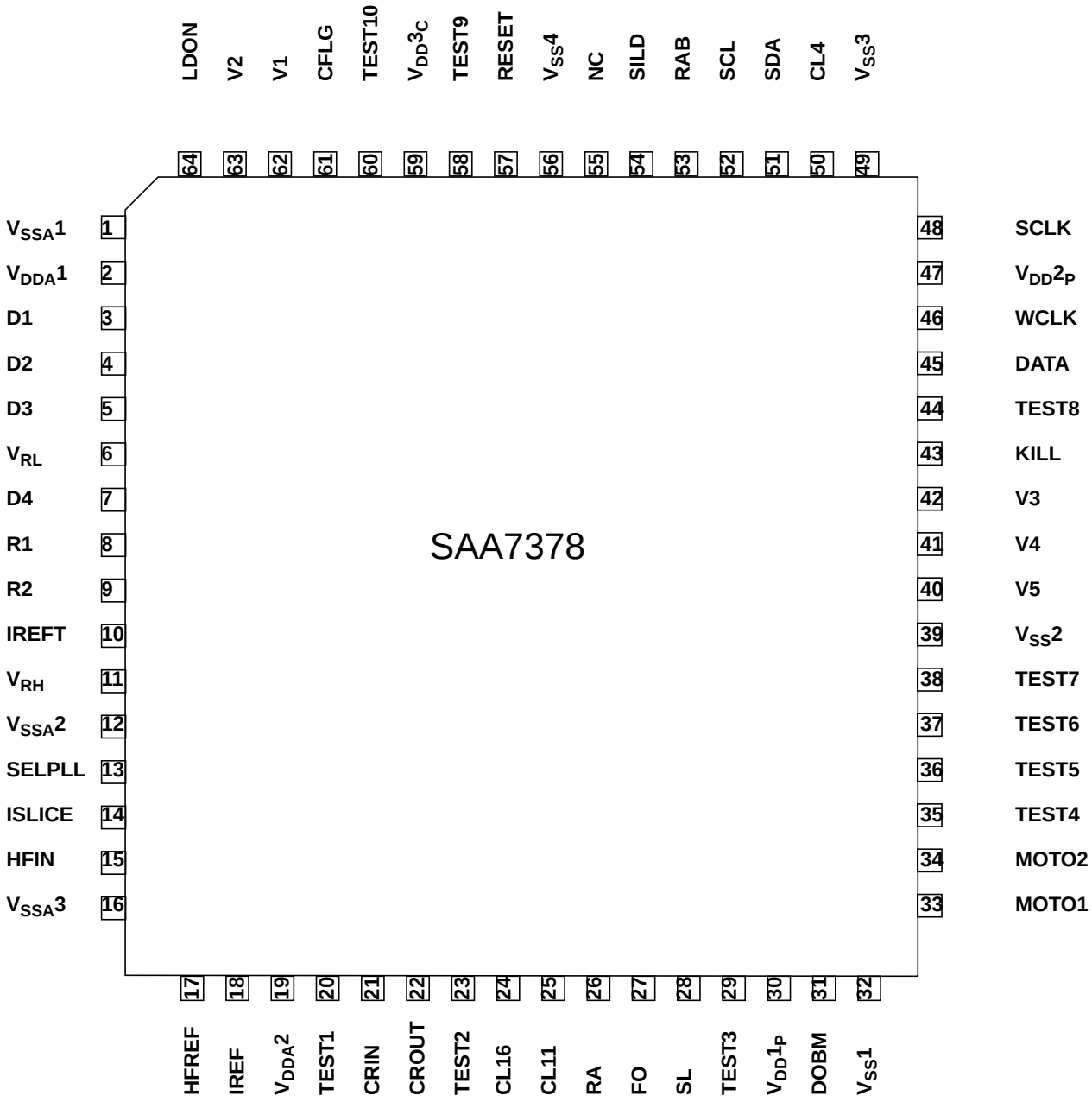


Figure 2 Pinning Diagram

6. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	supply voltage	note 1	-0.5	+6.5	V
$V_{I(max)}$	maximum Input voltage (any input)		-0.5	V_{DD} + 0.5	V
V_O	Output voltage (any output)		-0.5	+6.5	V
VDD_{DIFF}	Difference between V_{DDA} and V_{DDD}			± 0.25	V
I_O	Output current (continuous)			± 20	mA
I_{IK}	DC input diode current (continuous)			± 20	mA
T_{amb}	operating ambient temperature		5	+70	°C
T_{stg}	storage temperature		-55	+125	°C
V_{es1}	electrostatic handling	note 2	-2000	+2000	V
V_{es2}	electrostatic handling	note 3	-200	+200	V

Notes: 1) All VDD and VSS connections must be made externally to the same power supply.

2) Equivalent to discharging a 100pF capacitor via a 1.5kΩ series resistor with a rise time of 15ns.

3) Equivalent to discharging a 200pF capacitor via a 2.5µH series inductor.

7. FUNCTIONAL DESCRIPTION OF THE DECODER PART

7.1 Principle Operation Modes of the Decoder Part

The decoding part operates at single speed and supports a full audio specification.

A simplified data flow through the decoder part is shown in Figure 5.

7.1.1 Crystal Frequency Selection

The SAA7378 which has an internal phase locked loop clock multiplier, can be used with 33.8688, 16.9344 or 8.4672MHz crystal frequencies by setting register B and SELPLL as shown below.

Register B	SELPLL	crystal frequency (MHz)
00xx	0	33.8688
00xx	1	8.4672
01xx	0	16.9344

The internal clock multiplier, controlled by SELPLL, should only be used if an 8.4672MHz crystal, ceramic resonator or external clock is present.

Note: The CL11 output is a 5.6448MHz clock if a 16.9344MHz external clock is used.

7.1.2 Standby Modes

The SAA7378 may be placed in two standby modes, (Note that the device core is still active), selected by register B :

Standby 1 : "CD-STOP" mode. Most I/O functions are switched off.

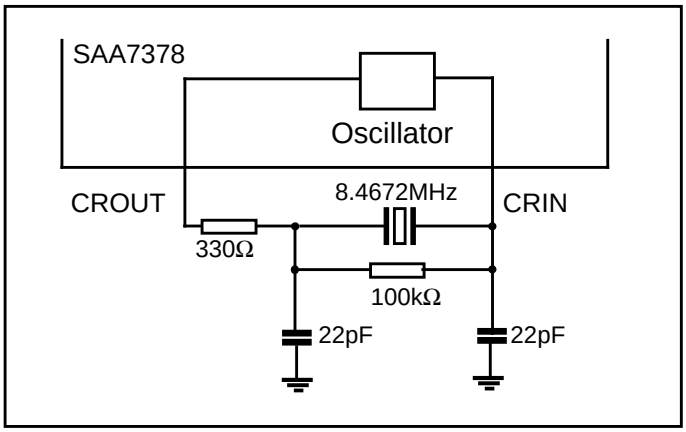
Standby 2: "CD-PAUSE" mode. Audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active. This is also called a "Hot Pause".

In the standby modes the various pins will have following values:

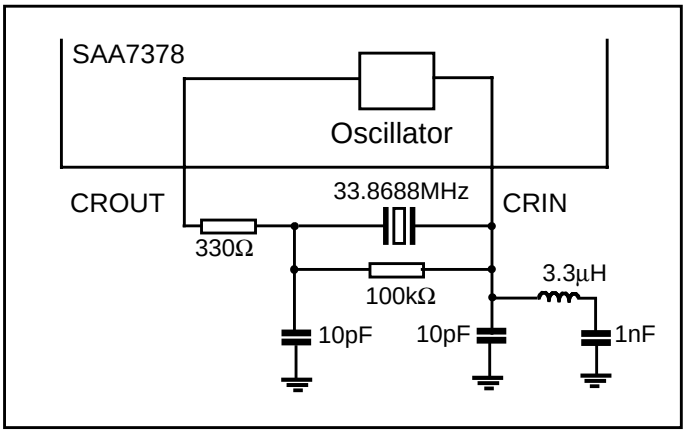
MOTO1, MOTO2:	Put in Hi-z, PWM mode (standby 1 and reset : operating in standby 2). Put in Hi-z, PDM mode (standby1 and reset: operating in standby 2).
SCL,SDA, SILD, RAB:	No interaction. Normal operation continues.
SCLK, WCLK, DATA, CL11, DOBM:	Tri-state in both standby modes. Normal operation continues after reset.
CRIN, CROUT, CL16, CL4:	No interaction. Normal operation continues.
V1, V2, V3, V4, V5, CFLG:	No interaction. Normal operation continues.

7.2 Crystal Oscillator

The crystal oscillator is a conventional 2 pin design operating at 8 MHz to 35 MHz. This oscillator is capable of working with ceramic resonators as well as with both fundamental and third overtone crystals. External components should be used to suppress the fundamental output of the third overtone crystals as shown below in Figure 3. Typical oscillation frequencies required are 8.4672MHz, 16.9344MHz or 33.8688MHz depending on the internal clock settings used and whether or not the clock multiplier is enabled.



8.4672MHz Fundamental Configuration



33.8688MHz 3rd Overtone Configuration

Figure 3 Crystal Oscillator Circuits

7.3 Data Slicer and Clock Regenerator

The SAA7378 has an integrated slice level comparator which can be clocked by the crystal frequency clock, or 8 times the crystal frequency clock (if SELPLL is set high while using an 8.4672MHz crystal, and register 4 is set to **0xxx**). The slice level is controlled by an internal current source applied to an external capacitor under the control of the Digital Phase-Locked Loop (DPLL).

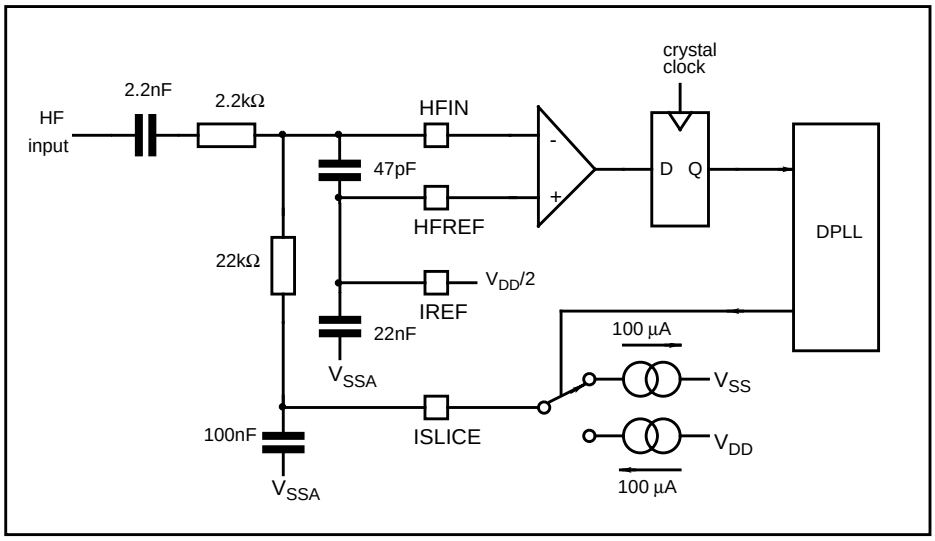


Figure 4 Data Slicer Showing Typical Application Components

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization.

For certain applications an *offtrack* input is necessary. This is internally connected from the servo part (its polarity can be changed by the *foc_parm1* parameter), but may be input via the V1 pin if selected by register C. If this flag is high, the SAA7378 will assume that its servo part is following on the wrong track, and will flag all incoming HF data as incorrect.

7.4 Demodulator

7.4.1 Frame Sync Protection

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data. The master counter is only reset if:

- a sync coincidence detected; sync pattern occurs 588 ± 1 EFM clocks after the previous sync pattern.
- a new sync pattern is detected within ± 6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active high after 1 sync coincidence found, and reset low if during 61 consecutive frames no sync coincidence is found. The PLL lock signal can be accessed via the SDA or STATUS pins selected by register 2 and 7.

Also incorporated in the demodulator is a RL2 (Run Length 2) correction circuit. Every symbol detected as RL2 will be pushed back to RL3. To do this the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

7.4.2 EFM Demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

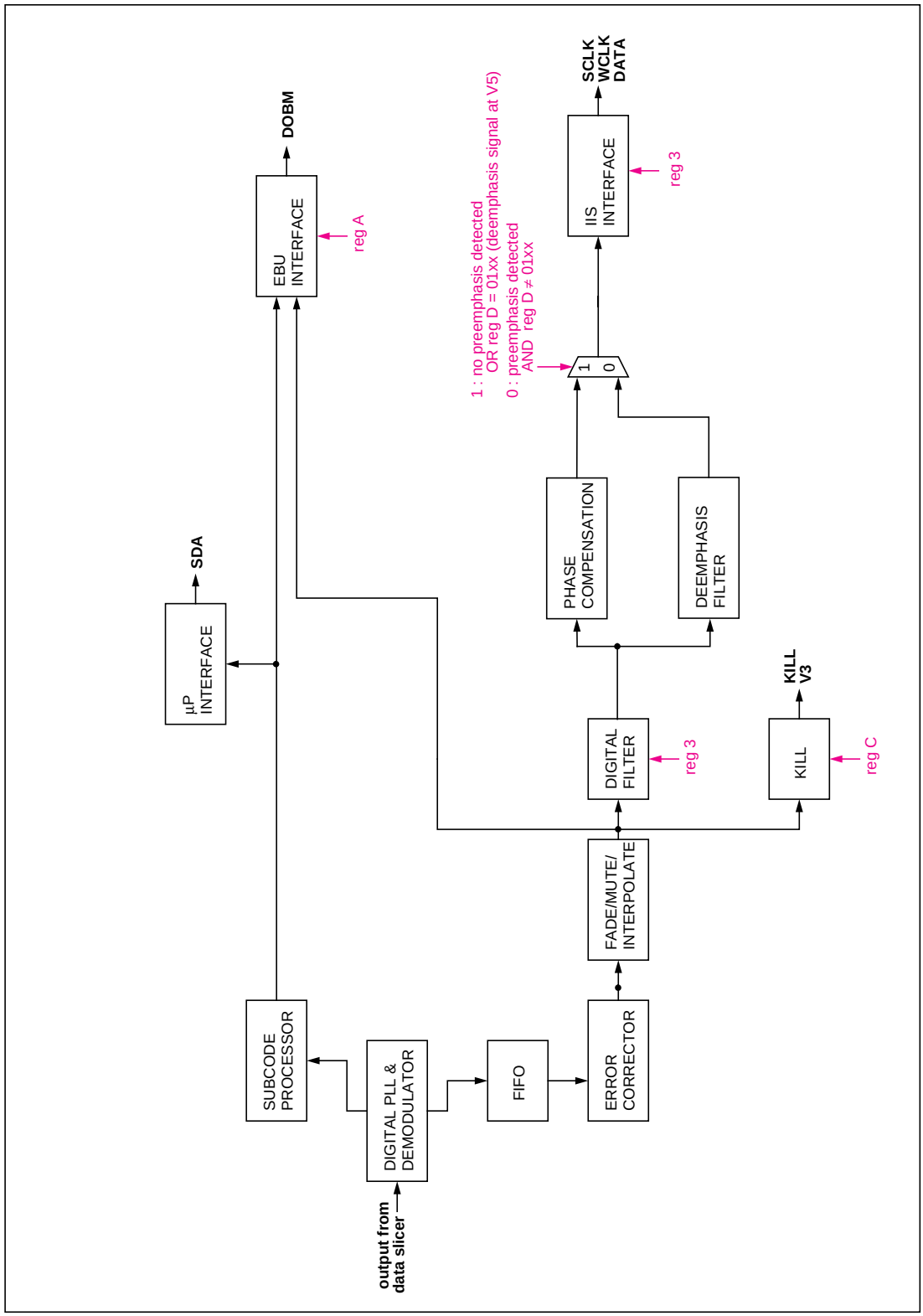


Figure 5 SAA7378 Decoder Function: Simplified Data Flow

7.5 Subcode Data Processing

7.5.1 Q-Channel Processing

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the *SUBQREADY-I* signal will go low. *SUBQREADY-I* can be read via the SDA or STATUS pins, selected via register 2. Good Q-channel data may be read from SDA.

7.5.2 Subcode Channels Q-W

Data of subcode channels, Q-W, is available in the EBU output (DOBM).

7.6 FIFO and Error Corrector

The SAA7378 has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after (de-interleaving) by C2, to help in the generation of C2 output flags.
The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM).

7.6.1 Flags Output (CFLG)

The flags output pin CFLG (open-drain) shows the status of the error corrector and interpolator and is updated every frame 7.35kHz. In the SAA7378 chip a 1-bit flag is present on the CFLG pin as shown in Figure 6.This signal shows the status of the error corrector and interpolator.

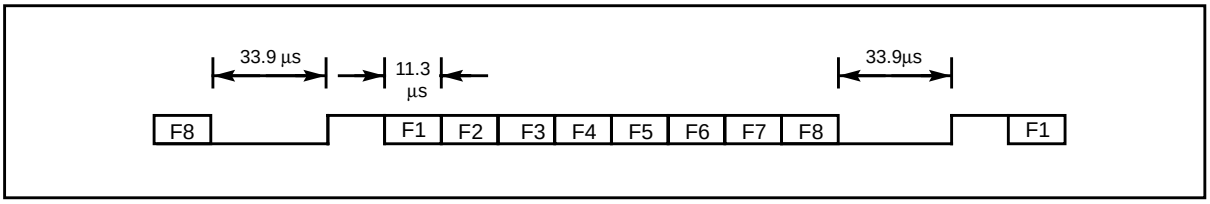


Figure 6 Flag Output Timing Diagram

F1	F2	F3	F4	F5	F6	F7	F8	MEANING
0	x	x	x	x	x	x	x	No Absolute Time sync
1	x	x	x	x	x	x	x	Absolute Time sync
x	0	0	x	x	x	x	x	C1 frame contained no errors
x	0	1	x	x	x	x	x	C1 frame contained 1 error
x	1	0	x	x	x	x	x	C1 frame contained 2 errors
x	1	1	x	x	x	x	x	C1 frame uncorrectable
x	x	x	0	0	x	x	0	C2 frame contained no errors
x	x	x	0	0	x	x	1	C2 frame contained 1 error
x	x	x	0	1	x	x	0	C2 frame contained 2 errors
x	x	x	0	1	x	x	1	C2 frame contained 3 error
x	x	x	1	0	x	x	0	C2 frame contained 4 errors
x	x	x	1	1	x	x	1	C2 frame uncorrectable
x	x	x	x	x	0	0	x	No interpolations
x	x	x	x	x	0	1	x	At least one 1-sample interpolation
x	x	x	x	x	1	0	x	At least one hold and no interpolations
x	x	x	x	x	1	1	x	At least one hold and one 1-sample interpolation

The first flag bit, F1, is the absolute time sync signal; the FIFO-passed subcode-sync and relates the position of the subcode-sync to the audio data (DAC output). The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by register A.

7.7 Audio Functions

7.7.1 Deemphasis and Phase Linearity

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a deemphasis filter section. When deemphasis is not required, a phase compensation filter section controls the phase of the digital oversampling filter to $\leq \pm 1°$ within the band 0 - 16 kHz. With deemphasis the filter is not phase linear.
If the deemphasis signal is set to be available at V5, selected via register D, then the deemphasis filter is bypassed.

7.7.2 Digital Oversampling Filter

The SAA7378 contains a 2 - 4 times oversampling IIR filter. The filter specification of the 4 x oversampling filter is given in the table below.

PASSBAND	ATTENUATION
0 - 19 kHz	≤0.001 dB
19 - 20 kHz	≤0.03 dB
STOPBAND	**ATTENUATION**
24.0 kHz	≥25 dB
24 - 27 kHz	≥38 dB
27 - 35 kHz	≥40 dB
35 - 64 kHz	≥50 dB
64 - 68 kHz	≥31 dB
68 kHz	≥35 dB
69 - 88 kHz	≥40 dB

These attenuations do not include the sample and hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled -0.5 dB down, to avoid overflow on full scale sine wave inputs (0 - 20 kHz).

7.7.3 Concealment

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (Figure 7). .

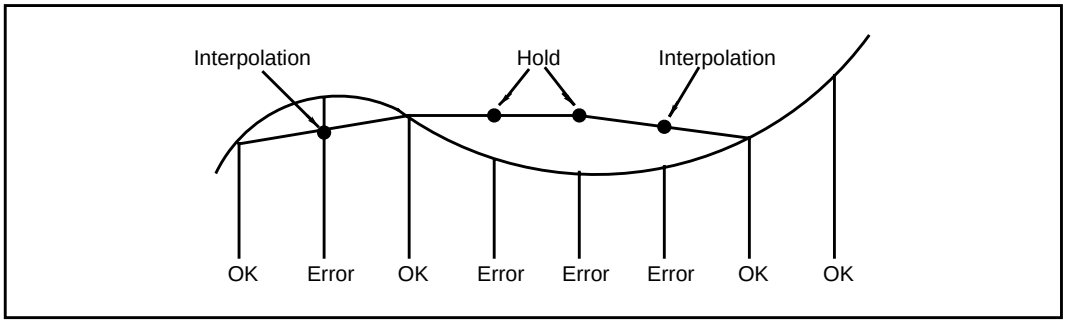


Figure 7 Concealment Mechanism

7.7.4 Mute, Full Scale, Attenuation and Fade

A digital level controller is present on the SAA7378 which performs the functions of soft mute, full scale, attenuation and fade; these are selected via register 0.

Mute: signal reduced to 0 in a maximum of 128 steps; 3ms.

Attenuate: signal scaled by -12dB.

Full scale: ramp signal back to 0dB level. From mute takes 3ms.

Fade: activates a 128 stage counter which allows the signal to be scaled up/down by 0.07dB steps.

- 128 = full scale
- 120 = -0.5dB (ie. full scale if oversampling filter used)
- 32 = -12dB
- 0 = mute

7.7.5 Peak Detector

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via SDA.

7.8 DAC Interface

The SAA7378 is compatible with a wide range of Digital-Analogue Converters. Six formats are supported and are shown below. Figure 8 and Figure 9 show the Philips IIS and the EIAJ data formats respectively. All formats are MSB first and fs is 44.1kHz. The polarity of the WCLK and the data can be inverted; selectable by register 7.

REGISTER 3	SAMPLE FREQUENCY	No of BITS	SCLK MHz	FORMAT	INTERPOLATION
0000	4fs	16	8.4672 * n	EIAJ - 16 bits	yes
0100	4fs	18	8.4672 * n	EIAJ - 18 bits	yes
1100	4fs	18	8.4672 * n	Philips I^2S - 18 bits	yes
0011	2fs	16	4.2336 * n	EIAJ - 16 bits	yes
0111	2fs	18	4.2336 * n	EIAJ - 18 bits	yes
1111	2fs	18	4.2336 * n	Philips I^2S - 18 bits	yes

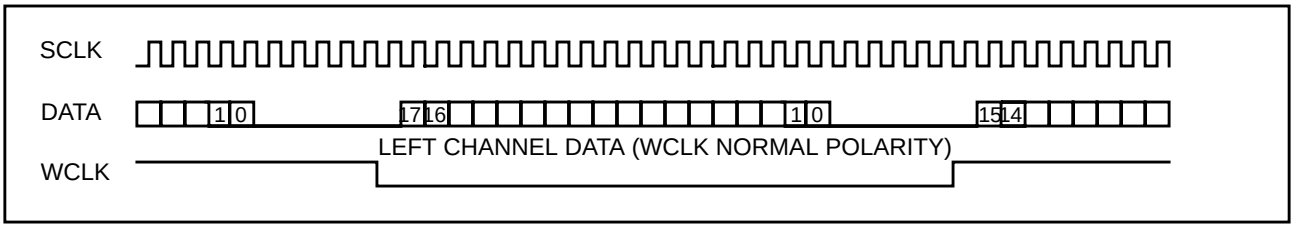


Figure 8 Philips I^2S Data Format (18-Bit Word Length Shown)

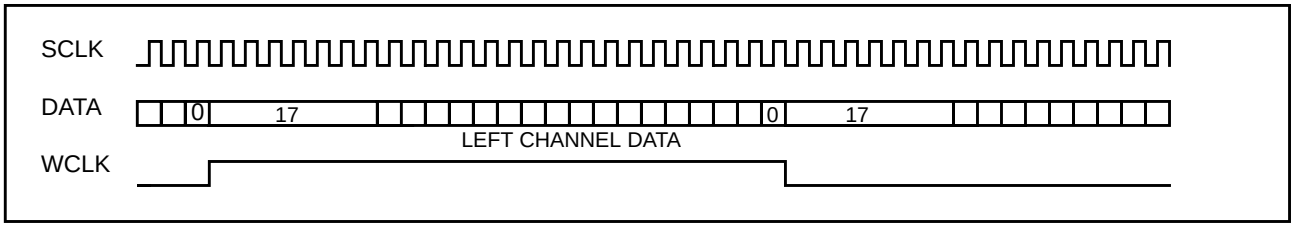


Figure 9 EIAJ Data Format (18-Bit Word Length Shown)

7.9 EBU Interface

The biphasemark digital output signal at pin DOBM is according to the format defined by the IEC958 specification. The DOBM pin can be held low; selected via register A:

7.9.1 Format

The digital audio output consists of 32-bit words ("subframes") transmitted in biphasemark code (two transitions for a logic'1' and one transition for a logic'0'). Words are transmitted in blocks of 384.

sync	bits 0 - 3	
auxiliary	bits 4 - 7	Not used. Normally zero
error flags	bit 4	CFLG error and interpolation flags when selected by register A
audio sample	bits 8 - 27	First 4 bits not used (always zero). 2's compliment. LSB = bit 12, MSB = bit 27
validity flag	bit 28	Valid = logic 0
user data	bit 29	Used for subcode data (Q to W)
channel status	bit 30	Control bits and category code
parity bit	bit 31	Even parity for bits 4 to 30

Sync: The Sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations:
- Sync B:- Start of a block (384 words), word contains left sample.
- Sync M:- Word contains left sample (no block start).
- Sync W:- Word contains right sample.

Audio sample: Left and right samples are transmitted alternately.

Validity flag: Audio samples are flagged (bit 28 = '1') if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment

User data: Subcode bits Q until W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.

Channel status: The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is shown below.

control	bits 0 - 3	copy of CRC checked Q-channel control bits 0 - 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has preemphasis
reserved mode	bits 4 - 7	always zero.
category code	bits 8 - 15	CD: bit 8 = logic1, all other bits = logic 0
clock accuracy	bits 28 - 29	set by register A: 10 = level I 00 = level II 01 = level III
remaining	bits 16 - 27 bits 30 - 191	always zero

7.10 KILL Circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel before the digital filter. The output is switched active-low when silence has been detected for at least 250ms, or if Mute is active. Two modes are available, selected by register C:

- 1 pin kill: KILL active low indicates silence detected on both left and right channels.
- 2 pin kill: KILL active low indicates silence detected on left channel.
  V3 active low indicates silence detected on right channel.

7.11 The VIA Interface

The SAA7378 has five pins that can be reconfigured for different applications:

PIN NAME	PIN no.	TYPE	CONTROL REGISTER ADDRESS	CONTROL REGISTER DATA	FUNCTION
V1	62	Input	1100	xxx1	External offtrack signal input
				xxx0	Internal offtrack signal used Input may be read via decoder status bit; selected via register 2.
V2	63	Input			Input may be read via decoder status bit; selected via register 2.
V3	42	Output	1100	xx0x	Kill output for Right channel
				x01x	Output = 0
				x11x	Output = 1
V4	41	Output	1101	0000	4-line motor drive (using V4 & V5)
				xx10	Output = 0
				xx11	Output = 1
V5	40	Output	1101	01xx	Deemphasis output (active high)
				10xx	Output = 0
				11xx	Output = 1

7.12 Spindle Motor Control

7.12.1 Motor Output Modes

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ± 8 frame FIFO and Disc speed information are used to calculate the motor control output signals. Several output modes, selected by register 6, are supported:

- Pulse Density, 2-line (true complement output), 1MHz sample frequency.
- PWM-output, 2-line, 22.05kHz modulation frequency.
- PWM-output, 4-line, 22.05kHz modulation frequency.
- CDV motor mode.

7.12.1.1 Pulse Density Output Mode

In the Pulse Density mode the motor output pin, MOTO1, is the pulse density modulated motor output signal. 50% duty cycle corresponds with the motor not actuated, higher duty cycles mean acceleration, lower mean braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a 1MHz internal clock signal. Possible application diagrams are shown in Figure 10.

7.12.1.2 PWM Output Mode, 2-Line

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output, and the motor braking signal is pulse-width modulated on the MOTO2 output. Figure 11 shows the timing and Figure 12 a typical application diagram.

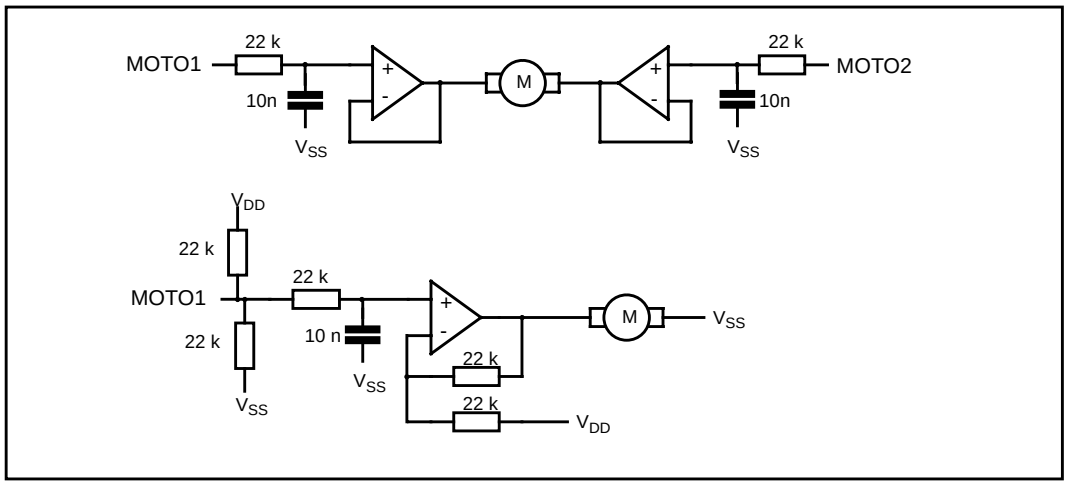


Figure 10 Motor Pulse Density Application Diagrams

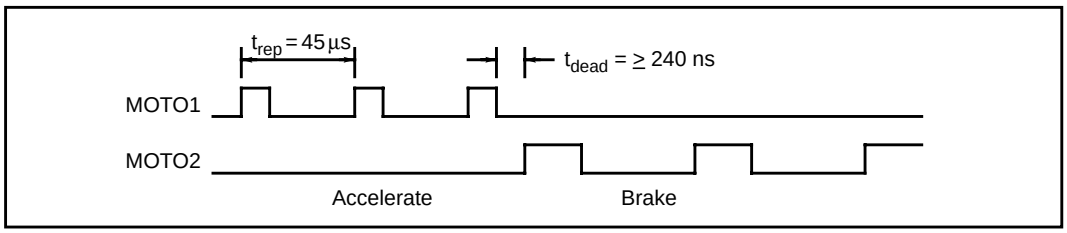


Figure 11 2-Line PWM Mode Timing

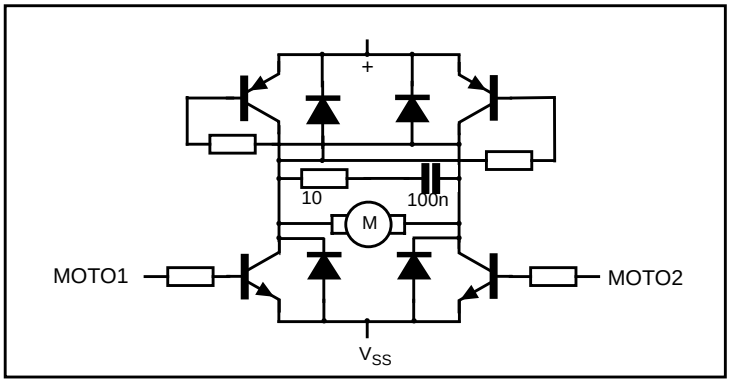


Figure 12 Motor 2-Line PWM Mode Application Diagram

7.12.1.3 PWM Output Mode, 4-Line

Using two extra outputs from the Versatile Pins Interface, it is possible to use the SAA7378 with a 4-input motor bridge.

Figure 13 shows the timing, and Figure 14 a typical application diagram.

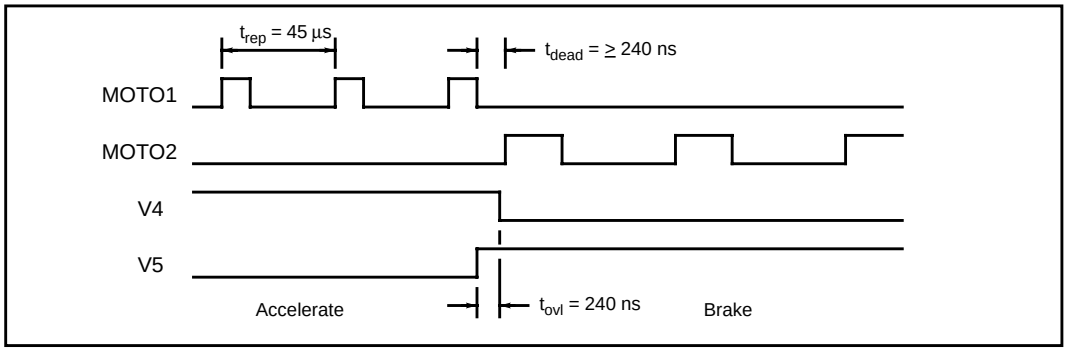


Figure 13 4-Line PWM Mode Timing

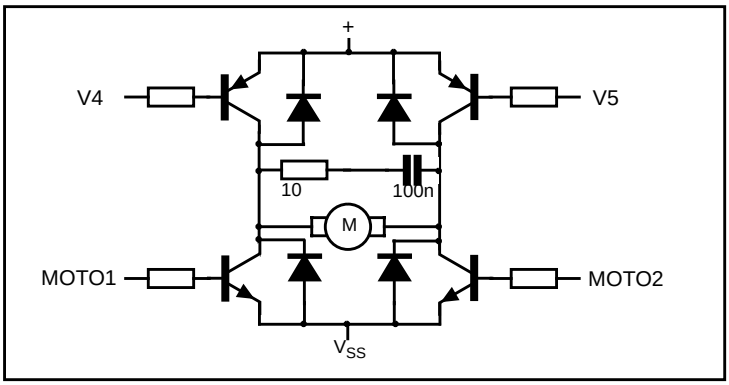


Figure 14 Motor 4-Line PWM Mode Application Diagram

7.12.1.4 CDV/CAV Output Mode

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin (carrier frequency 300Hz), and the PLL frequency signal will be put in pulse-density modulated form (carrier frequency 4.23MHz) on the MOTO2 pin. The integrated motor servo is disabled in this mode.

Notes: 1) The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half full) will result in a PWM output of 60%.

7.12.2 Spindle Motor Operating Modes

The motor servo has the following operation modes controlled by register 1:

Start mode 1 Disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No Disc speed information is available for the µP.

Start mode 2 The Disc is accelerated as in *Start mode 1*, however the PLL will monitor the Disc speed. When the Disc reaches 75% of its nominal speed, the controller will switch to *Jump mode*. The motor status signals selectable via register 2 are valid.

Jump mode Motor servo enabled but FIFO kept reset at 50%, integrator is held. The audio is muted but it is possible to read the subcode.

Jump mode 1 Similar to *Jump mode* but motor integrator is kept at zero. Used for long jumps, where there is a large change in disc speed.

Play mode FIFO released after resetting to 50%. Audio mute released.

Stop mode 1 Disc is braked by applying a negative voltage to the motor. No decisions are involved.

Stop mode 2 The Disc is braked as in *Stop mode 1*, but the PLL will monitor the Disc speed. As soon as the Disc reaches 12% (or 6%, depending on the programmed brake percentage, via register E) of its nominal speed, the MOTSTOP status signal will go high and switch the motor servo to *Off mode*.

Off mode Motor not steered.

In the SAA7378 decoder there is an anti-wind-up mode for the motor servo, selected via register 1. When the anti-wind-up mode is activated the motor servo integrator will hold if the motor output saturates.

7.12.2.1 Power Limit

In *Start mode 1, Start mode 2, Stop mode 1* and *Stop mode 2*, a fixed positive or negative voltage is applied to the motor. This voltage can be programmed as a percentage of the maximum possible voltage, via register 6, to limit current drain during start and stop. The following power limits are possible:

100% (no power limit), 75%, 50%, or 37% of maximum.

7.12.3 Loop Characteristics

The gain and crossover frequencies of the motor control loop can be programmed via registers 4 and 5. The following parameter values are possible:

Gains: 3.2, 4.0, 6.4, 8.0, 12.8, 16, 25.6, 32

Crossover frequency f_4: 0.5Hz, 0.7Hz, 1.4Hz, 2.8Hz

Crossover frequency f_3: 0.85Hz, 1.71Hz, 3.42Hz

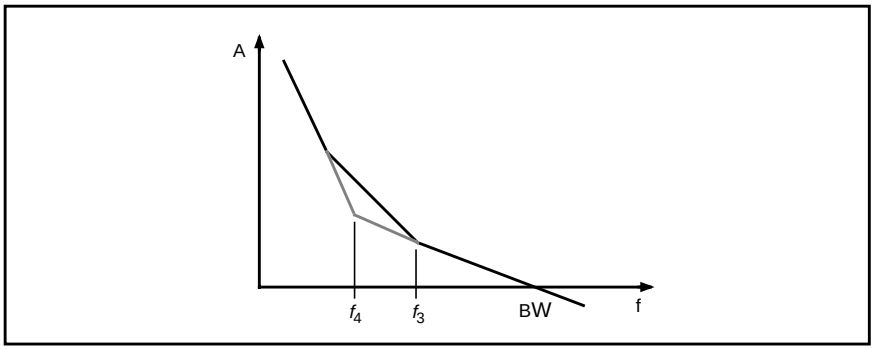


Figure 15 Motor Servo Bode Diagram

7.12.4 FIFO Overflow

If FIFO overflow occurs during *Play mode* (eg: as a result of motor rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator tries to conceal as much as possible to minimise the effect of data loss.

8. FUNCTIONAL DESCRIPTION OF THE SERVO PART

8.1 Diode Signal Processing

The photo detector in conventional two-stage three-beam compact disc systems normally contains six discrete diodes. Four of these diodes (three for single focault systems) carry the central aperture (CA) signal while the other two diodes (satellite diodes) carry the radial tracking information. The CA signal is processed into an HF signal (for the decoder function) and LF signal (information for the focus servo loop) before it is supplied to the SAA7378.

The analog signals from the central and satellite diodes are converted into a digital representation using analog to digital converters (ADCs). The ADCs are designed to convert unipolar currents into a digital code. The dynamic range of the input currents is adjustable within a given range which is dependent on the value of external resistor connected to IREFT. The maximum current for the central diodes and satellite diodes is given below:

$I_{in(max,\ central)} = (2.4 * 10^6 / R_{IREFT})\ \mu A$

$I_{in(max,\ satellite)} = (1.2 * 10^6 / R_{IREFT})\ \mu A$

The V_{RH} voltage is internally generated by control circuitry which takes care that the V_{RH} voltage is adjusted depending upon the spread of internal capacitors, using the reference current generated by the external resistor on IREFT. In the application V_{RL} is connected to V_{SSA1}. The maximum input currents for a range of resistors is given below:

R_{IREFT} (Ω)	diode input current range	
	D1,D2,D3,D4 (μA)	R1,R2 (μA)
220k	10.909	5.455
240k	10.000	5.000
270k	8.889	4.444
300k	8.000	4.000
330k	7.273	3.636
360k	6.667	3.333
390k	6.154	3.077
430k	5.581	2.791
470k	5.106	2.553
510k	4.706	2.353
560k	4.286	2.143
620k	3.871	1.935

This mode of V_{RH} automatic adjustment can be selected by the preset latch command.

Alternatively the dynamic range of the input currents can be made dependent on the ADC reference voltages; V_{RL} and V_{RH}, for this case the maximum current for the central diodes and satellite diodes is given below:

$I_{in(max,\ central)} = f_{sys} * (V_{RH} - V_{RL}) * 1.0 * 10^{-6}\ \mu A$

$I_{in(max,\ satellite)} = f_{sys} * (V_{RH} - V_{RL}) * 0.5 * 10^{-6}\ \mu A$ where f_{sys} = 4.2336MHz

V_{RH} is generated internally, and there are 32 levels which can be selected under software control, via the preset latch command. With this command the V_{RH} voltage can be set to 2.5V then modified, decremented one level or incremented, by resending the command the required number of times. In the application V_{RL} is connected to V_{SSA1}.

8.2 Signal Conditioning

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain the various control signals. The signals from the central aperture diodes are processed to obtain a normalised focus error signal:

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

where the detector set up is assumed as shown in Figure 16.

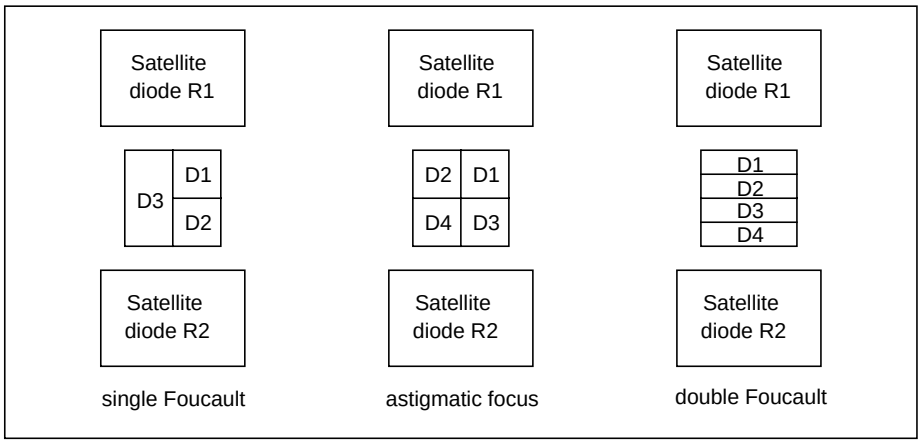


Figure 16 Detector Arrangement

In the case of single Foucault focusing method, the signal conditioning can be switched under software control such that the signal processing is as follows:

$$FE_n = 2 * \frac{D1 - D2}{D1 + D2}$$

The error signal, FE_n, is further processed by a proportional integral and differential (PID) filter section.

A focus OK (FOK) flag is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the track-loss (TL) generation, the focus start up procedure and the drop out detection.

The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal can be formulated as follows:

$$RE_s = (R1 - R2) * re\_gain + (R1 - R2) * re\_offset$$

where the index 's' indicates the automatic scaling operation which is performed on the radial error signal. This scaling is necessary to avoid non-optimal dynamic range usage in the digital representation and reduces the radial bandwidth spread. Furthermore, the radial error signal will be made free from offset during start up of the disc.

The four signals from the central aperture detectors together with the satellite detector signals generate a track position signal (TPI), which can be formulated as follows:

$$TPI = sign\ [\ (D1 + D2 + D3 + D4) - (R1 + R2) * sum\_gain]$$

Where the weighting factor *sum_gain* is generated internally, by the SAA7378, during initialisation.

8.3 Focus Servo System

The SAA7378 includes the following focus servo functions:

8.3.1 Focus Start-up

Five initially loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangle voltage can be influenced by 3 parameters; for height *(ramp_height*) and DC-offset (*ramp_offset*) of the triangle and its steepness (*ramp_incr*).

For protection against false focus point detections two parameters are available, which are an absolute level on the CA-signal (*CA_start*) and a level on the FE_n signal (*FE_start*). When this CA level is reached the FOK signal becomes true.

If this FOK signal is true and the level on the FE_n signal is reached, the focus PID is enabled to switch on when the next zero crossing is detected in the FE_n signal.

8.3.2 Focus Position Control Loop

The focus control loop contains a digital PID controller which has 5 parameters available to the user. These coefficients influence the integrating (*foc_int*), proportional (foc_lead_length, part of *foc_parm3*) and differentiating (foc_pole_lead, part of *foc_parm1*) action of the PID and a digital low pass filter (foc_pole_noise, part of *foc_parm2*) following the PID. The fifth coefficient *foc_gain* influences the loop gain.

8.3.3 Drop-out Detection

This detector can be influenced by one parameter (CA_drop). The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false it is assumed, initially, to be caused by a black dot.

8.3.4 Focus Loss Detection and Fast Restart

Whenever FOK is false for longer than about 3ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300ms depending on the microprocessor programmed coefficients.

8.3.5 Focus Loop Gain Switching

The gain of the focus control loop (*foc_gain*) can be multiplied by a factor of 2 or divided by a factor of 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (foc_pole_lead) action of the PID can be switched at the same time as the gain switching is performed.

8.4 Radial Servo System

The SAA7378 includes the following focus servo functions:

8.4.1 Level Initialisation

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain (*re_gain*), offset (*re_offset*) and satellite sum gain (*sum_gain*) for TPI level generation. The initialisation procedure runs in a radial open loop situation and is ≤300ms. This start-up time period may coincide with the last part of the motor start up time period.

Automatic gain adjustment: As a result of this initialisation the amplitude of the RE signal is adjusted within ±10% around the nominal RE amplitude

Offset adjustment: The additional offset in RE due to the limited accuracy of the start-up procedure is less than ±50nm.

TPI level generation: The accuracy of the initialisation procedure is such that the duty cycle range of TPI becomes 0.4 < dutycycle < 0.6 (def. dutycycle: TPI-'high' / TPI-period).

8.4.2 Sledge Control

The microprocessor can move the sledge in both directions via the steer sledge command.

8.4.3 Tracking Control

The actuator is controlled using a PID loop filter with user defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over 0.75 track. Upon request from the microprocessor S-curve extension over 2.25 tracks is used, automatically changing to access control when exceeding those 2.25 tracks.

Both modes of S-curve extension make use of a track-count mechanism. In this mode track counting results in an 'automatic return to zero track', to avoid major music rhythm disturbances in the audio output for improved shock resistance. The sledge is continuously controlled using the filtered value of the radial PID output. Alternatively the microprocessor can read the average voltage on the radial actuator, and provides the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control are user presettable.

8.4.4 Access

The access procedure is divided into two different modes, depending upon the requested jump size.

ACCESS TYPE	JUMP SIZE	ACCESS SPEED
Actuator jump	1 - brake_distance[1]	decreasing velocity
Sledge jump	brake_distance[1] - 32768	maximum power to sledge [1]

[1] : microprocessor presettable

The access procedure makes use of a track counting mechanism, a velocity signal based on a fixed number of tracks passed within a fixed time interval, a velocity setpoint calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.

If the number of tracks to go is greater than brake_distance then the sledge jump mode should be activated else the actuator jump should be performed. The requested jump size together with the required sledge breaking distance at maximum access speed defines the value brake_distance.

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the radial PID output. All filter parameters (for actuator and sledge) are user programmable.

In sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction, while the actuator becomes idle (the contents of the actuator integrator leaks to zero just after the sledge jump mode is initiated).

8.5 Off Track Counting

The track position (TPI) signal is a flag which is used to indicate whether the radial spot is positioned on the track, with a margin of ± 1/4 of the track-pitch. In combination with the radial polarity flag (RP) the relative spot position over the tracks can be determined. These signals are, however afflicted with some uncertainties caused by:

- disc defects such as scratches and fingerprints.
- the HF information on the disc, which is considered as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a track loss (TL) signal as well as an off-track counter value. These extra conditions influence the maximum speed and this implies that, internally, one of the three following counting states is selected:

1. Protected state: used in normal play situations.
   A good protection against false detection caused by disc defects is important in this state.
2. Slow counting state: used in low velocity track jump situations.
   In this state a fast response is important rather than the protection against disc defects (if the phase relationship between TL and RP of 1/2 π radians is affected too much, the direction cannot be determined accurately anymore).
3. Fast counting state: used in high velocity track jump situations.
   Highest obtainable velocity is the most important feature in this state.

8.6 Defect Detection

A defect detection circuit is incorporated into the SAA7378. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability. The defect detector can be switched off, applied only to focus control, or applied to both focus and radial controls under software control (part of *foc_parm1*).

The defect detector (Figure 17) has programmable setpoints selectable by the parameter, *defect_parm*.

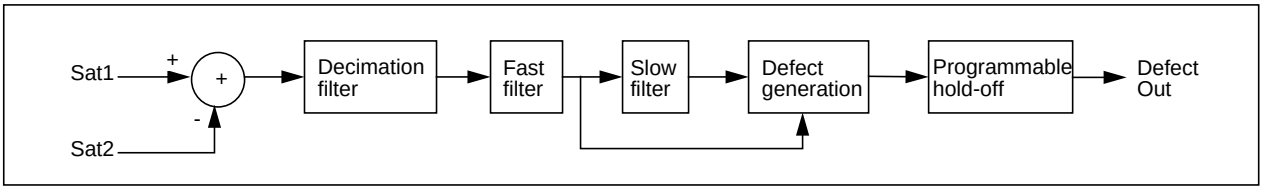


Figure 17 Defect Detector Block Diagram

8.7 Off Track Detection

During active radial tracking, off track detection has been realised by continuously monitoring the off track counter value. The off track flag becomes valid whenever the off track counter value is unequal to zero. Depending on the type of extended S-curve the off track counter is reset after 0.75 extend or at the original track in the 2.25 track extend mode.

8.8 Driver Interface

The control signals (pins RA, FO and SL) for the mechanism actuators are pulse density modulated. The modulating frequency can be set to either 1.0584MHz (DSD mode) or 2.1168MHz; controlled via the *xtra_preset* parameter. An analog representation of the output signals can be achieved by connecting a first order low pass filter to the outputs.

During reset (ie. RESET pin is held low) the RA, FO and SL pins are high impedance.

8.9 Laser Interface

The LDON pin (open drain output) is used to switch the laser off and on; when the laser is on the output is high impedance. The action of the LDON pin is controlled by the *xtra_preset* parameter; the pin is automatically driven if the focus control loop is active.

8.10 Radial Shock Detector

The shock detector (block diagram shown in Figure 18) can be switched on during normal track following; and detects within an adjustable frequency whether disturbances in the radial spot position relative to the track exceed an adjustable level (controlled by *shock_level*). Every time the radial tracking error (RE) exceeds this level the radial control bandwidth is switched to twice its original bandwidth and the loop gain is increased by a factor of 4.

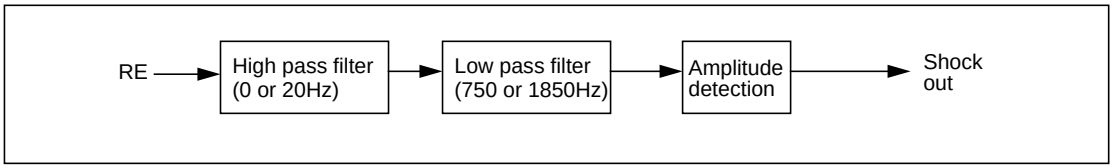


Figure 18 Block Diagram of Shock Detector

The shock detection level is adjustable in 16 steps from 0 to 100% of the traverse radial amplitude which is sent to an amplitude detection unit via an adjustable bandpass filter (controlled by *sledge_parm1*); lower corner frequency can be set at either 0 or 20Hz, and upper corner frequency at 750 or 1850Hz. The shock detector is switched off automatically during jump mode.

9. MICROPROCESSOR INTERFACE

Communication on the microprocessor interface is via a 4-wire bus: the protocol being compatible with SAA7345 (CD6) and TDA1301 (DSIC2):

SCL - serial bit clock.

SDA - serial data.

RAB - R/W control and data strobe (active high) for writing to registers 0 - F, reading status bit selected via register 2 and reading Q channel subcode.

SILD - R/W control and data strobe (active low) for servo commands.

9.1 Writing Data to Registers 0 - E

The sixteen 4-bit programmable configuration registers, 0 to E (Table 1), can be written to via the microprocessor interface using the protocol shown in Figure 19.

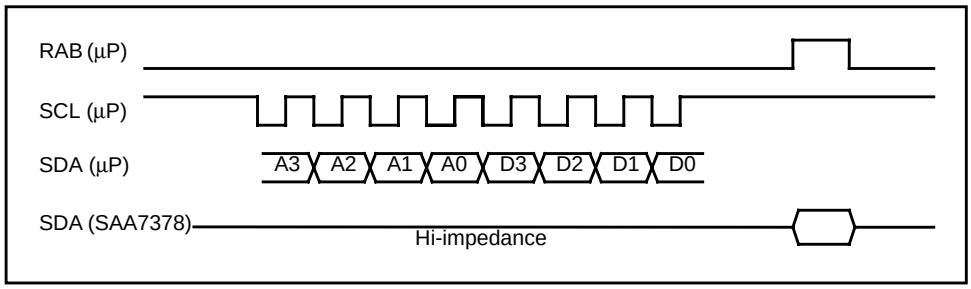


Figure 19 Microprocessor Write Protocol for Registers 0 to E

Note that: - SILD must be held high.
- A(3:0) identifies the register number, D(3:0) is the data.
- the data is latched into the register on the low-high transition of RAB.

9.1.1 Writing Repeated Data to Registers 0 - E

The same data can be repeated several times (eg: for a fade function) by applying extra RAB pulses as shown in Figure 20. Note that SCL must stay high between RAB pulses.

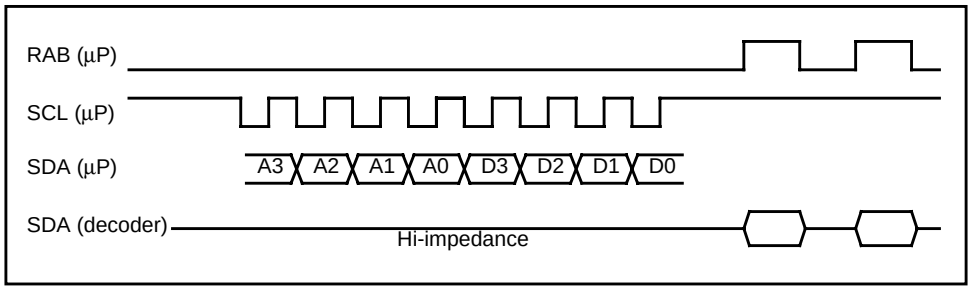


Figure 20 Microprocessor Write Protocol for Registers 0 to E - Repeat Mode

9.2 Reading Decoder Status Information on SDA

There are several internal status signals, selected via register 2, which can be made available on the SDA line. These are:

- *SUBQREADY-I* Low if new subcode word is ready in Q-channel register.
- *MOTSTART1* High if motor is turning at 75% or more of nominal speed.
- *MOTSTART2* High if motor is turning at 50% or more of nominal speed.
- *MOTSTOP* High if motor is turning at 12% or less of nominal speed. Can be set to indicate 6% or less (instead of 12% or less) via register E.
- *PLL Lock* High if *Sync coincidence* signals are found.
- *V1* Follows input on V1 pin.

- *V2* Follows input on V2 pin.
- *MOTOR-OV* High if the motor servo output stage saturates.
- *FIFO-OV* High if FIFO overflows.
- *SHOCK* $\overline{\text{MOTSTART2}}$ + $\overline{\text{PLL Lock}}$ + MOTOR-OV + FIFO-OV + OTD (high if shock detected)
- *LA-SHOCK* Latched SHOCK signal

The status read protocol is shown in Figure 21.

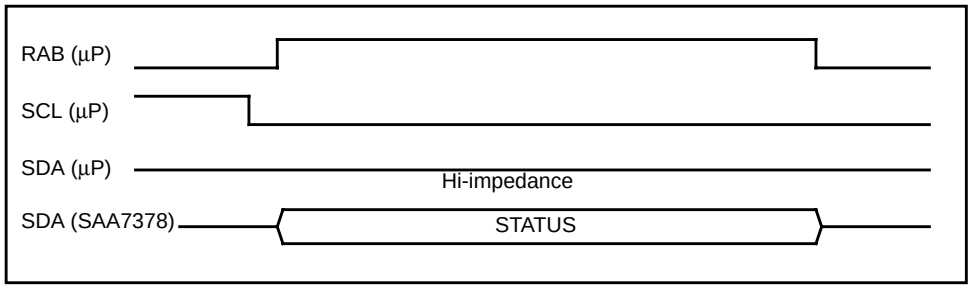


Figure 21 Microprocessor Read Protocol for Decoder Status on SDA

Note that: - SILD must be held high.

9.3 Reading Q-Channel Subcode

To read Q-channel subcode direct in 4-wire bus mode, the *SUBQREADY-I* signal should be selected as status signal. The subcode read protocol is shown in Figure 22.

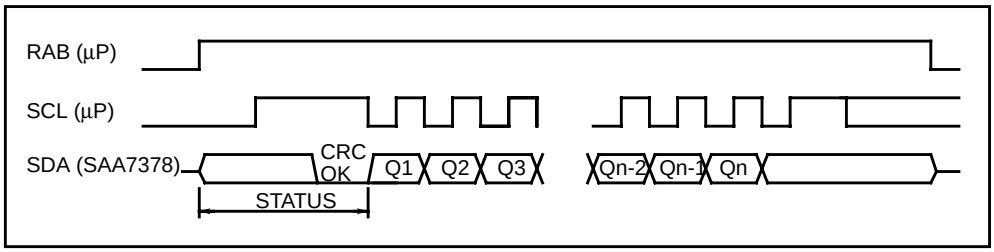


Figure 22 Microprocessor Protocol for Reading Q-Channel Subcode

Note that: - SILD must be held high.
- after subcode read starts, the microprocessor may take as long as it wants to terminate the read operation.
- when enough subcode has been read (1 - 96 bits), terminate reading by pulling RAB low.

9.3.1 Behaviour of the *SUBQREADY-I* Signal

When the CRC of the Q-channel word is good, and no subcode is being read, the *SUBQREADY-I* status signal will react as shown in Figure 23:

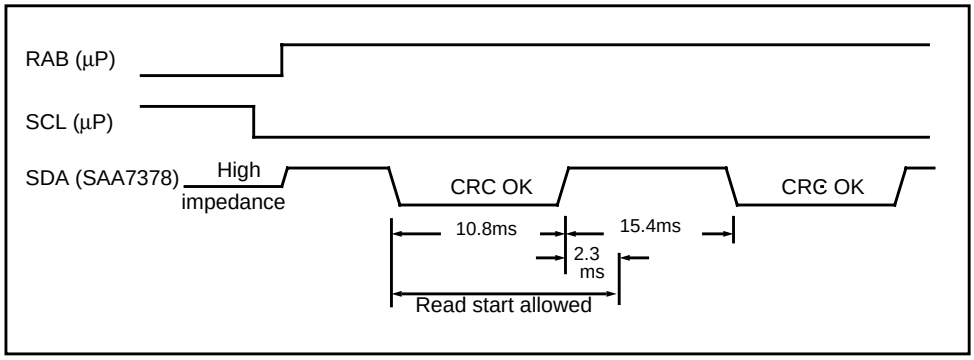


Figure 23 *SUBQREADY-I* Status Timing when no Subcode is Read

When the CRC is good and subcode is being read, the timing in Figure 24 applies:

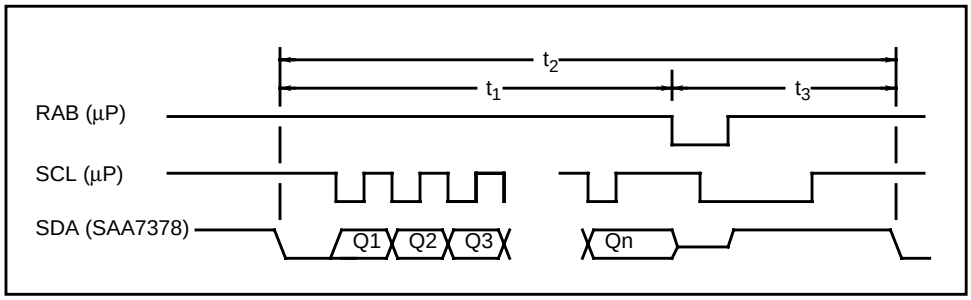


Figure 24 *SUBQREADY-I* Status Timing when Subcode is Read

If t_1 (*SUBQREADY-I* status low to end of subcode read) is below 2.6ms, then t_2 = 13.1ms [ie: the microprocessor can read all subcode frames if it completes the read operation within 2.6ms after the subcode is ready]. If this criterion is not met, it is only possible to guarantee that t_3 will be below 26.2ms (approximately).

If subcode frames with failed CRCs are present, the t_2 and t_3 times will be increased by 13.1ms for each defective subcode frame.

9.4 Write Servo Commands

A write data command is used to transfer data (a number of bytes) from the microprocessor, using the protocol shown in Figure 25. The first of these bytes is the command byte and the following are data bytes; the number (between 1 and 7) depends on the command byte.

Note that: - RAB must be held low.
- The command or data is interpreted by the SAA7378 after the high-low transition of SILD.
- There must be a minimum time of 65µs between SILD pulses.

9.4.1 Writing Repeated Data In Servo Commands

The same data byte can be can be repeated by applying extra SILD pulses as shown in Figure 26. SCL must stay high

between the SILD pulses.

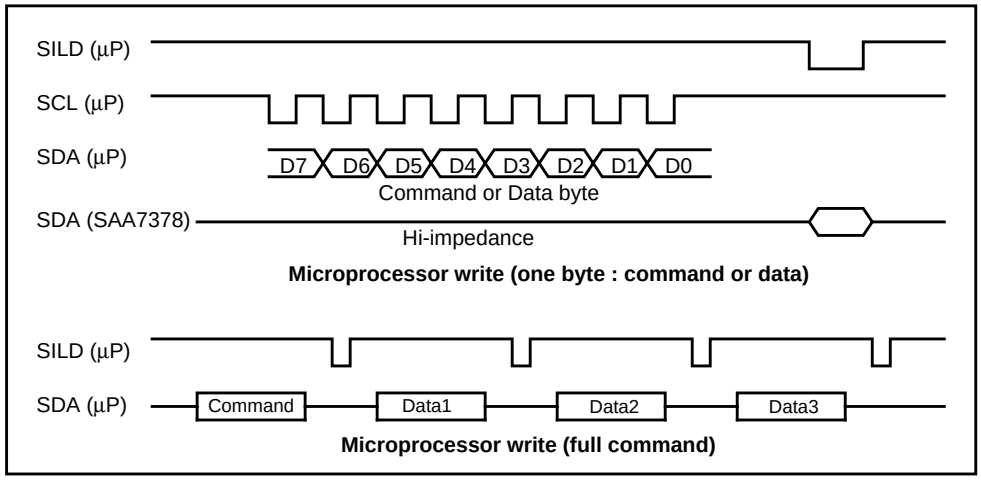


Figure 25 Microprocessor Protocol for Write Servo Commands

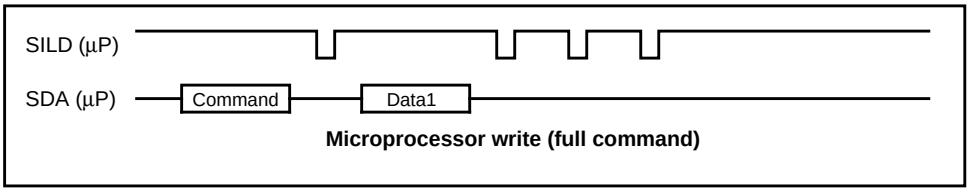


Figure 26 Microprocessor Protocol for Repeated Data in Write Servo Commands

9.5 Read Servo Commands

A read data command is used to transfer data (status information) to the microprocessor, using the protocol shown in Figure 27. The first byte written determines the type of command. After this byte a variable number of bytes can be read.

Note that: - RAB must be held low.
- After the end of a read command there must be a delay of 65µs before a write command is started.
- There must be a minimum time of 65µs between SILD pulses.

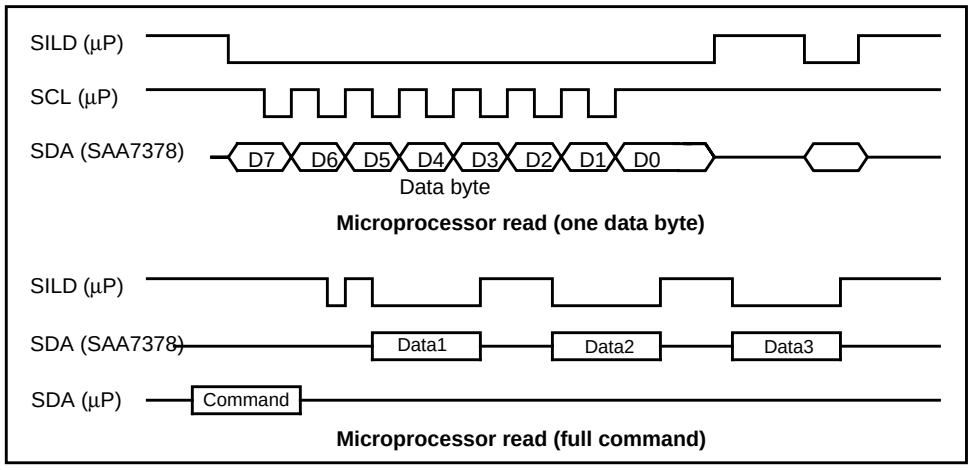


Figure 27 Microprocessor Protocol for Read Servo Commands

9.6 Summary of Functions Controlled by Registers 0 to E

The INITIAL column shows the power-on reset state

Table 1 Registers 0 to E

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
0 (Fade and Attenuation)	0 0 0 0	0 0 0 0	Mute	Reset
		0 0 1 0	Attenuate	
		0 0 0 1	Full Scale	
		0 1 0 0	Step Down	
		0 1 0 1	Step Up	
1 (Motor mode)	0 0 0 1	x 0 0 0	Motor off mode	Reset
		x 0 0 1	Motor stop mode 1	
		x 0 1 0	Motor stop mode 2	
		x 0 1 1	Motor start mode 1	
		x 1 0 0	Motor start mode 2	
		x 1 0 1	Motor jump mode	
		x 1 1 1	Motor play mode	
		x 1 1 0	Motor jump mode 1	
		1 x x x	anti-windup active	
		0 x x x	anti-windup off	Reset
2 (Status control)	0 0 1 0	0 0 0 0	status = SUBQREADY-I	Reset
		0 0 0 1	status = MOTSTART1	
		0 0 1 0	status = MOTSTART2	
		0 0 1 1	status = MOTSTOP	
		0 1 0 0	status = PLL Lock	
		0 1 0 1	status = V1	
		0 1 1 0	status = V2	
		0 1 1 1	status = MOTOR-OV	
		1 0 0 0	Status = FIFO overflow	
		1 0 0 1	Status = Shock Detect	
		1 0 1 0	Status = Latched Shock Detect	
		1 0 1 1	Status = Latched Shock Detect Reset	
3 (DAC output)	0 0 1 1	1 1 0 0	I^2S - 18 bit - 4fs mode	Reset
		1 1 1 1	I^2S - 18 bit - 2fs mode	
		0 0 0 0	EIAJ - 16 bit - 4fs	
		0 0 1 1	EAIJ - 16 bit - 2fs	
		0 1 0 0	EIAJ - 18 bit - 4fs	
		0 1 1 1	EIAJ - 18 bit - 2fs	

Table 1 Registers 0 to E

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
4 (Motor gain)	0 1 0 0	x 0 0 0	Motor gain G = 3.2	Reset
		x 0 0 1	Motor gain G = 4.0	
		x 0 1 0	Motor gain G = 6.4	
		x 0 1 1	Motor gain G = 8.0	
		x 1 0 0	Motor gain G = 12.8	
		x 1 0 1	Motor gain G = 16.0	
		x 1 1 0	Motor gain G = 25.6	
		x 1 1 1	Motor gain G = 32.0	
		0 x x x	Disable comparator clock divider	Reset
		1 x x x	Enable comparator clock divider; only if SELLPLL set high	
5 (Motor bandwidth)	0 1 0 1	x x 0 0	Motor *f*4 = 0.5Hz	Reset
		x x 0 1	Motor *f*4 = 0.7Hz	
		x x 1 0	Motor *f*4 = 1.4Hz	
		x x 1 1	Motor *f*4 = 2.8Hz	
		0 0 x x	Motor *f*3 = 0.85Hz	Reset
		0 1 x x	Motor *f*3 = 1.71Hz	
		1 0 x x	Motor *f*3 = 3.42Hz	
6 (Motor output configuration)	0 1 1 0	x x 0 0	Motor power max. 37%	Reset
		x x 0 1	Motor power max. 50%	
		x x 1 0	Motor power max. 75%	
		x x 1 1	Motor power max. 100%	
		0 0 x x	MOTO1, MOTO2 pins tri-state	Reset
		0 1 x x	Motor PWM mode	
		1 0 x x	Motor PDM mode	
		1 1 x x	Motor CDV mode	
7 (DAC output)	0 1 1 1	x 0 0 0	DAC data normal value	Reset
		x 1 0 0	DAC data inverted value	
		0 x x x	L channel first at DAC (WCLK normal)	Reset
		1 x x x	R channel first at DAC (WCLK inverted)	
			Loop BW Hz Int. BW Hz Low-pass BW Hz	
8 (PLL loop filter bandwidth)	1 0 0 0	0 0 0 0	1640 525 8400	
		0 0 0 1	3279 263 16800	
		0 0 1 0	6560 131 33600	
		0 1 0 0	1640 1050 8400	
		0 1 0 1	3279 525 16800	
		0 1 1 0	6560 263 33600	
		1 0 0 0	1640 2101 8400	
		1 0 0 1	3279 1050 16800	Reset
		1 0 1 0	6560 525 33600	
		1 1 0 0	1640 4200 8400	
		1 1 0 1	3279 2101 16800	
		1 1 1 0	6560 1050 33600	

Table 1 Registers 0 to E

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
9 (PLL equalisation)	1 0 0 1	0 0 1 1	PLL loop filter equalisation	Reset
		0 0 0 1	PLL 30ns over-equalisation	
		0 0 1 0	PLL 15ns over-equalisation	
		0 1 0 0	PLL 15ns under-equalisation	
		0 1 0 1	PLL 30ns under-equalisation	
A (EBU output)	1 0 1 0	x 0 1 0	Level II clock accuracy (<1000ppm)	Reset
		x 0 1 1	Level I clock accuracy (<50ppm)	
		x 1 1 0	Level III clock accuracy (>1000ppm)	
		x 1 1 1	EBU off - output low	
		0 x x x	Flags in EBU off	Reset
		1 x x x	Flags in EBU on	
B	1 0 1 1	0 0 x x	33.8688MHz crystal present, or 8.4672MHz crystal with SELPLL set high	Reset
		0 1 x x	16.9344MHz crystal present	
		x x 0 0	Standby 1 : 'CD-STOP' mode	Reset
		x x 1 0	Standby 2 : 'CD-PAUSE' mode	
		x x 1 1	Operating mode	
C (Versatile pins interface)	1 1 0 0	x x x 1	External offtrack signal input at V1	
		x x x 0	Internal offtrack signal used (V1 may be read via status)	Reset
		x x 0 x	Kill-L at KILL output, Kill-R at V3 output	
		0 0 1 x	V3 = 0; single Kill output	Reset
		0 1 1 x	V3 = 1; single Kill output	
D (Versatile pins interface)	1 1 0 1	0 0 0 0	4-line motor (using V4, V5)	
		x x 1 0	V4 = 0	
		x x 1 1	V4 = 1	Reset
		0 1 x x	De-emphasis signal at V5, no internal de-emphasis filter	
		1 0 x x	V5 = 0	
		1 1 x x	V5 = 1	Reset
E	1 1 1 0	0 1 0 0	Motor brakes to 12%	Reset
		0 1 0 1	Motor brakes to 6%	

9.7 Summary of Servo Commands

A list of the servo commands are given below; note that these are not fully backwards compatible with DSIC2:

Table 2 CD7 Servo Commands.

WRITE COMMANDS			
	code	bytes	parameters
Write_focus_coefs1	17h	7	<foc_parm3> <foc_int> <ramp_incr> <ramp_height> <ramp_offset> <FE_start> <foc_gain>
Write_focus_coefs2	27h	7	<defect_parm> <rad_parm_jump> <vel_parm2> <vel_parm1> <foc_parm1> <foc_parm2> <CA_drop>
Write_focus_command	33h	3	<foc_mask> <foc_stat> <shock_level>
Focus_gain_up	42h	2	<foc_gain> <foc_parm1>
Focus_gain_down	62h	2	<foc_gain> <foc_parm1>
Write_radial coefs	57h	7	<rad_length_lead> <rad_int> <rad_parm_play> <rad_pole_noise> <rad_gain> <sledge_parm2> <sledge_parm_1>
Preset_Latch	81h	1	<chip_init>
Radial_off	C1h	1	"1Ch"
Radial_init	C1h	1	"3Ch"
Short_jump	C3h	3	<tracks_hi> <tracks_lo> <rad_stat>
Long_jump	C5h	5	<brake_dist> <sledge_U_max> <tracks_hi> <tracks_lo> <rad_stat>
Steer_sledge	B1h	1	<sledge_level>
Preset_init	93h	3	<re_offset> <re_gain> <sum_gain>
Write_parameter	A2h	2	<param_ram_addr> <param_data>
READ COMMANDS			
	code	bytes	parameters
Read_status	70h	up to 5	<foc_stat> <rad_stat> <rad_int_lpf> <tracks_hi> <tracks_lo>
Read_aux_status	F0h	up to 3	<re_offset> <re_gain> <sum_gain>

9.7.1 Summary of Servo Command Parameters

A list of the servo command parameters are given below:

parameter	RAM addr.	affects	POR value	determines
foc_parm_1	-	focus PID		end of focus lead defect detector enabling
foc_parm_2	-	focus PID		focus low pass focus error normalising
foc_parm_3	-	focus PID		focus lead length minimum light level
foc_int	14h	focus PID		focus integrator crossover freq
foc_gain	15h	focus PID	70h	focus PID loop gain
CA_drop	12h	focus PID		sensitivity of drop-out detector
ramp_offset	16h	focus ramp		assymetry of focus ramp
ramp_height	18h	focus ramp		p-p value of ramp voltage
ramp_incr	-	focus ramp		slope of ramp voltage
FE_start	19h	focus ramp		minimum value of focus error
rad_parm_play	28h	radial PID		end of radial lead
rad_pole_noise	29h	radial PID		radial low-pass
rad_length_lead	1Ch	radial PID		length of radial lead
rad_int	1Eh	radial PID		radial integrator crossover freq
rad_gain	2Ah	radial PID	70h	radial loop gain
rad_parm_jump	27h	radial jump		filter during jump
vel_parm1	1Fh	radial jump		PI controller crossover freqs
vel_parm2	32h	radial jump		jump pre-defined profile
speed_threshold	48h	radial jump		maximum speed in fastrad mode
hold_mult	49h	radial jump	00h	sledge bandwidth during jump
brake_dist_max	21h	radial jump		max sledge distance allowed in fast actuator steered mode
sledge_long_brake	58h	radial jump	7Fh	brake distance of sledge
sledge_Umax	-	sledge		voltage on sledge during long jump
sledge_level	-	sledge		voltage on sledge when steered
sledge_parm_1	36h	sledge		sledge integrator crossover freq
sledge_parm_2	17h	sledge		sledge low pass freqs sledge gain sledge operation mode
defect_parm	-	defect detector		defect detector setting
shock_level	-	shock detector		shock detector operation
chip_init	-	setup		V_{RH} level setting
xtra_preset	4Ah	setup	38h	laser on/off RA, FO, SL PDM modulating freq.
config_parm1	42h	setup		initialisation
config_parm2	53h	setup		initialisation
config_parm3	59h	setup		initialisation
config_parm4	68h	setup		initialisation

10. OPERATING CHARACTERISTICS

10.1 General Characteristics

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0; T_{amb} = 5 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	-	49		mA
Decoder Analogue Front-End (V_{DD} = 5.0 V; V_{SS} = 0; T_{amb} = 25 °C)						
	Comparator Inputs, HFIN, HFREF:					
f_{comp}	clock frequency	see Note 1	8	-	70	MHz
V_{th}	switching thresholds		1.2	-	V_{DD} - 0.8	V
V_{tpt}	HFIN input level			1.0	-	V
	Reference Generator, IREF:					
V_{IREF}	reference voltage at IREF pin		-	V_{DD}/2	-	V
Servo Analogue Part (V_{DD} = 5.0 V; V_{SS} = 0; T_{amb} = 25 °C)						
	Pins D1, D2, D3, D4, R1, R2, VRH, VRL, IREFT:					
I_{IREFT}	input current for IREFT		1.935	-	5.45	µA
R_{IREFT}	external resistor on IREFT		220	-	620	kΩ
V_{IREFT}	voltage on current input IREFT		-	1.2	-	V
I_D	maximum input current for central diode input signal	see Note 2	3.871	-	10.9	µA
I_R	maximum input current for satellite diode input signal	see Note 2	1.935	-	5.45	µA
V_{RL}	LOW level reference voltage		0	0	0	V
V_{RH}	HIGH level reference voltage	see Note 3				
		output state 0	-	0.5	-	V
		output state v	-30%	$.5*10^{v/44.4}$	+30%	V
		output state 31	-	2.5	-	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB; see Note 5	-	-50	-45	dB
S/N	signal to noise ratio		-	55	-	dB
PSRR	power supply rejection at $V_{DDA}2$	see Note 4	-	45	-	dB
G_{tol}	gain tolerance	see Note 6	-12	0	+12	%
ΔG	variation of gain between channels		-	-	2	%
a	channel separation		-	60	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
	Input: RESET, V1, V2, SELPLL	**CMOS input with pullup and hysteresis**				
V_{THR}	switching threshold rising		-	-	0.8 x V_{DD}	V
V_{THF}	switching threshold falling		0.2 x V_{DD}	-	-	V
V_{hys}	hysteresis voltage		-	0.33 x V_{DD}	-	V
R_{PU}	input pull-up resistance	V_{IN} = 0	-	50	-	kΩ
C_{IN}	input capacitance		-	-	10	pF
t_{RW}	reset pulse width (active low)	RESET only	1	-	-	µs
	Input: SCL, RAB, SILD	**CMOS input**				
V_{IL}	input voltage LOW		-0.3	-	0.3 x V_{DD}	V
V_{IH}	input voltage HIGH		0.7 x V_{DD}	-	V_{DD} + 0.3	V
I_{IN}	input leakage current	V_{IN} = 0 - V_{DD}	-10	-	+10	µA
C_{IN}	input capacitance		-	-	10	pF
Digital Output						
	Outputs: CL4					
V_{OL}	output voltage LOW	I_{OL} = + 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = - 1 mA	V_{DD} - 0.4	-	V_{DD}	V
C_L	load capacitance		-	-	25	pF
t_R	output rise time (C_L = 20 pF)	0.8 to (V_{DD} - 0.8)	-	-	20	ns
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) to 0.8	-	-	20	ns
	Outputs: CL16					
V_{OL}	output voltage LOW	I_{OL} = +1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = -1 mA	V_{DD} - 0.4	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
t_R	output rise time (C_L = 20 pF)	0.8 - (V_{DD} - 0.8)	-	-	15	ns
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) - 0.8	-	-	15	ns
	Outputs: V4, V5					
V_{OL}	output voltage LOW (V_{DD} = 4.5 to 5.5 V)	I_{OL} = + 10 mA	0	-	1.0	V
	output voltage LOW (V_{DD} = 3.4 to 5.5 V)	I_{OL} = + 5 mA	0	-	1.0	V
V_{OH}	output voltage HIGH (V_{DD} = 4.5 to 5.5 V)	I_{OH} = -10 mA	V_{DD} - 1	-	V_{DD}	V
	output voltage HIGH (V_{DD} = 3.4 to 5.5 V)	I_{OH} = -5 mA	V_{DD} - 1	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
t_R	output rise time (C_L = 20 pF)	0.8 - (V_{DD} - 0.8)	-	-	10	ns
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) -0.8	-	-	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Open Drain Outputs						
	Outputs: CFLG, STATUS, KILL, V3, LDON	**Open drain output with protection diode to VDD**				
V_{OL}	output voltage LOW	I_{OL} = +1 mA	0	-	0.4	V
I_{OL}	output current		-	-	2	mA
C_L	load capacitance		-	-	25	pF
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) - 0.8	-	-	30	ns
Tri-State Outputs						
	Outputs: SCLK, WCLK, DATA, CL11					
V_{OL}	output voltage LOW	I_{OL} = +1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = -1 mA	V_{DD} - 0.4	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
t_R	output rise time (C_L = 20 pF)	0.8 - (V_{DD} - 0.8)	-	-	15	ns
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) - 0.8	-	-	15	ns
I_{IN}	tri-state leakage current	V_{IN} = 0 - V_{DD}	-10	-	+10	µA
	Output: CL11					
t_{HIGH}	output high time (relative to clock period)	V_O = 1.5 V	45	50	55	%
	Outputs: RA, FO, SL					
V_{OL}	output voltage LOW	I_{OL} = +1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = -1 mA	V_{DD} - 0.4	-	V_{DD}	V
C_L	load capacitance		-	-	25	pF
t_R	output rise time (C_L = 20 pF)	0.8 - (V_{DD} - 0.8)	-	-	20	ns
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) - 0.8	-	-	20	ns
I_{IN}	tri-state leakage current	V_{IN} = 0 - V_{DD}	-10	-	+10	µA
	Outputs: MOTO1, MOTO2, DOBM					
V_{OL}	output voltage LOW (V_{DD} = 4.5 to 5.5 V)	I_{OL} = +10 mA	0	-	1.0	V
	output voltage LOW (V_{DD} = 3.4 to 5.5 V)	I_{OL} = +5 mA	0	-	1.0	V
V_{OH}	output voltage HIGH (V_{DD} = 4.5 to 5.5 V)	I_{OH} = -10 mA	V_{DD} - 1	-	V_{DD}	V
	output voltage HIGH (V_{DD} = 3.4 to 5.5 V)	I_{OH} = -5 mA	V_{DD} - 1	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
t_R	output rise time (C_L = 20 pF)	0.8 - (V_{DD} - 0.8)	-	-	10	ns
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) -0.8	-	-	10	ns
I_{IN}	tri-state leakage current	V_{IN} = 0 - V_{DD}	- 10	-	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output						
	Input/Output: SDA	**CMOS input/open drain output (with protection diode to VDD)**				
V_{IL}	input voltage LOW		-0.3	-	0.3 x V_{DD}	V
V_{IH}	input voltage HIGH		0.7 x V_{DD}	-	V_{DD} + 0.3	V
I_{IN}	tri-state leakage current	V_{IN} = 0 - V_{DD}	-10	-	+10	µA
C_{IN}	input capacitance		-	-	10	pF
V_{OL}	output voltage LOW	I_{OL} = +2 mA	0	-	0.4	V
I_{OL}	output current		-	-	4	mA
C_L	load capacitance		-	-	50	pF
t_F	output fall time (C_L = 20 pF)	(V_{DD} - 0.8) - 0.8	-	-	15	ns
Crystal Oscillator						
	Input: CRIN (external clock)					
V_{IL}	input voltage LOW		-0.3	-	0.3 x V_{DD}	V
V_{IH}	input voltage HIGH		0.7 x V_{DD}	-	V_{DD} + 0.3	V
I_{IN}	input leakage current		-10	-	+10	µA
C_{IN}	input capacitance		-	-	10	pF
	Output: CROUT	see Figure 3				
fc	crystal frequency	see Note 7	8	8.4672	35	MHz
g_m	mutual conductance at 100kHz		-	10	-	mA/V
A_V	small signal voltage gain	$A_V = g_m * R_O$	-	18	-	V/V
C_F	feedback capacitance		-	-	5	pF
C_{OUT}	output capacitance		-	-	10	pF

Notes:

1) Highest clock frequency at which data slicer produces 1010 output in analogue self-test mode.

2) V_{RL} = 0V, f_{sys}=4.2336MHz. The maximum input current depends on the value of the external resistor connected to IREFT.

   For D1 to D4: $I_{max} = 2.4 / R_{IREFT} \Rightarrow 2.4 / 220k = 10.9\mu A$.
   For R1 and R2: $I_{max} = 1.2 / R_{IREFT} \Rightarrow 1.2 / 220k = 5.45\mu A$.

3) Internal reference source with 32 different output voltages. Selection is achieved during a calibration period or via the serial interface. The values given are for an unloaded V_{RH}.

4) f_{ripple} = 1 kHz, V_{ripple} = 0.5 V_{p-p}.

5) V_{RH} = 2.5 V and V_{RL} = 0 V, measuring bandwidth: 200 Hz - 20 kHz, $f_{in(ADC)}$ = 1 kHz.

6) Gain of the ADC is defined as :

   G(ADC) = f_{sys}/I_{max} (counts/µA)
   Thus digital output = I_I x G(ADC) where:
   Digital output = the number of pulses at the digital output in counts/s and I_I = the DC input current in µA.
   The maximum input current depends on the system frequency (f_{sys}=4.2336MHz) and on V_{RH} - V_{RL}.
   The gain tolerance is the deviation from the calculated gain regarding Note 2.

7) It is recommended that the series resistance of the crystal or ceramic resonator is ≤ 60Ω.

10.2 Operating Characteristics (I2S Timing)

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0; T_{amb} = 5 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I^2S Timing; see Figure 28						
	Clock output: SCLK (C_L = 20pF)					
t_{PO}	output clock period	sample rate = fs	-	472.4	-	ns
		sample rate = 2 fs	-	236.2	-	ns
		sample rate = 4 fs	-	118.1	-	ns
t_{HC}	clock HIGH time	sample rate = fs	166	-	-	ns
		sample rate = 2 fs	83	-	-	ns
		sample rate = 4 fs	42	-	-	ns
t_{LC}	clock LOW time	sample rate = fs	166	-	-	ns
		sample rate = 2 fs	83	-	-	ns
		sample rate = 4 fs	42	-	-	ns
	Outputs: WCLK, DATA, EF (CL = 20pF)					
t_{ST}	setup time	sample rate = fs	95	-	-	ns
		sample rate = 2 fs	48	-	-	ns
		sample rate = 4 fs	24	-	-	ns
t_{HT}	hold time	sample rate = fs	95	-	-	ns
		sample rate = 2 fs	48	-	-	ns
		sample rate = 4 fs	24	-	-	ns

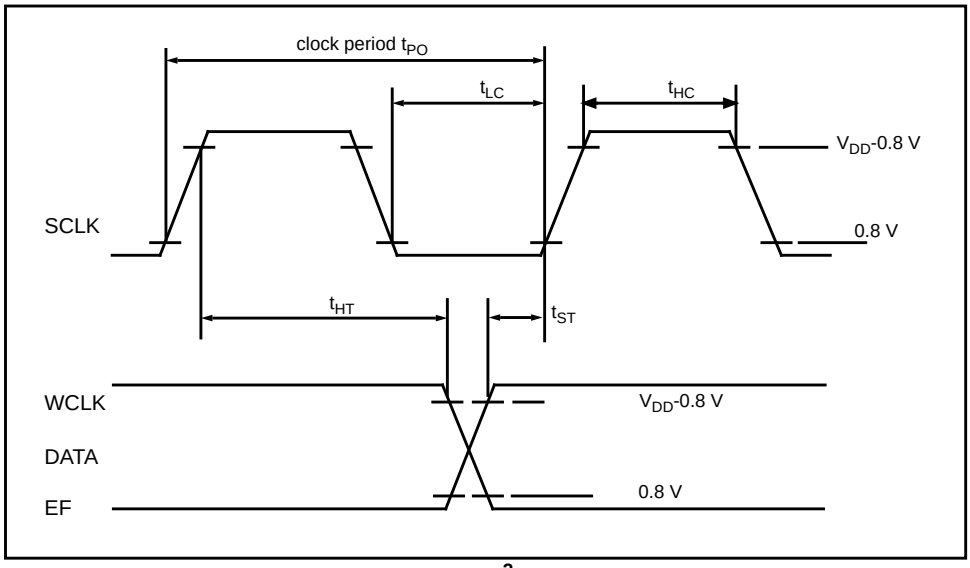


Figure 28 I^2S Timing

10.3 Operating Characteristics (µP Interface Timing)

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0; T_{amb} = 5 to 70 °C; unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
µP interface timing (writing to registers 0 to F; reading Q-channel subcode and decoder status) see Figure 29 and Figure 30.						
	Inputs SCL and RAB					
t_L	input LOW time		500	-	-	ns
t_H	input HIGH time		500	-	-	ns
t_R	rise time		-	-	480	ns
t_F	fall time		-	-	480	ns
	Read mode (CL = 20pF)					
t_{DRD}	delay time RAB to SDA valid		-	-	50	ns
t_{DD}	propagation delay SCL to SDA		700	-	980	ns
t_{DRZ}	delay time RAB to SDA hi-impedance		-	-	50	ns
	Write mode (CL = 20pF)					
t_{SD}	setup time SDA to SCL	note 1	-700	-	-	ns
t_{HD}	hold time SCL to SDA		-	-	980	ns
t_{SCR}	setup time SCL to RAB		260	-	-	ns
t_{DWZ}	delay time SDA hi-impedance to RAB		0	-	-	ns
µP interface timing (servo commands) see Figure 31 and Figure 32.						
	Inputs SCL and SILD					
t_L	Input LOW time		710	-	-	ns
t_H	Input HIGH time		710	-	-	ns
t_R	rise time		-	-	240	ns
t_F	fall time		-	-	240	ns
	Read mode (CL = 20pF)					
t_{DLD}	delay time SILD to SDA valid		-	-	25	ns
t_{DD}	propogation delay SCL to SDA		-	-	950	ns
t_{DLZ}	delay time SILD to SDA hi-impedance		-	-	50	ns
	Write mode (CL = 20pF)					
t_{SD}	set up time SDA to SCL		0	-	-	ns
t_{HD}	hold time SCL to SDA		950	-	-	ns
t_{SCL}	aet up time SCL to SILD		480	-	-	ns
t_{HCL}	hold time SILD to SCL		120	-	-	ns
t_{PLP}	delay between two SILD pulses		65	-	-	µs
t_{DWZ}	delay time SDA hi-impedance to SILD		0	-	-	ns

Notes: 1) Negative set-up time means that the data may change after clock transition.

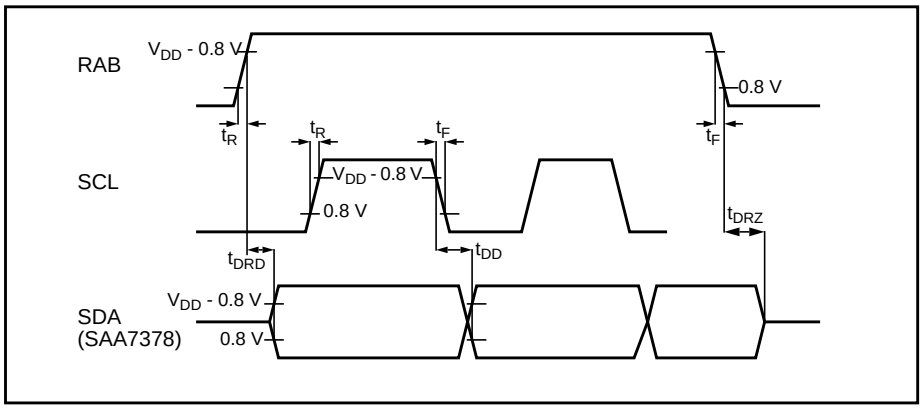


Figure 29 Microprocessor Timing (Q-channel subcode and decoder status information) - Read Mode

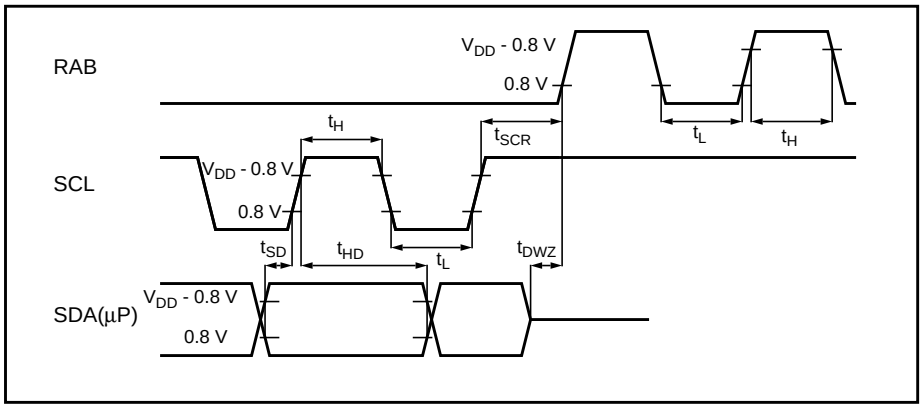


Figure 30 Microprocessor Timing (Registers 0 to E) - Write Mode

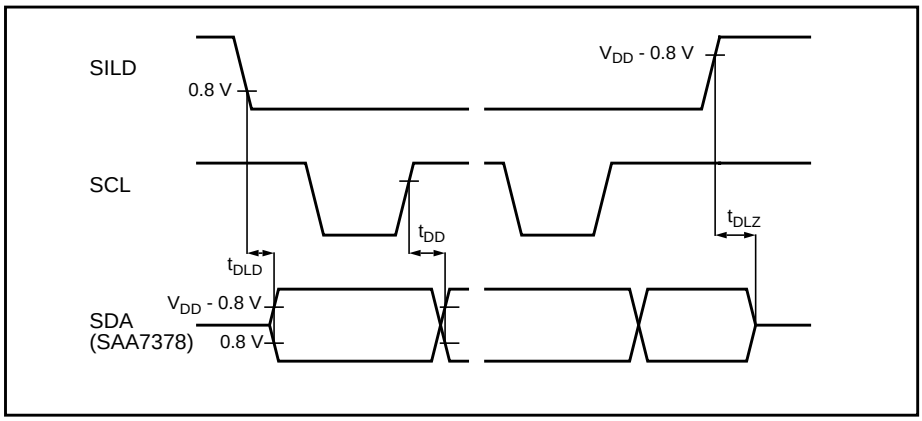


Figure 31 Microprocessor Timing (servo commands) - Read Mode

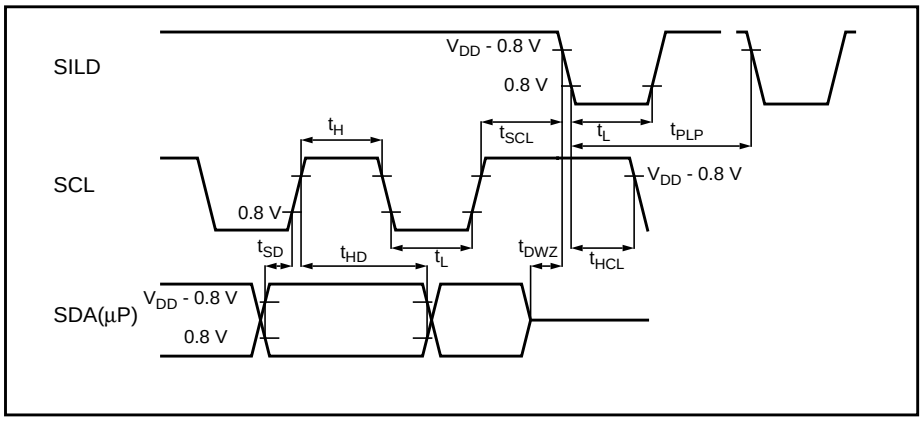
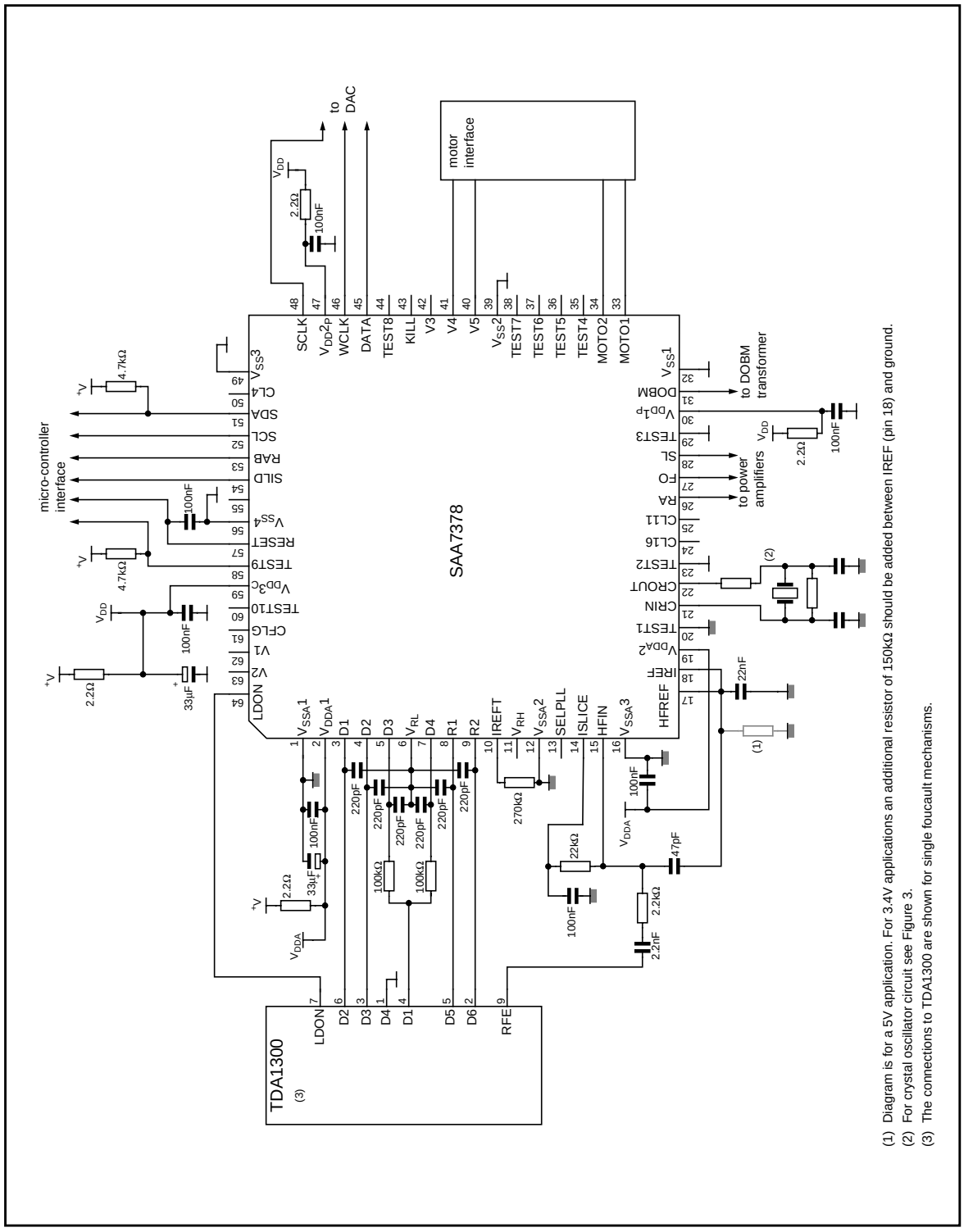


Figure 32 Microprocessor Timing (servo commands) - Write Mode

11. APPLICATION INFORMATION



(1) Diagram is for a 5V application. For 3.4V applications an additional resistor of 150kΩ should be added between IREF (pin 18) and ground.
(2) For crystal oscillator circuit see Figure 3.
(3) The connections to TDA1300 are shown for single foucault mechanisms.

Figure 33 Typical SAA7378 application diagram

12. PACKAGE OUTLINE

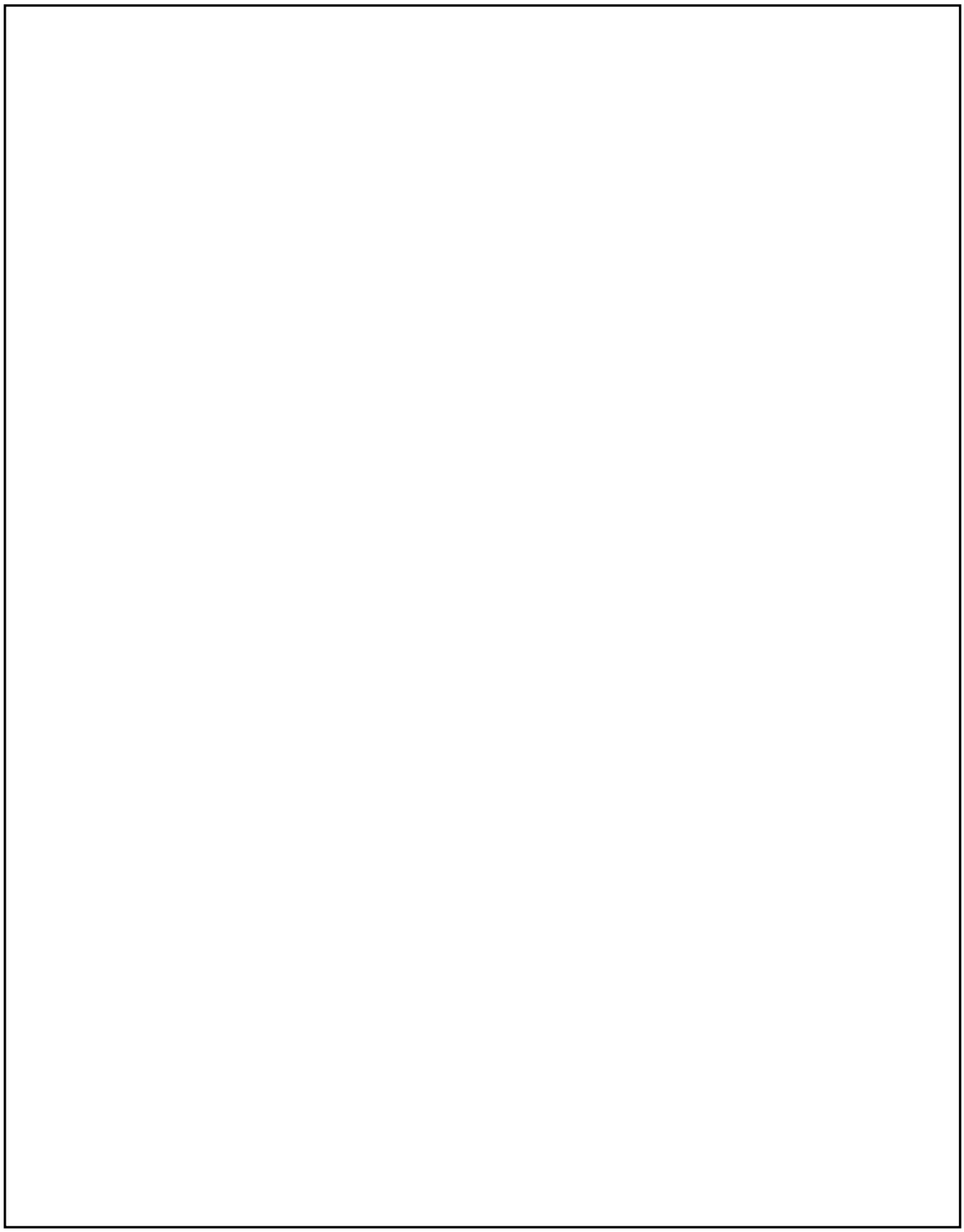


Figure 34 64-lead quad flat-pack; plastic (SOT393-1)

13. SOLDERING

13.1 Plastic quad flat-packs

13.1.1 BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is reccommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

13.1.2 BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Prehaeting is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

13.1.3 REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

14. DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

15. LIFE SUPPORT APPLICATIONS

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