AK4319A

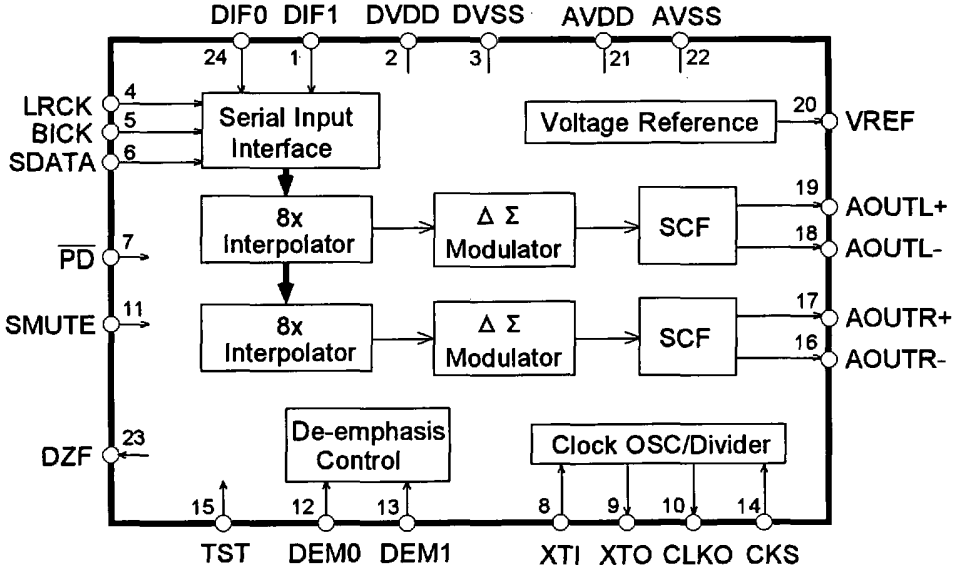
18Bit SCF DAC

General Description

The AK4319A is a high performance 1bit stereo DAC for digital audio systems. A 1bit DAC can achieve monotonicity and low distortion with no adjustment. On chip SCF filter makes the device less affected to the clock jitter and also suppresses the undesirable radio emission noise. The device equips differentially configurated output pins, but either of the pins can be used as single-end. The AK4319A achieves lower Out-band noise characteristic and it is suitable for digital broadcasting tuner and other digital audio applications.

Features

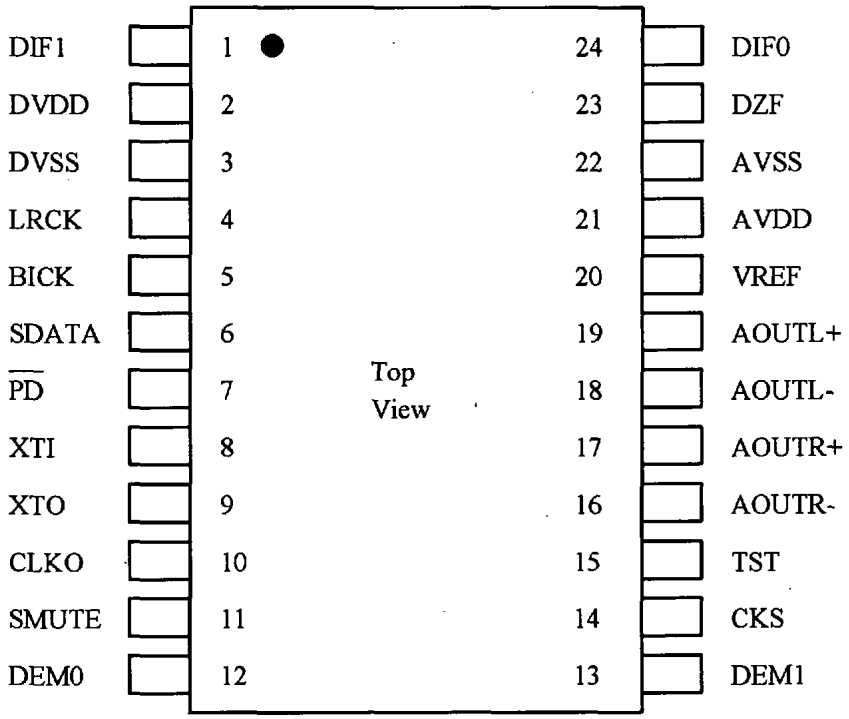
- ☐ Sampling Rate Ranging from 8kHz to 54kHz
- ☐ 128 times Oversampling
- ☐ 18bit 8 times Digital Filter
- ☐ 2nd order SCF with High Tolerance to Clock Jitter
- ☐ Differential outputs(Single-end use is available)
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ Soft mute
- ☐ I/F format : MSB justified, LSB justified, IIS
- ☐ THD+N: -87dB
- ☐ DR: 92dB
- ☐ Master Clock: 256fs or 384fs
- ☐ Power supply: 4.5 to 5.5V
- ☐ Small Package: 24pin SSOP
- ☐ AK4319 Compatible



■ Ordering Guide

AK4319AVM	-40~+85°C	24pin SSOP(0.65mm pitch)
AKD4319A	Evaluation Board	

■ Pin Layout



■ Different Points from AK4319

Parameter	AK4319	AK4319A
fs(min)	10kHz	8kHz
THD+N	-90dB	-87dB
DR	96dB	92dB
S/N	96dB	92dB

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DIF1	I	Digital Input Format Pin (Internal Pull-down pin)
2	DVDD	-	Digital Power Supply
3	DVSS	-	Digital Ground Pin
4	LRCK	I	L/R Clock Pin
5	BICK	I	Audio Serial Data Clock Pin
6	SDATA	I	Audio Serial Data Input Pin 2's complement MSB-first data is input on this pin.
7	$\overline{PD}$	I	Power-Down Mode Pin When at "L", the AK4319A is in power-down mode and is held in reset. The AK4319A should always be reset upon power-up.
8	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external CMOS clock can be input on XTI.
9	XTO	O	Crystal Oscillator Output Pin When an external clock is input, this pin should be left floating.
10	CLKO	O	Clock Output Pin The inverted XTI clock is output.
11	SMUTE	I	Soft Mute Pin (Internal Pull-down pin) When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
12	DEM0	I	De-emphasis Frequency Select Pin
13	DEM1	I	De-emphasis Frequency Select Pin
14	CKS	I	Master Clock Select Pin (Internal Pull-down pin) "L": MCLK=256fs,"H": MCLK=384fs
15	TST	I	Test Pin (Internal Pull-down pin) Must be left floating or tied to AVSS.
16	AOUTR-	O	Rch Negative analog output pin
17	AOUTR+	O	Rch Positive analog output pin
18	AOUTL-	O	Lch Negative analog output pin
19	AOUTL+	O	Lch Positive analog output pin
20	VREF	O	Voltage Reference Output Pin, 3.0V (typ, respects to AVSS) Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel witha 10uF electrolytic capacitor.
21	AVDD	-	Analog Power Supply Pin
22	AVSS	-	Analog Ground pin
23	DZF	O	Zero Input Detect Pin
24	DIF0	I	Digital Input Format Pin (Internal Pull-down pin)

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog Digital DVDD-AVDD	AVDD DVDD VDA	-0.3 -0.3 -	6.0 6.0 0.3	V V V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1 . All voltages with respect to ground..

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog (Note 2) Digital	AVDD DVDD	4.5 4.5	5.0 5.0	5.5 AVDD	V V

Notes:2 . AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 18bit Input Data; Measurement Bandwidth=10Hz~20kHz; $R_L \geq 5k\Omega$; unless otherwise specified)

Parameter	min	typ	max	Units
Resolution			18	Bits
Dynamic Characteristics (Note 3)				
THD+N (0dB Output)		-87	-80	dB
Dynamic Range (-60dB Output, A weight)	88	92		dB
S/N (A weight)	88	92		dB
Interchannel Isolation(1kHz)	90	100		dB
Interchannel Gain Mismatch		0.15	0.3	dB
DC Accuracy				
Gain Drift		100	-	ppm/°C
Output Voltage (Note 4)	±2.60	±2.80	±3.00	Vpp
Load Resistance	5			kΩ
Output Current			300	uA
Power Supplies				
Power Supply Current				
Normal Operation ($\overline{PD}$="H")				
AVDD		13	20	mA
DVDD		4	7	mA
Power-Down-Mode ($\overline{PD}$="L")				
AVDD+DVDD (Note 5)		10		uA
Power Dissipation (AVDD+DVDD)				
Normal Operation		85	135	mW
Power-Down-Mode (Note 5)		50		uW
Power Supply Rejection (Note 6)		40		dB

Notes:
3. Measured by AD725C(SHIBASOKU). Averaging mode. Refer to the eva board manual.
4. Full-scale voltage(0dB). When summing the differential outputs by unity gain, AOUT(typ.@0dB)=(AOUT+)-(AOUT-)= ±2.80Vpp*VREF/5.
5. In the power-down mode, all digital input pins including clock pins(XTI,,BICK,LRCK) are held DVDD or DVSS.
6. PSR is applied to AVDD,DVDD with 1kHz, 100mVpp.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=4.5V~5.5V; fs=44.1kHz; DEM0="1",DEM1="0")

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ±0.06dB (Note 7) -6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 7)	SB	24.1			kHz
Passband Ripple	PR			±0.06	dB
Stopband Attenuation	SA	43			dB
Group Delay (Note 8)	GD	-	14.7	-	1/fs
Digital Filter + SCF					
Frequency Response 0~20.0kHz		-	±0.2	-	dB

Note: 7. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.1dB), SB=0.546*fs.

8. The calculating delay time which occurred by digital filtering. This time is from setting the 16/18bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25°C; AVDD,DVDD=4.5~5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (XTI pin)	VIH1	70%DVDD	-	-	V
(All pins except XTI pin)	VIH2	2.2	-	-	V
Low-Level Input Voltage (XTI pin)	VIL1	-	-	30%DVDD	V
(All pins except XTI pin)	VIL2	-	-	0.8	V
AC coupled Input Voltage (XTI pin)	VAC	1	-	-	Vpp
High-Level Output Voltage (Iout=-100uA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100uA)	VOL	-		0.5	V
Input Leakage Current (Note 9)	Iin	-	-	±10	uA

Notes: 9. TST,SMUTE,DIF0,DIF1,CKS pins have internal pull-down devices, nominally 130kΩ.

SWITCHING CHARACTERISTICS

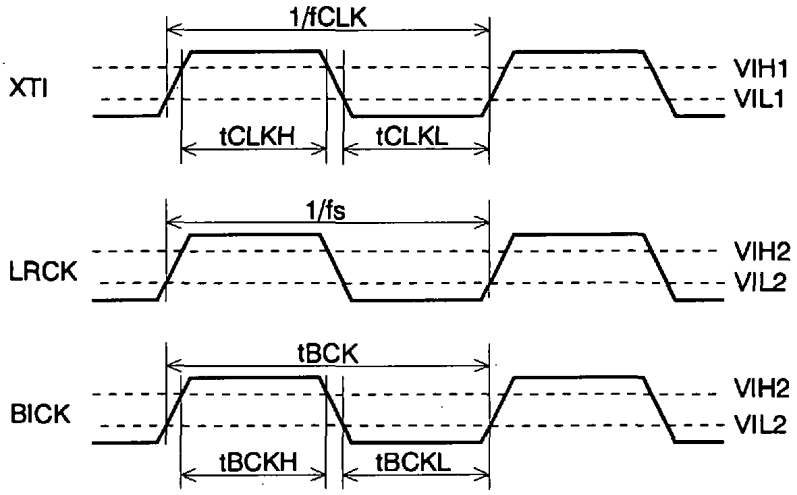
(Ta=25°C; AVDD,DVDD=4.5~5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
Master Clock Timing						MHz
Crystal Resonator	256fs:	fCLK	7.10		13.9	MHz
	384fs:	fCLK	10.70		20.7	MHz
External Clock	256fs:	fCLK	2.048		13.824	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	3.072		20.736	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
LRCK Frequency		fs	8	44.1	54	kHz
Duty Cycle		Duty	45		55	%
Serial Interface Timing						
BICK Period		tBCK	290			ns
BICK Pulse Width Low		tBCKL	100			ns
Pulse Width High		tBCKH	100			ns
BICK rising to LRCK edge	(Note 10)	tBLR	40			ns
LRCK Edge to BICK rising	(Note 10)	tLRB	40			ns
SDATA Hold Time		tSDH	40			ns
SDATA Setup Time		tSDS	40			ns
Reset Timing						
$\overline{PD}$ Pulse Width	(Note 11)	tPD	100			ns

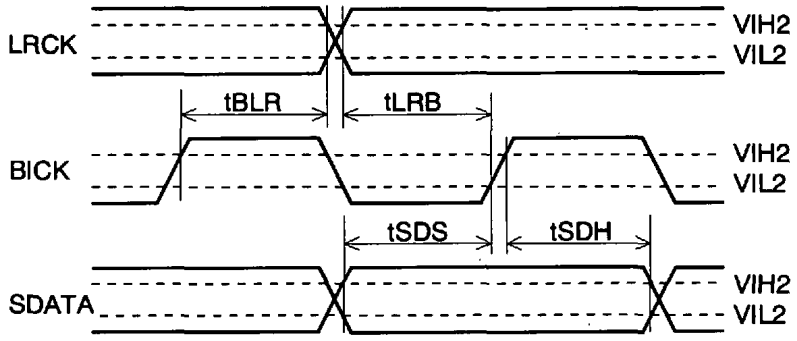
Notes: 10. BICK rising edge must not occur at the same time as LRCK edge.

11. The AK4319A can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

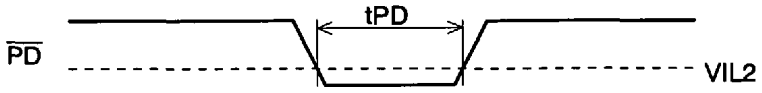
■ **Timing Diagram**



Clock Timing



Serial Interface Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4319A are XTI, LRCK, BICK. The master clock(XTI) should be synchronized with LRCK but the phase is not critical. The XTI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of XTI is determined by the sampling rate (LRCK) and CKS pin. Table 1 illustrates corresponding clock frequencies. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Refer to Figure 1 .

The master clock can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. Not only CMOS clock but sine wave signal with 1Vp-p can be input to the XTI pin by AC coupling. Table 1 illustrates corresponding clock frequencies used in each speed. When using internal oscillation, CLKO can not be used by external circuit at the power-down mode.

All external clocks(XTI,BICK,LRCK) should always be present whenever the AK4319A is in normal operation mode($\overline{PD}$="H"). If these clocks are not provided, the AK4319A may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4319A should be reset by $\overline{PD}$="L" after these clocks are provided. If the external clocks are not present, the AK4319A should be in the power-down mode($\overline{PD}$="L"). After exiting reset at power-up etc., the AK4319A is in power-down mode until XTI and LRCK are input.

Clock		frequency
LRCK (fs)		8k~540kHz
BICK		~64fs
MCLK	CKS="L"	256fs
	CKS="H"	384fs

Table 1 . System Clocks

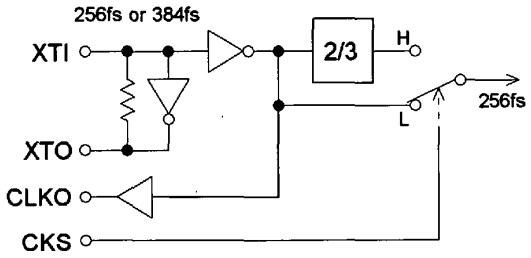


Figure 1 . Internal clock circuit

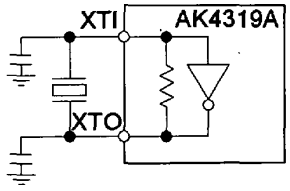


Figure 2 . X'tal resonator connection

■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Four serial data modes can be selected by the DIF0 and DIF1 pins as shown in Table 2 . In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16 MSB justified formats by zeroing the unused LSBs.

DIF1	DIF0	Mode	BICK	Figure
0	0	0: 16bit LSB Justified	≥32fs	Figure 2
0	1	1: 18bit LSB Justified	≥36fs	Figure 2
1	0	2: 18bit MSB Justified	≥36fs	Figure 3
1	1	3: I^2S Compatible	≥36fs or 32fs	Figure 4

Table 2 . Serial Data Modes

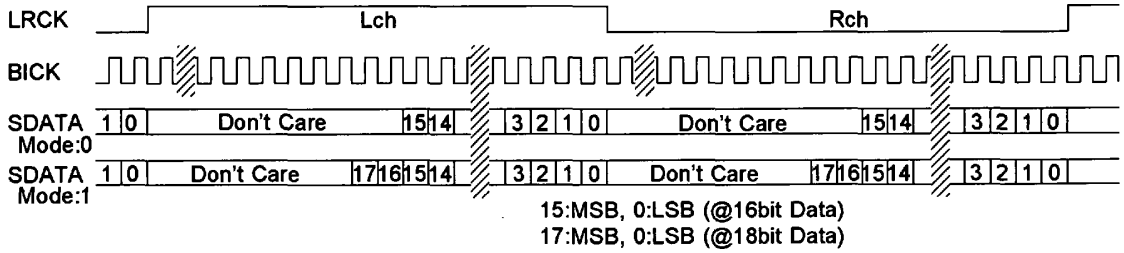


Figure 3 . Mode 0,1 Timing

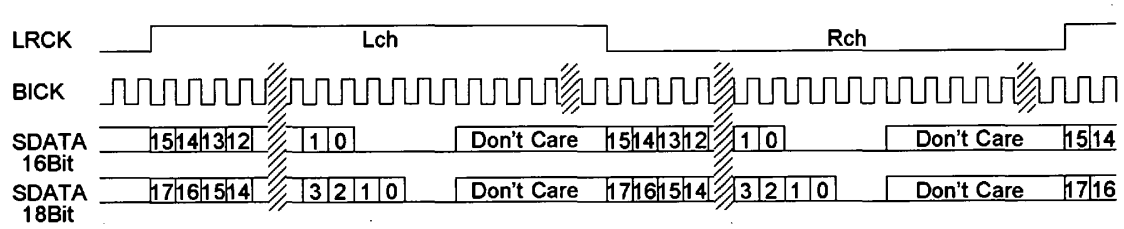


Figure 4 . Mode 2 Timing

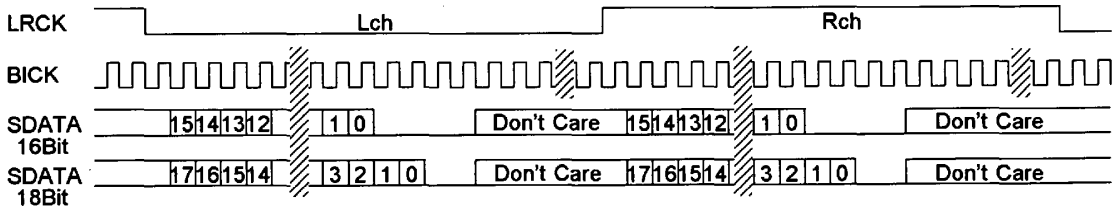


Figure 5 . Mode 3 Timing

■ **De-emphasis filter**

The AK4319A includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three sampling frequencies(32kHz,44.1kHz,48kHz). De-emphasis is enabled by the following two ways.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

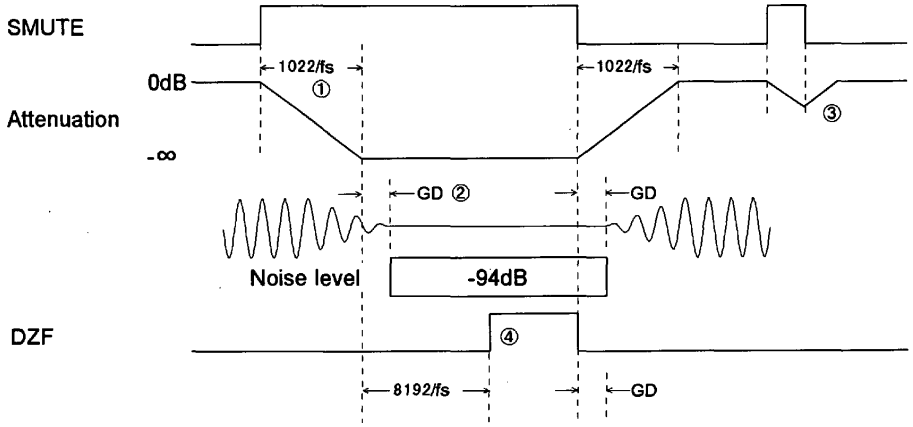
Table 3 . De-emphasis filter control

■ **Zero detection**

After the input data at both channels are continuously zeros for 8192 LRCK cycles or when the muting period exceeds 8192+1022 LRCK cycles, DZF goes to "H". DZF goes "L" immediately after non zero data is input or soft mute is released.

■ **Soft mute operation**

When SMUTE goes "H", the output signal is attenuated into -∞ during 1022 LRCK cycles. SMUTE is returned to "L", the mute condition is released and the output attenuation gradually changes to 0dB during 1022 LRCK cycles. If the soft mute is released within 1022LRCK cycles, the attenuation is recovered to 0dB with same gradient and cycles.
The soft mute function is effective when changing the signal source without stopping the signal transmission.



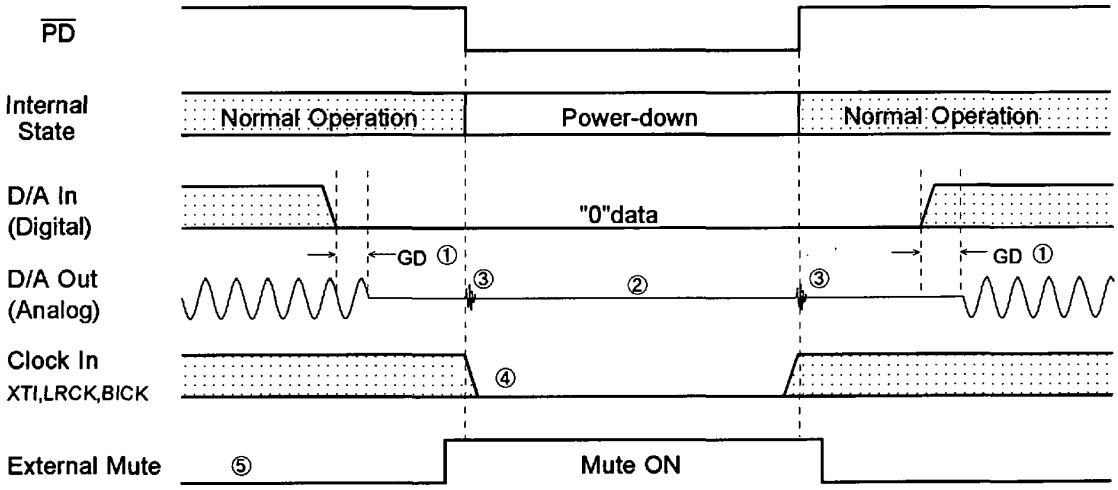
Notes:

① The output signal is attenuated into -∞ during 1022 LRCK cycles(1022/fs).
② Analog output corresponding to digital input have the group delay(GD).
③ If the soft mute is released within 1022 LRCK cycles, the attenuation is recovered to 0dB.
④ When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF goes "L" immediately after non-zero data is input.

Figure 6 . Soft mute and zero detection

■ **Power-Down**

The AK4319A are placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 7 shows an example of the system timing at the power-down and power-up.



① Analog output has the group delay(GD).
② When power-down is initiated, analog outputs are set into Hi-Z. Output noise level is about -110dB.
③ Some -50dB of click noise occurs at the transition("↑↓") of $\overline{PD}$ pin.
④ When the master clock is stopped, the AK4319A should have been in the power-down mode.
⑤ If the click noise(③)is a problem, an external mute circuit which generates above timing (⑤)is needed. Please refer to Figure 7 .

Figure 7 . Power-down/up sequence example

■ **System Reset**

The AK4319A should be reset once by bringing $\overline{PD}$ "L" upon power-up. The AK4319A is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by XTI. The AK4319A is in power-down mode until LRCK is input.

■ **External mute circuit**

Some click noise may occur at the transition("↑↓") of $\overline{PD}$ signal. The click noise of $\overline{PD}$ signal can be avoided by controlling the external mute circuit. The S/N of -110dB could be achieved by muting the analog outputs using DZF signal.

SYSTEM DESIGN

Figure 8 shows the system connection diagram. An example of external analog filter is shown in Figure 9 . An evaluation board[AKD4319A] is available in order to allow an easy study on the layout of a surrounding circuit.

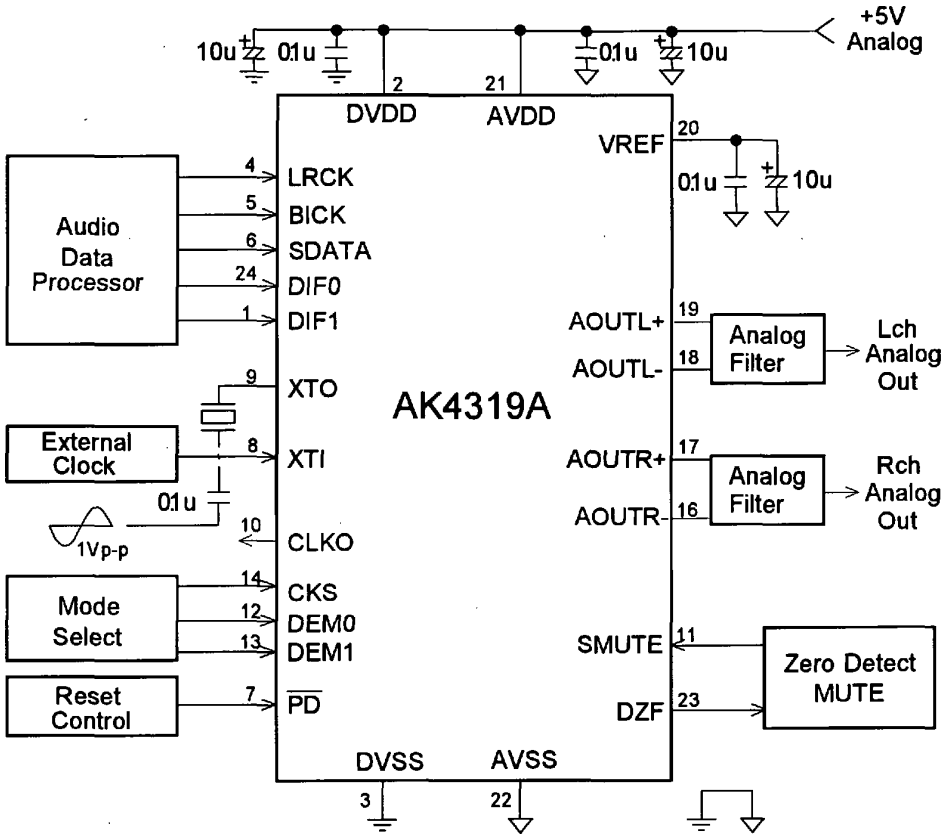


Figure 8 . Typical Connection Diagram

Notes:

- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except internal pull-down pins should not be left floating.

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD as shown in Figure 8 . Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

2. Voltage reference

The on-chip voltage reference is output on the VREF pin. An electrolytic capacitor smaller than 10uF in parallel with a 0.1uF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Especially, the ceramic capacitor should be connected to VREF pin within a few mm as near as possible. No load current may be taken from the VREF output pin. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the AK4319A.

3. Analog Outputs

The analog signals are output from the differential output pins of each channel, therefore they are summed externally. The analog outputs are the differential voltage,ΔVAOUT=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. The bias voltage(Vop/2) for this summing circuit is supplied externally. The output signal range is ±1.40V(0.99Vrms, typ) centered at an internal common voltage(AVDD/2). If the summing gain is 1, the output range is ±2.80V (1.98Vrms, typ). The input data format is 2's complement. The output voltage(ΔVAOUT) is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal ΔVAOUT is 0V for 0000H(@16bit).
DC offsets on analog outputs are eliminated by AC coupling the signals since DAC outputs have a few mV offsets.

The noise generated by the delta-sigma modulator beyond the audio passband is sufficiently attenuated by the high speed over-sampling and by the on-chip SCF filter. However, as the outband noise moves into the audible band at low sampling rate, careful attention is required. On Figure 9 , the differential outputs of AK4319A are summed by the
1st-order LPF and the 1.98Vrms output signal range is acquired.

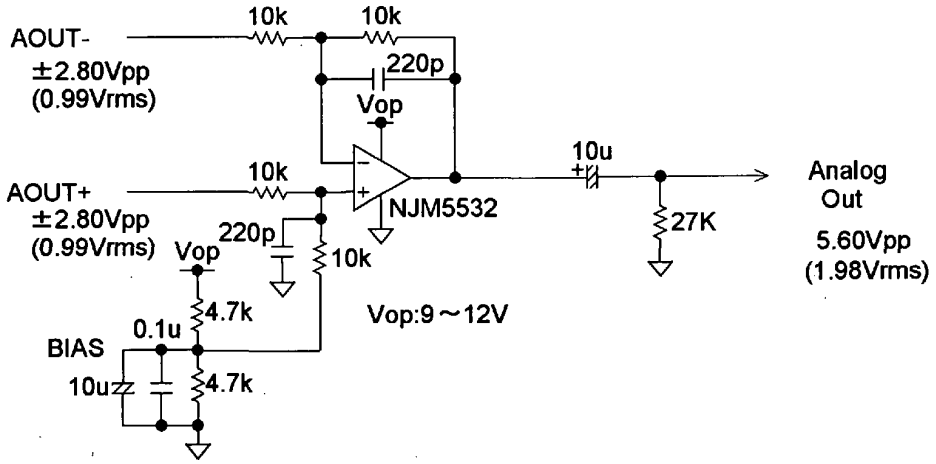


Figure 9 . External LPF example

4. Single-end usage

The load impedance for the output pin should be higher than 5kΩ. When the AK4319A drives some capacitive load, series resistor(220ohm or more than) should be added the analog output and it should be connected to the analog output pin as near as possible. The output pin which is not used could be left open. When the AK4319A is used as a single-end configuration, the analog characteristics (such as THD+N, DR, S/N) may degrade by 1dB.

For single-end operation, in the circuit example of Figure 9 , DC isolation capacitance is added between AOUT- and 10kΩ. Then the 10kΩ resistor which is connected to AOUT+ is removed. In this case, the output level becomes 0.99Vrms. With a single-end configuration, the AK4319A interfaces directly to external circuit such as volume AMP, which simplifies the circuit.

Figure 10 shows a circuit example for single end operation. The series resistor should be connected to the AOUT pin as near as possible. The operation mode setting in this circuit is as follows.

[Operation mode]
- fs=44.1kHz
- De-emphasis ON/OFF for fs=44.1kHz
- Data format: Mode 0, 16bit LSB justified
- BICK: 64fs
- MCLK: 256fs

[Performancet example]
- THD+N: -86dB
- DR,S/N: 91dB

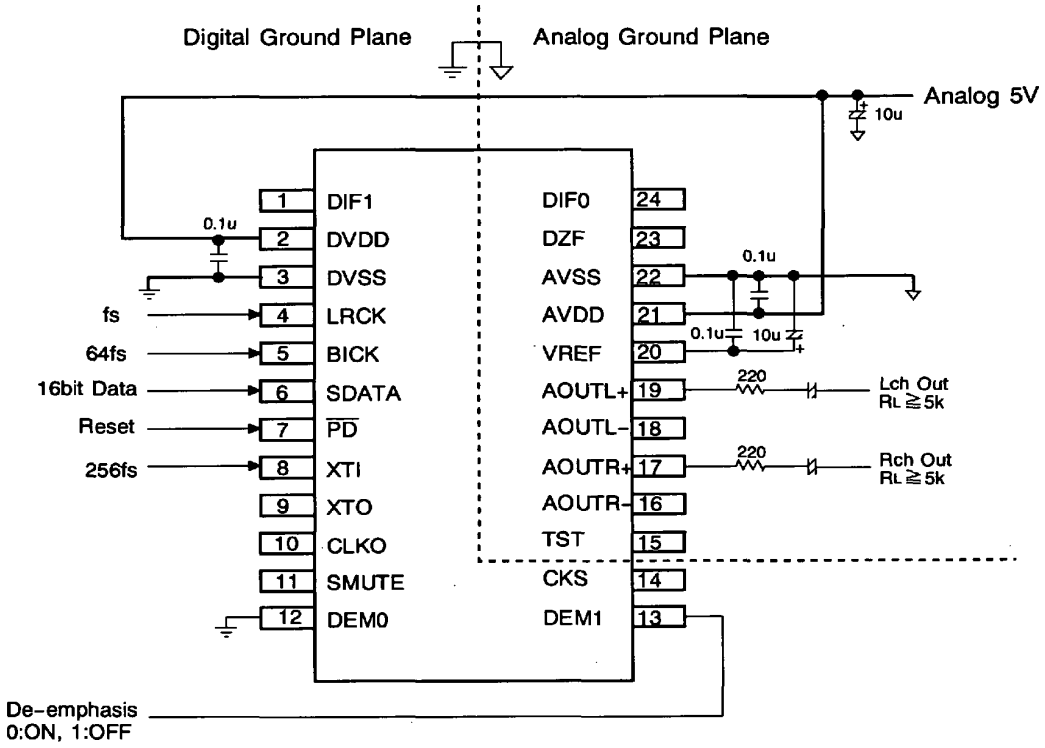
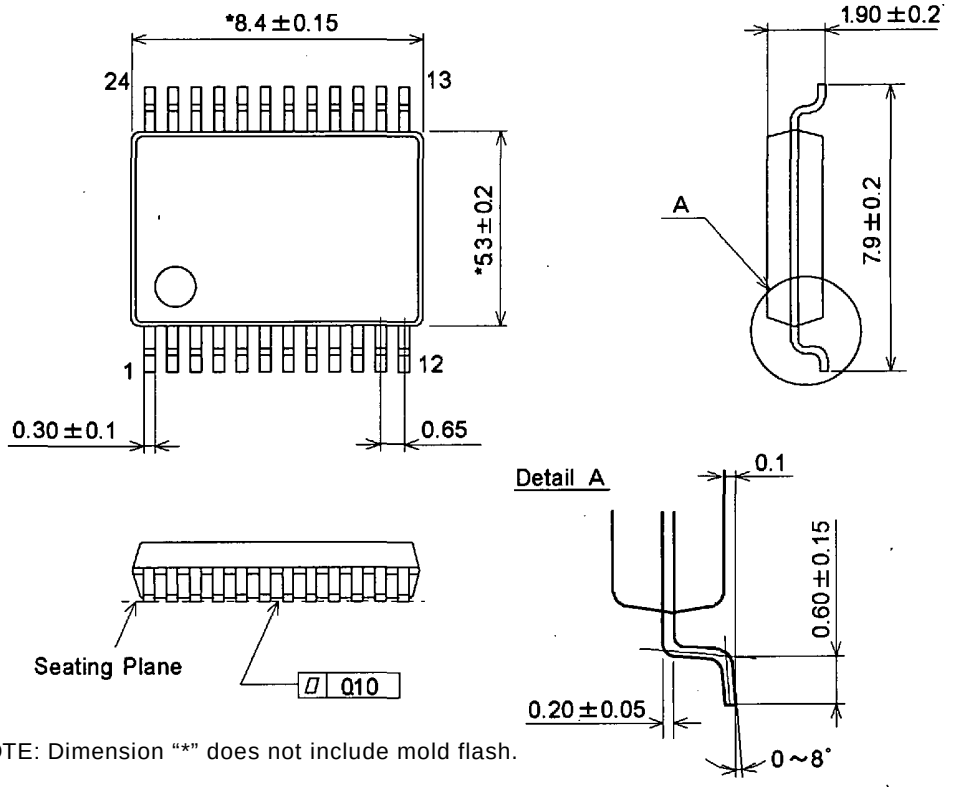


Figure 10 . System Connection External for single end operation

PACKAGE

● **24pin SSOP (Unit: mm)**

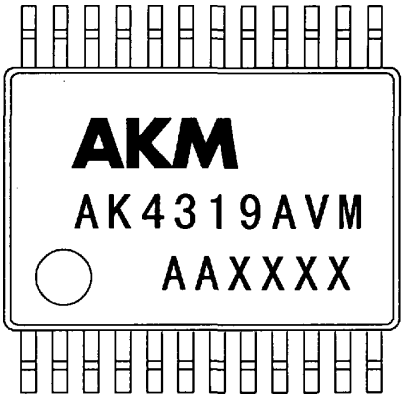


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXX
AA: Lot#
XXXX: Date Code

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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.