LSI LOGIC
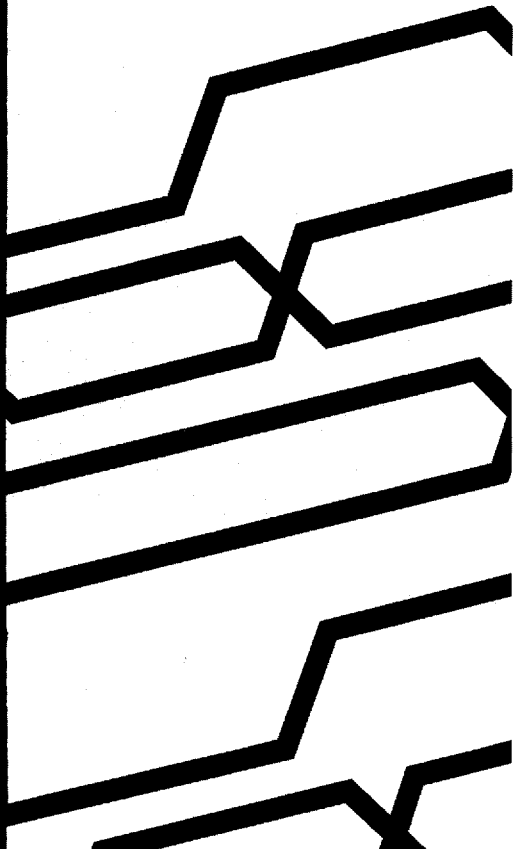
L64111
MPEG Audio Decoder
Technical Manual

September 1993

This document is preliminary. As such, it contains data derived from functional simulations and performance estimates. LSI Logic has not verified either the functional descriptions, or the electrical and mechanical specifications using production parts.

First Edition
MD72-000101-99 A
This document applies to revision B of the L64111 MPEG Audio Decoder and to all subsequent versions unless otherwise indicated in a subsequent edition or an update to this edition of the document.

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Preface

This book is the primary reference and technical manual for the L64111 MPEG Audio Decoder. It contains a complete functional description for the L64111 and includes complete physical and electrical specifications for the L64111.

Audience

This book assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the L64111 for possible use in a system
- Engineers who are designing the L64111 into a system

Organization

This book has the following chapters:

- Chapter 1, **Introduction**, describes the general characteristics and capabilities of the L64111 and provides an introduction to relevant MPEG concepts.
- Chapter 2, **Audio Decoder Functional Overview**, describes L64111 interfaces and discusses the chip's internal architecture and functions.
- Chapter 3, **Audio Decoder Signal Descriptions**, details the operation of each L64111 interface signal.
- Chapter 4, **Registers**, describes the L64111 registers and their usage.
- Chapter 5, **Specifications**, lists the electrical and mechanical characteristics of the product.
- Chapter 6, **Applications**, presents the designs of several applications.

Related Publications

ISO/IEC JTC 1/SC 29 Coded Representation of Picture, Audio and Multimedia/Hypermedia Information: MPEG CD 11172 Part 1 - Systems, Part 2 - Video, and Part 3 - Audio.

Conventions Used in this Manual

The following signal naming conventions are used throughout this manual:

■ A level-significant signal that is true or valid when the signal is LOW always has an overbar ($\overline{}$) over its name.

■ An edge-significant signal that initiates actions on a HIGH-to-LOW transition always has an overbar ($\overline{}$) over its name.

Hexadecimal numbers are indicated by the prefix "0x" before the number—for example, 0x32CF. Binary numbers are indicated by the subscripted "$_2$" following the number—for example, 1101_2.

The first time a word or phrase is defined in this manual, it is *italicized*.

Contents

Chapter 1
Introduction

Chapter 1 introduces the LSI Logic L64111 MPEG Audio Decoder and presents an introduction to MPEG technology. The L64111 is a single chip handling all aspects of the MPEG audio decoding process.

This chapter contains four sections:

■ Section 1.1, L64111 Features

■ Section 1.2, MPEG Overview

■ Section 1.3, MPEG Audio Encoding

■ Section 1.4, Transmission of MPEG Data

1.1
L64111 Features

The L64111 MPEG Audio Decoder is a single LSI component combining an ISO 11172 MPEG system stream decoder and an MPEG audio decoder.

Figure 1.1 is a block diagram of the L64111. The L64111 can accept either serial or parallel digital MPEG audio data. The L64111 contains an internal DRAM controller, which interfaces with external DRAM to provide memory for a Channel Buffer.

The L64111 can be used in stand-alone and controller-based applications, such as digital cable decoders, CD players, digital VCRs, digital direct-broadcast satellite decoders, laser disk players, CD ROM players, and workstations.

Figure 1.1
L64111 Interface
Signals
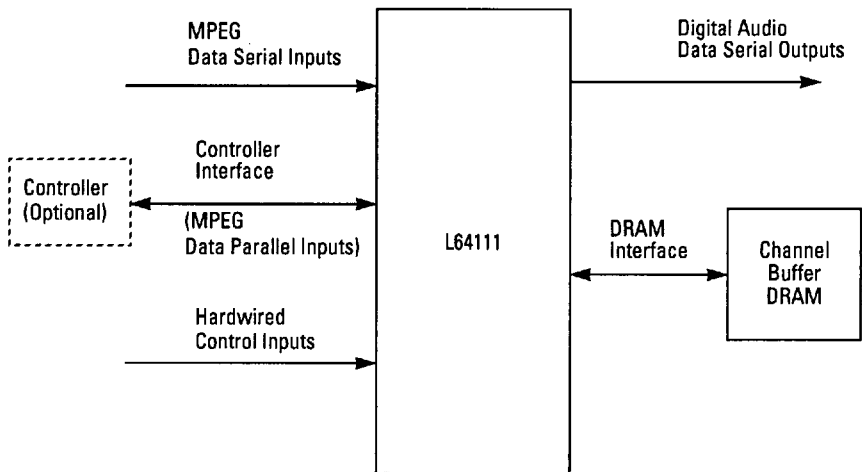
The key features of the L64111 are:

■ complies with ISO CD 11172-1 and CD 11172-3 specifications for decoding of MPEG 90/265 Layers I and II audio bitstreams

■ receives and handles MPEG ISO System Stream pack

■ handles MPEG audio stream (audio frame) packet

■ handles up to 15 Mbit/s (sustained rate) bitstream parsing

■ decodes/reconstructs MPEG-1 audio stream Layers I and II in real-time

■ supports data rates up to 192 Kbit/s monaural and 384 Kbit/s stereo/dual channel

- MUSICAM compatible at selected bitrates

- operates with or without an external system microcontroller

- handles 8- or 16-bit data through the external controller interface

- simple interface to external Channel Buffer using a single 256K x 4 100 ns fast page mode DRAM

- supports more than one second of delay for audio/video synchronization

- includes registers for cue and review control and output data rate control

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1.2
MPEG Overview

The ISO/IEC Motion Pictures Expert Group (MPEG) first proposed the JTC1/SC2/WG11 standard for coding of moving pictures and associated audio for use with digital storage media in 1990. Though a full discussion of MPEG is beyond the scope of this document, this section summarizes concepts common to both MPEG audio and video applications.

MPEG is a standard for the representation of compressed audio and video signals. It allows for:

- Data interchange between compatible systems

- Standardized decoding methodologies

Given an *elementary stream* of data (for audio data, this is called an *audio stream*), an MPEG encoder first digitally compresses and codes the data. The MPEG algorithm offers a choice of levels of complexity and performance for this process. (See Section 1.3, "MPEG Audio Encoding," for more information.)

To prepare a stream of compressed audio data for transmission, it is formatted into *audio frames*. Each audio frame contains audio data, error-correction data, and optional user-defined *ancillary data*. The audio frames are then sent in *packets* grouped within *packs* in an ISO MPEG *System Stream*. (See Section 1.4, "Transmission of MPEG Data," for more information.)

The packs in system streams may contain a mix of audio packets and video packets for one or more channels. Packs may contain packets from separate elementary streams. Thus, MPEG can easily support multiple

channels of program material, and a decoder given access to a system stream may access large numbers of channels.

On the receiving end, MPEG audio decoding involves:

- identifying and removing a channel's audio frames from the audio packets in the System Stream

- managing the temporary storage of frames

- applying appropriate algorithms for decoding the audio frames

- merging decoded audio frames back into continuous audio

- limiting the effect of transmission errors

The LSI Logic L64111 MPEG Audio Decoder is a single-chip solution that performs all MPEG-1 Audio Layer I and II decoding operations in real time. The L64111 produces decoded audio data in industry-standard Pulse Code Modulation (PCM) serial format, allowing the use of commodity parts (PCM DACs) for audio output.

The following two sections discuss the two major parts of MPEG audio processing in more detail.

1.3 MPEG Audio Encoding

MPEG audio encoding is intended to efficiently represent a digitized audio stream by removing redundant information. Because different applications have different performance goals, MPEG uses different encoding techniques. These techniques, called *Layers*, provide different trade-offs between compression and signal quality. The MPEG algorithm uses the two following processes for removing redundant audio information:

- Coding and quantization
- Psychoacoustic modelling

Coding and quantization are techniques that are applied to data that has been mapped into the frequency domain and filtered into subbands.

Psychoacoustic modeling is a technique that determines the best allocation of data within the available data channel bandwidth based on human perception.

The general structure of an MPEG encoder is shown in Figure 1.2.

Figure 1.2
Audio Encoding
Process (Simplified)

Digitized
Audio
Input

→ Frequency
Filter Bank
(Mapping)

→ Bit
Allocation
Processor

(Among
Subbands,
Coding,
Quantizing)

→ Bitstream
Formatter →

Psychoacoustic
Model
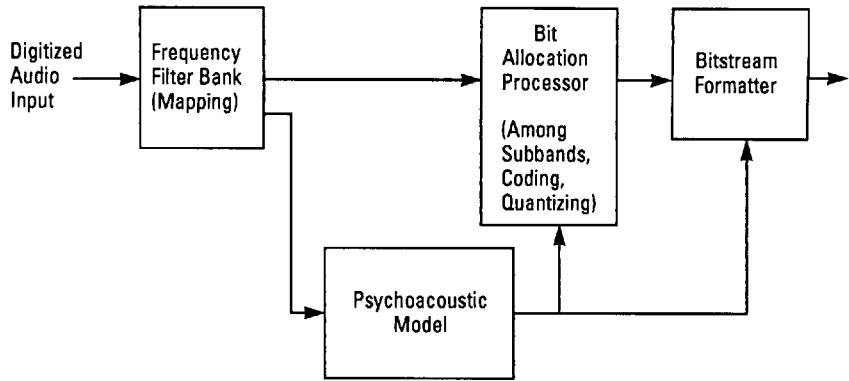
1.4
Transmission of
MPEG Data

This section discusses formatting and transmission of MPEG-encoded data.

Once audio data has been coded, it may be stored or transmitted digitally. MPEG provides a framework for use of packet-oriented transmission of compressed data. In particular, ISO CD 11172 defines formats for digital data streams for both video and audio. The ISO System Stream format is designed to accommodate both audio packets and video packets within the same framework for transmission.

An ISO System Stream contains data in a specified sequential format. The data may be physically delivered in parallel form or serial form. The following discusses how the L64111 decoder accepts and handles data streams at the physical and the logical level.

L64111 MPEG
Data Input

The L64111 provides the following formats for MPEG data:

■ Parallel input through a microcontroller interface

■ Serial input through a dedicated serial link

Parallel Data Input. In order to be compatible with computer and storage media applications, the L64111 accepts parallel data through its Controller Interface. For more details on the Controller Interface, refer to the discussions in Chapters 2 and 3.

Serial Data Input. In order to be compatible with data transmission applications, the L64111 has a dedicated serial link interface to handle coded data, which is typically provided in bit-serial fashion.

ISO System Streams

This subsection discusses MPEG system syntax. The highest level MPEG syntax is the ISO System Stream. The System Stream is composed of a sequence of packs, as shown in Figure 1.3.

Figure 1.3
ISO System Stream

Pack ► ◄ Pack

| Pack Layer Header | System Header Packet | Packet (first) | more Packets (variable #) | Packet (last) | ISO 11172 end code |

. . .

Contains:
Pack Start Code (32 bits), System Clock Reference (128 bits)

Contains:
Various data, including system stream ID

Contains:
Audio stream data (in audio frames)
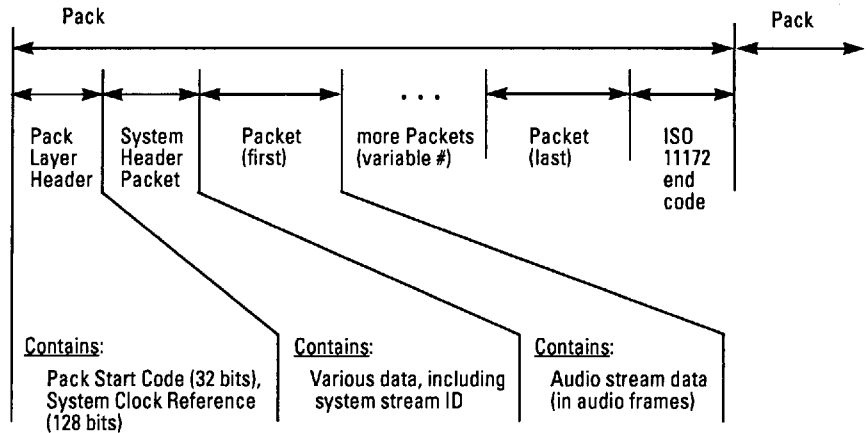
An MPEG pack is composed of a *pack layer header*, a *system header packet*, a sequence of *packets*, and ends with an ISO 11172 *end code*. The pack layer header contains a pack start code used for synchronization purposes, and a system clock value. The system header packet contains a variety of housekeeping data and in particular contains a system stream ID used to differentiate multiple system streams. A sequence of one or more packets contains either encoded audio or encoded video stream data. The ISO 11172 end code is the final element in an MPEG pack.

For detailed definition of pack headers, refer to the ISO CD 11172-1 system stream descriptions. The following section describes MPEG packets in more detail.

MPEG Packets

Any one MPEG packet carries either audio or video data, but not both simultaneously. An MPEG Audio Packet contains an audio packet header and one or more Audio Frames. Figure 1.4 shows the packet structure.

Figure 1.4
MPEG Audio Packet
Structure
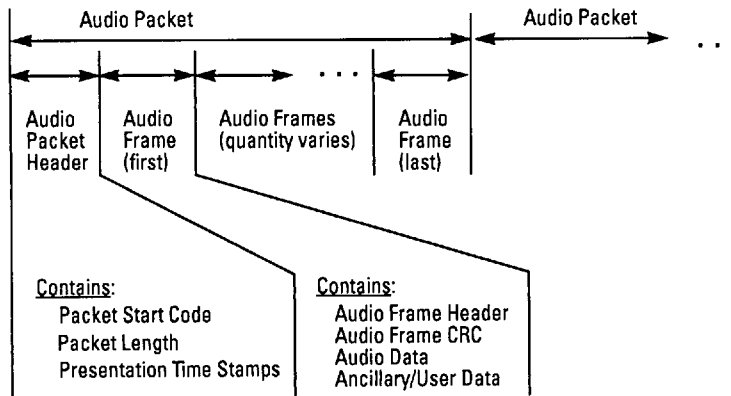
Audio Packet Header. An audio packet header contains the following:

■ Packet Start Code

Identifies this as an audio packet. The Packet Start Code also contains a five-bit audio stream identifier that may be read by the user to identify the audio channel.

■ Packet Length

Indicates the number of bytes remaining in the audio packet

■ Presentation Time Stamps (PTS)

These time stamps (PTS) are optional. The L64111 makes the PTS data available to the user through registers.

Audio Frame. An Audio Frame contains a slice of the audio data stream together with some supplementary data. Audio frames have the following elements:

■ Audio Frame Header

Table 1.1 shows the audio frame header structure:

Table 1.1
Audio Frame Header
Structure

Data Field	Size	Purpose
Sync Word	12 bits	Has a fixed value of 0xFFF. The decoder uses the sync word to synchronize with the data stream.
ID	1 bit	The decoder uses the ID to identify whether the data is MPEG coded or not.
Layer Type	2 bits	Defines whether data is encoded as Layer I, II, or III.
Protection Bit	1 bit	A CRC is included in the data stream.
Bitrate Index	4 bits	Defines an index into a table defining the bit rate.

(Sheet 1 of 2)

Table 1.1 (Continued) *Audio Frame Header* *Structure*	Data Field	Size	Purpose
	Sampling Frequency ID	2 bits	Identifies the sampling frequency.
	Padding Bit	1 bit	Adds additional bytes to an audio frame to match the sample rate to the bit rate.
	Private Bit	1 bit	User definable spare bit.
	Channel Mode	2 bits	Identifies whether the channel data is stereo, joint stereo, dual channel, or monaural.
	Mode Extension	2 bits	Used only in joint stereo mode. Indicates joint stereo subbands.
	Copyright	1 bit	Flags whether the data stream contains copyrighted material.
	Original/Home	1 bit	Indicates whether this data stream is an original or a copy.
	Emphasis	2 bits	Indicates the type of de-emphasis to be used.

(Sheet 2 of 2)

■ Audio Frame Cyclic Redundancy Code (CRC)

This field contains a 16-bit checksum, which can be used to detect errors in the audio frame header.

■ Audio Data

The L64111 uses the audio data to reconstruct the sampled audio data. Its format is beyond the scope of this document. The data structures for Layer I dual channel/stereo, intensity stereo, and for the more complex Layer II audio data fields are described in Sections 2.4.1.5 and 2.4.1.6 of the ISO CD 11172-3.

■ Ancillary Data

The final field in an audio frame contains user-defined data (ancillary data).

Chapter 2
Audio Decoder
Functional Overview

Chapter 2 describes the features, major internal architecture, and general
internal operation of the L64111 MPEG Audio Decoder. Additional
application-specific material is given in Chapter 6, "Applications."

■ Section 2.1, L64111 Features

■ Section 2.2, L64111 Internal Organization

■ Section 2.3, Decoding Details

■ Section 2.4, Rate Control and Clock Granularity

2.1
L64111 Features

The L64111 can be used in environments ranging from stand-alone to controller-based, as well as in a workstation or embedded application. Applications for the L64111 include digital cable decoders, CD players, digital VCRs, digital direct-broadcast satellite decoders, laser disk players, CD ROM players, and multimedia workstations.

Data Input

The L64111 decoder can accept MPEG coded data in serial or parallel form. In Bypass mode, the L64111 routes input data unprocessed to the output. The L64111 can accept parallel data in either 8-bit or 16-bit form from a system controller.

Control and Processing

The L64111 parses ISO Systems Streams and also accepts Audio Streams.

The decoder can parse system bitstreams at rates up to 15 Mbits/second (depending on system clock speed), store and catalog audio frames in its external channel buffer, and provide presentation time stamp information for audio-video synchronization.

Control

The L64111 may be used either as a stand-alone processor or with a system controller (microcontroller or microprocessor). The controller interface supports 8- or 16-bit data transfers. The L64111 obtains decoding information directly from the data stream. A controller may supply optional parameters for decoder synchronization, error correction, and frequency selection. When operating stand-alone, the L64111 uses default parameters.

Channel Buffer Capability

The L64111 requires an external channel buffer for temporary storage of audio frames that have been removed from the stream. The L64111's internal DRAM controller requires just one external component: a 256K x 4 fast page mode DRAM. The channel buffer can handle at least one second of data, which facilitates audio-video synchronization or other delay compensation.

Audio-Video Synchronization

Synchronization of audio and video streams requires that an external system controller monitor the video and audio presentation time stamps. The decoder delays audio frames (stores them in the buffer) until the controller determines that the correct presentation time has been reached. At this point the controller commands the L64111 to start decoding from data in the channel buffer. Using the 256K x 4 Channel Buffer, the decoder can compensate for at least one second of delay between audio and video data.

Processing

The L64111 completely integrates and automates the process of decoding Layer I or Layer II streams.

Output

The L64111 provides a 16-bit PCM output by means of a multiplexed serial output bus compatible with commodity PCM serial D to A converters (DACs). A bypass command allows four-wire PCM serial audio data to be passed directly from serial input to serial output with only a multiplexer delay.

Error Handling

The L64111 provides the ability to conceal errors in data. When this function is enabled, two choices of response to error are provided:
(1) repeat of last error-free audio frame, or (2) muting.

Synchronization

A multipass synchronization mechanism minimizes frame synchronization errors. With this technique, successive valid syncs must be acquired before synchronization is established.

2.2
L64111 Internal
Organization

When initialized, the L64111 synchronizes itself by monitoring the data stream and locating an audio frame in the data stream. When MPEG data is input, the chip strips away all unneeded information, retaining only the audio and control data. The audio and control data is then partially expanded and stored in a channel buffer. When the appropriate control signals are seen, this stored data is played; that is, decompression is performed and the data is output in PCM format.

Figure 2.1 shows the L64111's internal architecture. The functions of the main elements are discussed after the figure.

Figure 2.1
L64111 Internal
Architecture

HDMUTE
BYPASS

Serial Input:
MPEG Encoded
PCM Unencoded

SERI
SCLKI
LRCLKI
WCLKI

Set SERO to 0 — HDMUTE

BYPASS

Serial Output:
SERO
SCLKO
LRCLKO
WCLKO

4

4

4

Output
Multiplexer

4

CTL Signals

PCM

ERROR

PCM Counter Input

4

PCM
Serial
Converter

16-bit
Format
PCM
Serial
Data

SSEL

Ancillary
Data
FIFO
16 x 8

RESET

SYSCLK

READ

D[15:0]

A[4:0]

AS

CSLDS

CSUDS

STARTI

STARTO

DTACK

Controller
Interface
and
Input/Output
Control
Registers

Play
Director

Decoder

1024 x 24
Vector
RAM

Audio
Frames

T/C, Param,
Errors

Data

FALF

FEMPTY

FALE

INTR

Input Data
FIFO
128 x 8

Data

Pre-parser

DRAM
Controller

Timing
and CTL

Audio
Frames

RAS, CAS, WE
BD[3:0]
BA[8:0]

DRAM
256K x 4   OE

Channel Buffer

Controller Interface and Input Data FIFO

Data enters the L64111 in parallel through the Controller Interface, or in serial through the serial port. The data is first synchronized to the system clock (SYSCLK), then sent to the Input Data FIFO. The FIFO buffers the data and supplies it to the Pre-parser. Various flags signal the extent to which the buffer is full or empty. The flags are made available for flow control. The input FIFO is not part of the channel buffer, and its flags do not reflect the state of the channel buffer.

Figure 2.2
Input Data FIFO

Flag: Input Data FIFO Buffer

FALF ◄──────────────
        (FIFO Almost Full)
        @ 32 bytes from top

                                         128 bytes

FALE ◄──────────────
        (FIFO Almost Empty)
        @ 32 bytes from bottom

FEMPTY ◄──────────────
        (FIFO Empty)   @ bottom
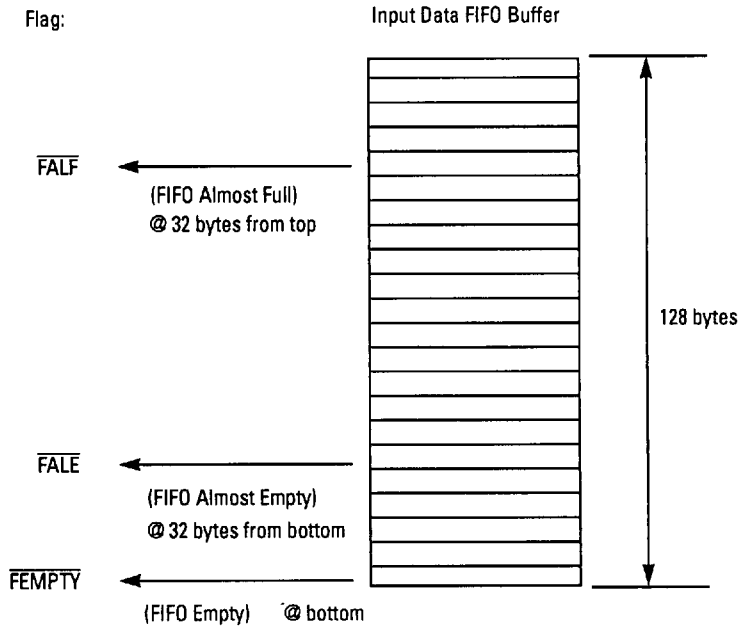
Pre-parser

The Pre-parser performs stream parsing. For ISO System Stream parsing and synchronization, the Pre-parser detects the pack start code or system header start code and uses one of these to synchronize to the ISO stream.

The Pre-parser then looks for packet header information and attempts packet identification. It identifies audio frame information and discards all else. Next, it calculates the CRC and separates the header information from the audio data and sends the audio data to the channel buffer.

Decoder	The decoder receives data from the Channel Buffer and fully decodes the data using the MPEG algorithm. The reconstructed data is then sent into the PCM Serial Converter.
DRAM Controller	The DRAM Controller handles the read/write and refresh activities of the external Channel Buffer DRAM. The Channel Buffer stores blocks of partially decoded audio data prior to their reconstruction in the decoder.
Play Director	The Play Director maintains a list of the frames in the Channel Buffer. It also holds certain header information required to complete the decoding operation of each frame. The frames are normally accessed as a circular buffer. It is possible to skip or replay frames (cue and review) while they are in the Play Director. The Play Director is also used in error concealment.
PCM Serial Converter	The 16-bit reconstructed stereo pair is output in a PCM format compatible with most serial D to A converters. Various modes are supported.
Output Multiplexer	The Output Multiplexer controls routing of serial data signals. It can be program-controlled or hardwired to select one of the following three outputs:

- SERO set to zero
- Unprocessed input data (passed through unchanged)
- PCM format output of decoder

In Bypass Mode, the L64111 passes all four PCM inputs unaltered to the output. All signals retain their temporal alignment.

2.3 Decoding Details

The decoder can operate with bit rates up to 384 Kbits/second stereo or dual channel with sampling frequencies of 32 KHz, 44.1 KHz, or 48 KHz. Once the decoder has started decoding, it takes data from the Channel Buffer. The decoder uses a two-pass system, as described in the following paragraphs.

In the first pass, the decoder parses the bitstream, separating out the sync, header information, allocations, and scalefactors, performs the CRC check, and removes ancillary data.

In the second pass, the decoder provides degrouping, inverse quantization, scaling, and subband synthesis. By performing two passes, the decoder can mask errors by repeating the same frame, and the two-pass approach allows identifying false audio syncs.

Figure 2.3
Decoder Audio
Stream Processing
Flow Chart
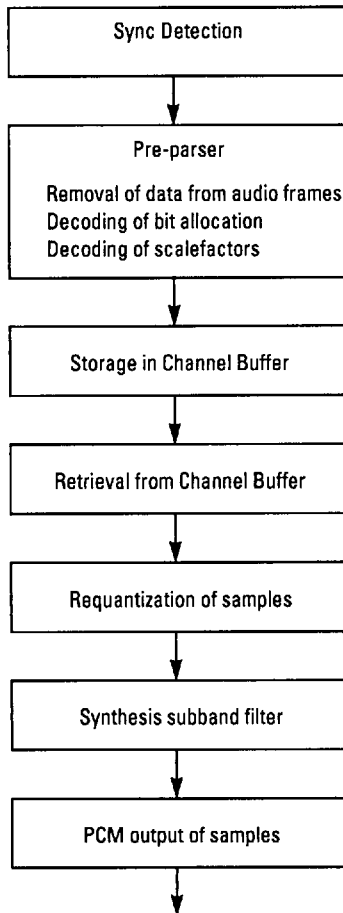
2.4
Rate Control and
Clock Granularity

Rate control is the ability of the decoder to deliver a continuous PCM output correctly timed while the input is coming in bursts. The rate control mechanism has two parts.

The first part is the Input Data FIFO. Part of this FIFO compensates for the variations in processing time for different parts of the Pre-parser. The rest of this FIFO allows data burst rates up to 7.5 Mbytes/second (60 Mbits/second) for a length of 128 bytes, until the Pre-parser processes this data at its 15 Mbit/second rate. These rates are valid for SYSCLK of 30 MHz.

The second channel rate control is the Channel Buffer. This buffer is filled at a 15 Mbit/second rate and is emptied at the PCM output sample rate.

There is a mechanism which allows the output sample rate to be accurately derived from the device clock. It is also possible to periodically correct the output sample rate for timebase drift between the encoder and the decoder in systems where they do not share a common clock.

Chapter 3
Audio Decoder
Signal Descriptions

Chapter 3 describes all L64111 interface signals. These descriptions are useful for hardware designers who are interfacing the L64111 with other devices.

This chapter contains the following sections:

■ Section 3.1, Digital Audio Data Serial Inputs

■ Section 3.2, DRAM Interface

■ Section 3.3, Controller Interface

■ Section 3.4, FIFO Status Indicators

■ Section 3.5, Other Control Signals

■ Section 3.6, PCM Audio Outputs

Figure 3.1 is the logic symbol for the L64111.

Figure 3.1
L64111 Logic Symbol
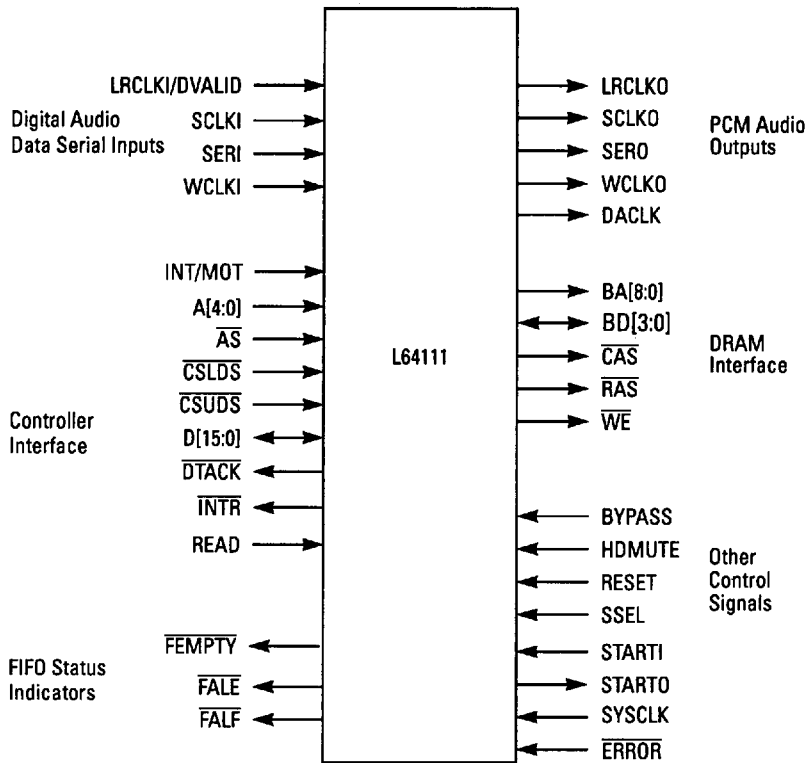
3.1 Digital Audio Data Serial Inputs

The Digital Audio serial inputs can accept MPEG or PCM serial data. The L64111 uses the serial data input when either the SSEL pin and/or the SER/PAR register bit is HIGH, or if the device is in Bypass mode. Otherwise, data on these inputs is ignored.

LRCLKI/DVALID

| Data Valid | Input |

When Bypass mode is inactive, this signal acts as DVALID. When DVALID is asserted by an external device, data on SERI is valid and is clocked into the L64111 on the next rising edge of SCLKI, which allows easy demultiplexing of multiple independent streams of serial data, or masking data (parity bits, for example) which is not part of the MPEG stream.

When the L64111 is in Bypass mode, this signal acts as LRCLKI. LRCLKI does not affect the data on SERI. During bypass, LRCLKI

is connected to LRCLKO through a multiplexer. A HIGH indicates that the SERI input contains left channel data; a LOW indicates that SERI contains right channel data. The data rate on this input is usually SCLKI/16.

SCLKI   **Serial Clock In**   **Input**
The L64111 samples SERI, DVALID, and $\overline{\text{ERROR}}$ on the rising edge of SCLKI. SCLKI can be asynchronous to SYSCLK up to a maximum frequency determined by device characterization, but it can never be more than twice the frequency of SYSCLK. The clock does not need to be periodic.

In Bypass mode, SCLKI is connected to SCLKO through a multiplexer.

SERI   **Serial Data In**   **Input**
Data on the Serial Data In pin is latched on the rising edge of SCLKI in the cycles where DVALID is HIGH. Serial Data In may be from either an MPEG system stream or an MPEG audio stream

In Bypass mode, SERI is connected to SCLKO through a multiplexer.

WCLKI   **Word Clock In**   **Input**
WCLKI is an optional PCM input and is not used internally by the L64111.

In Bypass mode, WCLKI is connected to WCLKO through a multiplexer.

3.2
DRAM Interface

The L64111 interfaces directly to DRAM, which is used for a Channel Buffer. The DRAM is required for the L64111 to operate properly.

BA[8:0]   **Buffer Address**   **Output**
BA[8:0] are multiplexed address lines to the Channel Buffer DRAMs. When the L64111 asserts $\overline{\text{RAS}}$, BA[8:0] contain the row address. When the L64111 asserts $\overline{\text{CAS}}$, BA[8:0] contain the column address. The L64111 contains address line drivers so that no external components are required to drive the DRAM.

BD[3:0]   **Buffer Data**   **Bidirectional**
BD[3:0] are bidirectional data lines between the L64111 and the Channel Buffer DRAM.

$\overline{\text{CAS}}$ **Column Address Strobe**   **Output**
$\overline{\text{CAS}}$ is the DRAM column address strobe. When asserted LOW, $\overline{\text{CAS}}$ indicates that BA[8:0] contain the column address.

$\overline{\text{RAS}}$ **Row Address Strobe**   **Output**
$\overline{\text{RAS}}$ is the DRAM row address strobe. When asserted LOW, $\overline{\text{RAS}}$ indicates that BA[8:0] contain the row address.

$\overline{\text{WE}}$ **Write Enable**   **Output**
The L64111 asserts $\overline{\text{WE}}$ LOW to write data into the Channel Buffer DRAM. The L64111 reads data from the Channel Buffer DRAM when both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are LOW with $\overline{\text{WE}}$ HIGH.

**3.3
Controller
Interface**

This section describes the signals for the controller interface.

A[4:0]   **Address Bus**   **Input**
A[4:0] are address lines that provide access to the L64111 internal registers. Refer to Table 4.1 on page 4-3 for a listing of the registers and their respective addresses.

$\overline{\text{AS}}$ **Address Strobe**   **Input**
When $\overline{\text{AS}}$ is asserted LOW, the L64111 latches the address on A[4:0]. $\overline{\text{AS}}$ may be tied to $\overline{\text{CSLDS}}$ if no $\overline{\text{AS}}$ signal is available from the system controller.

$\overline{\text{CSLDS}}$ **Chip Select and Lower Data Strobe**   **Input**
$\overline{\text{CSLDS}}$ is the active-LOW chip select and data strobe for the least significant eight bits of the data bus (low byte).

$\overline{\text{CSUDS}}$ **Chip Select and Upper Data Strobe**   **Input**
$\overline{\text{CSUDS}}$ is the chip select and data strobe for the most significant eight bits of the data bus (high byte). When using 16-bit data on D[15:0], this strobe must always occur simultaneously with, or be preceded by, $\overline{\text{CSLDS}}$. If operating with an eight-bit controller, this pin should be tied HIGH.

D[15:0]   **Data Bus**   **Bidirectional**
D[15:0] are bidirectional data bits. D[15:8] are the high byte; D[7:0] are the low byte. When operating in eight-bit mode only the low byte is used. Refer to Section 4.2, "Data Register," on page 4-3 for more information.

$\overline{\text{DTACK}}$ **Data Acknowledge**   **Output**
$\overline{\text{DTACK}}$ is the active-LOW data acknowledge signal to the external controller. It is asserted for at least one cycle for every transaction

over the controller interface, and remains LOW until the end of the transaction and after both $\overline{CSUDS}$ and $\overline{CSLDS}$ have been deasserted. Note that the L64111 still asserts $\overline{DTACK}$ on a write even if the Input Data FIFO is full and the write has resulted in an overflow.

INT/MOT   **Interface Mode Select**   **Input**

When Interface Mode Select is tied HIGH, the L64111 latches data on the falling edge of READ during write cycles. When tied LOW, it latches data on the rising edge of READ during write cycles. This pin should not be toggled during normal operation.

$\overline{INTR}$ **System Interrupt**   **Output**

The L64111 asserts $\overline{INTR}$ LOW to flag an interrupt. $\overline{INTR}$ is an open drain output and requires a 1 Kohm pullup resistor to VCC. Pulling up $\overline{INTR}$ allows multiple interrupts to be wire-ORed.

READ   **Read**   **Input**

The system controller asserts READ (HIGH) when reading from the L64111 and deasserts READ (LOW) when writing to the L64111. The system controller must assert $\overline{AS}$ and $\overline{CSLDS}$ during both read and write operations to the L64111.

**3.4
FIFO Status
Indicators**

The FIFO status flags operate in both serial and parallel input modes. The input FIFO and the channel buffer are unrelated, so these flags do not reflect the state of the channel buffer.

$\overline{FALE}$ **FIFO Almost Empty Flag**   **Output**

The L64111 asserts $\overline{FALE}$ LOW to indicate that the L64111's internal 128-byte Input Data FIFO is almost empty—there are only 32 bytes of data left in the buffer (see Figure 3.2). It is *not* an error to let the FIFO empty completely.

$\overline{FALF}$ **FIFO Almost Full Flag**   **Output**

The L64111 asserts $\overline{FALF}$ LOW to indicate that the L64111's internal 128-byte Input Data FIFO is almost full—there are only 32 unused bytes left in the buffer (see Figure 3.2). It is an error to let the FIFO overflow.

$\overline{FEMPTY}$ **FIFO Empty Flag**   **Output**

The L64111 asserts $\overline{FEMPTY}$ LOW to indicate that the L64111's internal 128-byte Input Data FIFO is empty and new data should be provided to the FIFO (see Figure 3.2). It is *not* an error to let the FIFO empty completely.

Figure 3.2
Input Data FIFO
and Flags
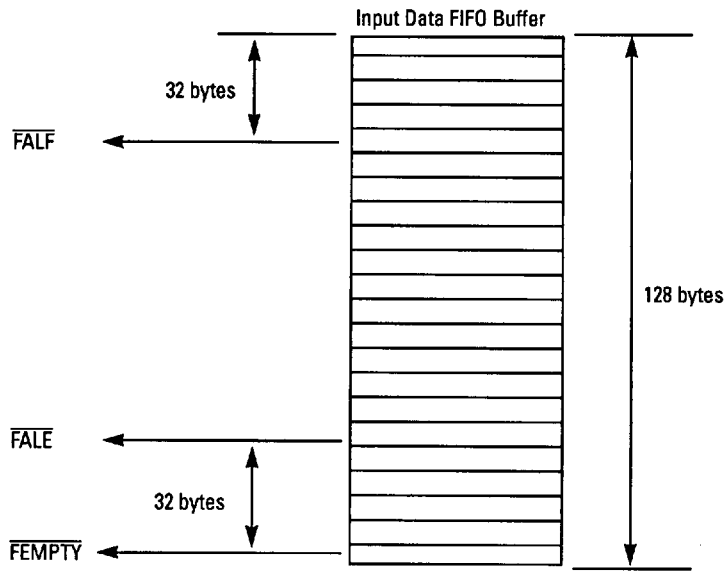
3.5 Other Control Signals

This section describes the remaining L64111 control signals.

BYPASS   **Decoder Bypass**   **Input**

If BYPASS is set to one, all serial inputs (SERI, SCLKI, DVALID, and WCLKI) are routed directly to their respective outputs (SERO, SCLKO, LRCLKO, and WCLKO) with hard mute still functional. Note that there is no buffering of PCM input data in the channel buffer. In Bypass mode, the L64111 does not process data from the serial data input.

If BYPASS is set to zero, the L64111 processes the data from the serial input.

Bypass mode can also be selected by writing to the BYPASS bit in Control Register 1, in which case the BYPASS pin should be tied LOW.

ERROR   **Error Indication**   **Input**

A LOW on the Error Indication pin indicates that the data on SERI has an error. Error Indication is used by the L64111 to conceal errors in the stream. A LOW on this pin also forces the L64111 to search for the next sync code as soon as it is released. ERROR can be connected to an error correction chip in the channel that is capable of flagging an uncorrectable error. The error indication is propagated internally along with the data.

HDMUTE Hard Mute   **Input**
When HDMUTE is asserted HIGH, the L64111 forces the PCM output to zeros.

Mute operation can also be selected by writing to the SOFT_MUTE bit in Control Register 2, in which case the HDMUTE pin may be tied LOW.

RESET   Reset   **Input**
The L64111 resets after RESET has been asserted HIGH for two clock cycles. RESET can be tied permanently LOW if the system controller software has been set up to assert the SOFT_RST bit in Control Register 1 through the controller interface.

SSEL   Serial Select   **Input**
The SSEL input selects the L64111's source of data. If SSEL is HIGH, the decoder accepts the serial data entering through input pins SERI, SCLKI, and DVALID. If SSEL is LOW, the decoder accepts data in parallel format from the Controller Interface data lines.

Serial selection can also be done by writing to the SER/PAR bit in Control Register 1, in which case this pin may be tied LOW.

STARTI   Start In   **Input**
When Start In is asserted HIGH, the L64111 begins to decode the data in its Channel Buffer. The L64111 may also be started by writing to the STARTI bit in Control Register 1, in which case this pin may be tied HIGH.

STARTO   Start Out   **Output**
The STARTO pin is provided for designs having multiple MPEG audio decoders that must be synchronized. When using more than a single L64111, connect STARTO of the first device to STARTI of the second device, as illustrated in Figure 3.3. STARTO is asserted HIGH when device begins decoding stored frames from the channel buffer.

SYSCLK   System Clock   **Input**
System Clock is a 50% duty cycle clock which is at least 384 times the maximum L64111 output sample frequency. System Clock should have crystal accuracy for best audio quality.

Figure 3.3
Use of STARTI and
STARTO Signals

First Decoder

Next Decoder
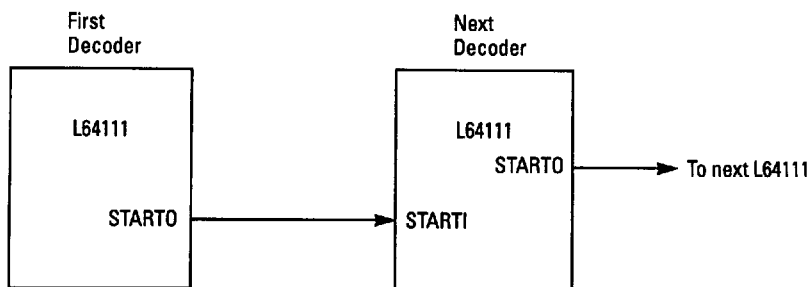
3.6 PCM Audio Outputs

The functions of the PCM Audio Output pins may be programmed to support a variety of common D to A converters.

DACLK **DAC Clock Out**   **Output**
DACLK is a clock which is half the frequency of SYSCLK. DACLK can be used to clock certain oversampling DACs.

LRCLKO **Left/Right Channel Indicator Out**   **Output**
LRCLKO indicates whether the current data output on SERO is left channel (LRCLKO = HIGH) or right channel (LRCLKO = LOW) information. In Bypass mode, the LRCLKO pin is a reflection of DVALID.

SCLKO **Serial Bit Clock Out**   **Output**
SCLKO is the bit clock for the serial data on SERO. In Bypass mode this pin is a reflection of SCLKI.

SERO **Serial Data Out**   **Output**
A serial 16 bit word, sign extended with MSB first, for each of the left and right channels, synchronized to SCLKO. The actual format may be programmed through the system interface. In Bypass mode this pin is a reflection of SERI.

WCLKO **Word Clock Out**   **Output**
Transitions from HIGH to LOW on both edges of LRCLK. This signal is synchronized to SCLKO. In bypass mode, the WCLKO pin is a reflection of WCLKI.

Chapter 4
Registers

Chapter 4 discusses the L64111's internal registers. These registers config-
ure and control the operation of the L64111, and monitor the operating sta-
tus of the L64111. This chapter contains the following sections:

■   Section 4.1, Register Operation and Summary

■   Section 4.2, Data Register

■   Section 4.3, Control Registers

■   Section 4.4, Interrupt Registers

■   Section 4.5, Timer Countdown and Offset Registers

■   Section 4.6, Parametric Data Word Registers

■   Section 4.7, Presentation Time Stamp (PTS) Registers

■   Section 4.8, Ancillary/User Data FIFO

■   Section 4.9, Channel Buffer Registers

4.1
Register
Operation and
Summary

The L64111 can operate either as a stand-alone device or in applications that use a system controller. In stand-alone operation, the L64111 operates according to the register field default values except as noted later.

Operating the L64111 with a system controller allows the full range of operating capabilities. A system controller provides register values and interrupt processing control. A system controller is typically used when it is necessary to synchronize audio and video decoders, or provide operating parameter value flexibility. A system controller can also convert ancillary data in the audio stream to text for visual display.

Table 4.1 lists the L64111's registers. Note that registers designated as read-only must not be written, because the write capability of certain registers may be reserved for use only with test parameters.

Table 4.1
L64111 Registers

Address A[4:0]	Register Name	Description	Read / Write Capability
0	Data	Data input	Write-only
1	Control Register 1	Configuration	Read / Write
2	Control Register 2	Configuration	Read / Write
3	Control Register 3	Configuration	Read / Write
4	Interrupt and Status Register 1	Contains status of interrupt sources; allows enabling/disabling interrupt sources	Read / Write
5	Interrupt and Status Register 2	Contains status of interrupt sources; allows enabling/disabling interrupt sources	Read / Write
6	Timer Countdown Register (TCR)	Reference Value for Clock Divider	Read / Write
7	Timer Offset Register H (TORH)	High Byte of Timer	Read / Write
8	Timer Offset Register L (TORL)	Low Byte of Timer	Read / Write
9	Parametric Data Word 1	Audio Frame Header Information	Read-only
10	Parametric Data Word 2	Audio Frame Header Information	Read-only
11	Parametric Data Word 3	Audio Frame Header Information	Read-only
12	Presentation Time Stamp 1	PTS lowest byte	Read-only
13	Presentation Time Stamp 2	PTS data	Read-only
14	Presentation Time Stamp 3	PTS data	Read-only
15	Presentation Time Stamp 4	PTS data	Read-only
16	Presentation Time Stamp 5	PTS highest byte	Read-only
17	Ancillary/User Data FIFO	Used for access to output of FIFO	Read-only
18	Channel Buffer Status Counter	Channel Buffer Storage Capacity	Read-only
19	Channel Buffer Write Counter	Pointer to the next write	Read / Write
20	Channel Buffer Read Counter	Pointer to the next read	Read / Write
21-31	Reserved		

4.2 Data Register

The L64111 has one Data Register. The Data Register is connected to Controller Interface pins D[15:0]. The L64111 transfers parallel MPEG data through this register.

Address A[4:0] = 00000₂

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
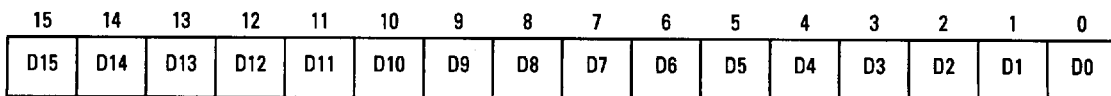
Low byte used for register access and
for MPEG data in eight-bit parallel format

MPEG data can also be written by the controller to this register in 16-bit parallel format

Data   **Data**   **[15:0]**
The Data Register is write-only. The usable width of this register
is either 8 or 16 bits, depending on the setting for the width of
the Controller Interface data path, which is controlled by bit 4
(SEL_16/8_BIT) of Control Register 2.

When eight-bit I/O is selected, the Data Register accepts the
lowest eight data bits D[7:0] from the Controller Interface data
pins; the highest eight bits are ignored. Eight-bit width mode is
automatically selected on reset.

When the L64111 is set for 16-bit I/O, all Controller Interface
data bits D[15:0] are accepted. 16-bit I/O is useful for increased
performance with controllers capable of transferring 16 bits of
data at a time.

4.3
Control Registers

The Control registers are located at addresses 1 through 3. These registers
set up and configure the L64111 and monitor its operating status.

Control Register 1

Control Register 1 is an eight-bit register accessed through data bits
D[7:0].

Address A[4:0] = 00001₂

7	6	5	4	3	2	1	0
ANC DATA FIFO RST	SER/PAR	BYPASS	RESERVED	RESERVED	BUF_RST	SOFT_RST	STARTI

ANC DATA FIFO RST

Ancillary Data FIFO Reset   7

When this bit is set to one, the L64111 clears/empties the Ancil-
lary Data FIFO on the next clock cycle. The bit must then be set
back to zero to enable the FIFO. The default for this bit upon sys-
tem reset is zero (FIFO enabled).

SER/PAR   **Serial/Parallel Input Select**   6

When SER/PAR is one, the L64111 uses the SERI input as the
source of MPEG data. When this bit is zero, the L64111 selects
MPEG data from the Controller Interface data bus D[15:0] when
$A[4:0] = 00000_2$. The L64111 uses the OR of this bit and the
SSEL pin to select the Serial or Parallel mode. This means that
if the SSEL pin is high the device will always be in Serial input
mode. The L64111 uses the value of the logical OR of this bit
and the SSEL pin to determine if the mode is Parallel or Serial.
The default value of this bit is zero (parallel mode).

BYPASS   **Bypass Mode**   5

The BYPASS bit determines whether the L64111 operates in
MPEG mode (BYPASS = 0) or Bypass mode (BYPASS = 1).The
L64111 uses the logical OR of this bit and the BYPASS pin to
determine if the Bypass mode is selected. If the BYPASS pin is
high, the device will always be in Bypass mode. The default
value of this bit is zero (not bypassed).

RESERVED   **Reserved**   [4:3]

Set the RESERVED bits to zero to maintain compatibility with
future L64111 revisions.

BUF_RST   **Buffer Reset**   2

When this bit is set to one, the Channel Buffer is emptied on the
next clock cycle. The L64111 does not reset this bit to zero after
emptying the Channel Buffer. The default value for this bit upon
system reset is zero. Note that the L64111 empties the Channel
Buffer when RESET is asserted or SOFT_RST is set to one.

SOFT_RST   **Soft System Reset**   1

Setting this bit to one causes the L64111 to reset itself on the next
clock cycle. After resetting itself, the L64111 sets this bit to zero.
The default value for this bit upon system reset is zero. The value
used by the L64111 to determine reset is the logical OR of the
RESET pin and the SOFT_RESET bit.

STARTI **Decoder Start** **0**

When this bit is one, the decoder functional block starts on the next clock cycle. If the Channel Buffer is empty, the decoder does not start until the Channel Buffer has received data. If this bit and the STARTI input pin are both HIGH, the decoder is enabled, and starts to play. When this bit is zero, the decoder is reset on the next cycle. The default value for this bit upon system reset is the state of the STARTI pin.

Control Register 2 Control Register 2 is an eight-bit register accessed through Controller Interface data bits D[7:0]. It is used to set up and control various functions as described in following paragraphs.

Address $A[4:0] = 00010_2$

7	6	5	4	3	2	1	0
MUTE[1:0]		SOFT_MUTE	SEL_16/8_BIT	AUDIO ONLY	I2S	PCM MODE	

MUTE[1:0] **Mute Control** **[7:6]**

This field determines the decoder's response to errors. An error occurs if any of the following conditions are detected: CRC errors, grammar errors in input data, or assertion of the $\overline{ERROR}$ input pin. The Play Director uses these two bits as follows:

MUTE[1:0] *Description*

00	Errors are ignored
01	On error, PCM output is muted
10	On error, the error is concealed by replaying the last valid frame
11	Reserved. Do not use this value.

The default value for this field upon system reset is 00_2.

SOFT_MUTE **Software Controlled Mute** **5**

When this bit is set to one, the L64111 forces the PCM output to zero, which mutes the output. Hard mute operation is controlled by the logical OR of the SOFT_MUTE bit and the HDMUTE pin. The default value for this bit upon system reset is zero. When read, the value of SOFT_MUTE is the logical OR of the SOFT_MUTE bit and the HDMUTE pin.

SEL_16/8_BIT **Data Width Select**   **4**

When this bit is one, the L64111 accepts 16-bit wide data on D[15:0]. When this bit is zero, the L64111 accepts 8-bit wide data on D[7:0] and ignores data bits D[15:8]. The L64111 only uses the 16-bit format for MPEG data; all control registers are eight bits wide. The default value for this bit upon system reset is zero.

AUDIO ONLY **Audio Only**   **3**

When this bit is one, the L64111 assumes that the input data stream is an MPEG audio stream. When this bit is zero, the L64111 assumes that input data is an ISO System Stream requiring full system processing to retrieve MPEG audio frames. Upon system reset, the value of this bit is set to the value of address line A4, which allows mode selection for stand-alone operation.

I2S   **I2S Protocol**   **2**

When this bit is one, the L64111 produces an I2S compatible protocol on the PCM output by delaying the data bit one SCLK cycle with respect to LRCLK. When this bit is zero, the PCM output is in standard mode.

PCM MODE   **PCM Output Mode**   **[1:0]**

These bits modify the PCM output in accordance with the table shown below. In each of the three PCM modes, the data is bit serial MSB first with sign extended. See the subsection entitled "Setting the PCM Output Mode" in Chapter 6 for more information.

PCM MODE[1:0]	Description
00	32 fs
01	64 fs
10	48 fs
11	Reserved

Control Register 3 Control Register 3 is an eight-bit register accessed through Controller Interface data bits D[7:0] that selects an audio channel from the incoming data stream.

Address $A[4:0] = 00011_2$

7	6	5	4	3	2	1	0
AUDIO_STREAM_ID_IGNORE	RESERVED		AUDIO_STREAM_IDENTIFIER				
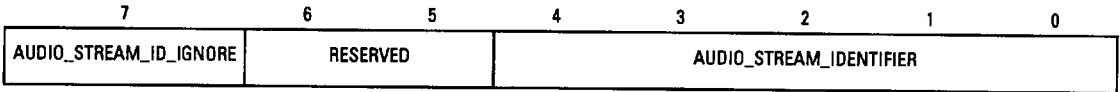
AUDIO_STREAM_ID_IGNORE

Ignore Audio Stream Identifier   7

When this bit is one, the L64111 responds to all audio streams and ignores the AUDIO_STREAM_IDENTIFIER value on bits [4:0]. When this bit is zero, the L64111 decodes only the audio streams with the audio ID value given in bits [4:0]. The default value of this bit upon system reset is one.

RESERVED   **Reserved**   [6:5]

Set these bits to zero to maintain compatibility with future revisions.

AUDIO_STREAM_IDENTIFIER

Audio Stream Identifier   [4:0]

The MPEG stream contains a packet start code with a five-bit audio stream identifier. A system controller may write to this register field to program the L64111 to respond only to the specified audio stream. Upon switching streams, resynchronization takes place automatically. The time taken depends on the nature of the bitstream and the number of times the L64111 finds an emulated sync code before finding an actual sync code. Once an actual sync code is found, the L64111 synchronizes within three frames. These bits are ignored if operating with an audio stream only.

4.4
Interrupt
Registers

Registers at addresses 4 and 5 provide monitoring and control of interrupts. The L64111 is capable of generating individually maskable interrupts in response to various internal events. An interrupt is enabled by writing a one to the location corresponding to a particular interrupt status bit. Writing a zero disables that interrupt. After a system reset, all interrupts are disabled.

When the system controller services an interrupt, it must read both registers because reading either of the registers deasserts the $\overline{\text{INTR}}$ output.

Interrupt Mask and Status Register 1

Interrupt Mask and Status Register 1 are eight-bit registers accessed through Controller Interface bits D[7:0]. They monitor the L64111's current status. A write to this location writes to Interrupt Mask 1. A read from this location reads Status Register 1. The Status Register 1 fields are defined following the registers.

Interrupt Mask 1 (Write Only)   Address $A[4:0] = 00100_2$

7	6	5	4	3	2	0
ANC DATA VALID	ANC DATA FIFO OVRFL	ANC DATA FIFO HFF	RESERVED	ERR BUF OVFL	RESERVED	

Status Register 1 (Read Only)   Address $A[4:0] = 00100_2$

7	6	5	4	3	2	0
ANC DATA VALID	ANC DATA FIFO OVRFL	ANC DATA FIFO HFF	0	ERR BUF OVFL	0	

ANC DATA VALID

Ancillary Data In FIFO is Valid   **7**

When set to one, this bit indicates that the Ancillary Data FIFO contains valid data. This bit does not cause an interrupt unless the Ancillary Data FIFO was previously empty. This bit continues to reflect the status of the Ancillary Data FIFO after Status Register 1 has been read and also after the FIFO has been read. A zero in this bit indicates that the Ancillary Data FIFO contains no data. Bit 7 in Interrupt Mask 1 masks this bit.

ANC DATA FIFO OVRFL

Ancillary Data In FIFO Overflowed   **6**

When set to one, this bit indicates that the Ancillary Data FIFO contains valid data and the FIFO is full, resulting in overflow.

This bit causes a single interrupt when the FIFO starts to overflow and does not interrupt again until the FIFO has been read from and starts to overflow again. This bit continues to reflect the status of the Ancillary Data FIFO after Status Register 1 has been read. Bit 6 in Interrupt Mask 1 masks this bit.

ANC DATA FIFO HFF

Ancillary Data FIFO Half Full Flag 5

When set to one, this bit indicates that the Ancillary Data FIFO is half full. Data may be lost if the FIFO is not read soon. This bit causes a single interrupt each time the FIFO passes over the half-full threshold in the high direction; another interrupt will not occur until the FIFO has been read, drops below, and then recrosses the half-full threshold. This bit continues to reflect the status of the Ancillary Data FIFO after Status Register 1 has been read. Bit 5 in Interrupt Mask 1 masks this bit.

RESERVED   Reserved   4, [2:0]

Set these bits to zero to maintain software compatibility with future revisions.

ERR BUFF OVFL

Channel Buffer Overflow Error 3

When set to one, this bit indicates that the Channel Buffer has overflowed and data is being lost. Channel Buffer overflow is an error that results in missing samples in the PCM output. The effect may or may not be audible. Bit 3 in Interrupt Mask 1 masks this bit.

Interrupt Mask and Status Register 2

Interrupt Mask and Status Register 2 are eight-bit registers accessed through Controller Interface data bits D[7:0]. They monitor the L64111's current status. A write to this location writes to Interrupt Mask 2. A read from this location reads Status Register 2.

Interrupt Mask 2 (Write Only)   Address $A[4:0] = 00101_2$

7	6	5	4	3	2	1	0
SYNTAX ERR DET	PTS AVAILABLE	SYNC AUD	SYNC SYS	FRAME DETECT IN	CRC ERR	NEW FRAME OUT	LAST FRAME

Status Register 2 (Read Only)   Address A[4:0] = 00101_2

7	6	5	4	3	2	1	0
0	SYNTAX ERR DET	PTS AVAILABLE	SYNC AUD	SYNC SYS	FRAME DETECT IN	CRC ERR	NEW FRAME OUT/LAST FRAME

The Status Register 2 fields are defined below. Each field has a corresponding mask in the Interrupt Mask 2 Register.

0   **0**   **7**

This bit reads as a zero.

SYNTAX ERR DET

Syntax Error Detected   **6**

When set to one, this bit indicates that the L64111 has detected a syntax error in either the ISO System Stream or in the audio stream. Bit 7 in Interrupt Mask 2 masks this bit.

PTS AVAILABLE

Presentation Time Stamp Available   **5**

When set to one, this bit indicates that the Presentation Time Stamp register contains a valid time stamp. The L64111 generates an interrupt only when this bit goes from zero to one. Bit 6 in Interrupt Mask 2 masks this bit.

SYNC AUD   **Synchronized Audio**   **4**

When set to one, this bit indicates that the L64111 is synchronized to the audio stream. The L64111 is considered synchronized after it has seen audio sync patterns in the correct location within three successive audio frames. The L64111 generates an interrupt when this bit goes from zero to one. Bit 5 in Interrupt Mask 2 masks this bit.

SYNC SYS   **Synchronized System**   **3**

When set to one, this bit indicates that the L64111 is synchronized to the system stream. The L64111 is considered synchronized after it has seen three consecutive system sync patterns in the correct location within the ISO System Stream. The L64111 generates an interrupt when this bit goes from zero to one. Bit 4 in Interrupt Mask 2 masks this bit.

FRAME DETECT IN

Frame Detect Input   **2**

When set to one, this bit indicates that a new frame is being processed. The parametric data word is valid and can be read for that frame. Bit 3 in Interrupt Mask 2 masks this bit.

CRC ERR   **CRC Error**   **1**

This bit is set to one when a CRC error has been detected. When an audio frame has a CRC error, the L64111 attaches its own internal flag to that frame's data and uses the flag to identify the frame as one having an error. Refer to the MUTE field description on page 4-6 for an example. Bit 2 in Interrupt Mask 2 masks this bit.

NEW FRAME OUT/LAST FRAME

         New Frame/Last Frame on Output   **0**

When set to one, this bit indicates that the L64111 has completed a frame and either the frame is being sent to the PCM output (New Frame Out) or there is only one frame in the channel buffer (Last Frame). The L64111 generates an interrupt when this bit goes from zero to one. Bit 1 in Interrupt Mask 2 masks the NEW FRAME OUT interrupt. Bit 0 in Interrupt Mask 2 masks the LAST FRAME interrupt.

4.5 **Timer Countdown** **and Offset** **Registers**	The following registers set the PCM Serial Output Clock (SCLKO) rate: ■ Timer Countdown Register (TCR) ■ Timer Offset Register High (TORH) ■ Timer Offset Register Low (TORL) The four-bit value in the TCR register is used as a terminal count. The 16-bit value formed from the TORH and TORL registers is used as the correction fraction, which is covered in more detail in Chapter 6.

Timer **Countdown** **Register (TCR)**	The TCR register provides the Terminal Count value, which determines the SCLKO clock rate. SCLKO makes one transition for every n transitions of SYSCLK. The value of n must be loaded into TCR[3:0]. Address $A[4:0] = 00110_2$

7	6	5	4	3			0
	RESERVED				TCR		
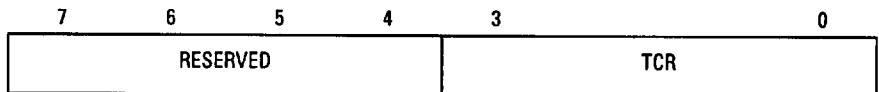
Timer Offset Register High (TORH)

The TORH register stores the eight most significant bits of the 16-bit word that contains the fractional part of the PCM timer. Note that the decimal point is located just prior to bit seven of the TORH register. TORH and TORL together provide the fractional portion of the PCM timer. The TCR register provides the integer portion of the SCLKO rate.

Address $A[4:0] = 00111_2$

DEC PT	7	6	5	4	3	2	1	0
.				TORH[15:8]				

Timer Offset Register Low (TORL)

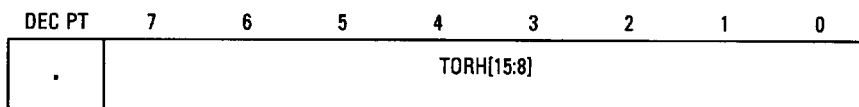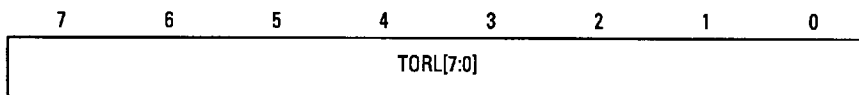The TORL register stores the least-significant fractional part of the PCM timer. TORL is accessed using Controller Interface bits D[7:0].

Address $A[4:0] = 01000_2$

7	6	5	4	3	2	1	0
			TORL[7:0]				

4.6 Parametric Data Word Registers

There are three eight-bit Parametric Data Word registers that contain the 20 header bits of the MPEG packet remaining after the 12-bit sync word 0xFFF has been stripped out. Each register can be read through Controller Interface data bits D[7:0]. The data in the Parametric Data Word registers is valid when the FRAME DETECT IN bit of Interrupt and Status Register 2 is set HIGH.

Note that the data must be read before the next frame overwrites it. The data remains valid for a minimum of seven milliseconds after the FRAME DETECT IN flag in Interrupt and Status Register 2 goes high. Reading the FRAME DETECT IN bit in the register again to determine if the data is still valid is not sufficient, since the FRAME DETECT IN bit goes HIGH only after the Parametric Data has been overwritten.

| Parametric Data Word Register 1 | The Parametric Data Register 1 contains the audio frame header data parsed from the stream. For complete details, consult ISO CD 11172-3. |

Address $A[4:0] = 01001_2$

7	6	5	4	3	0
ID	Layer [1:0]		protection_bit	bit_rate_index	

ID **Coding Type ID** 7
The ID bit indicates the ID of the algorithm. A one indicates MPEG; a zero indicates non-MPEG.

Layer [1:0] **Layer ID Number** [6:5]
The Layer field indicates the MPEG Layer used. The following table lists the encoding of the Layer field. The L64111 flags a syntax error if it sees Layer ID = 00 or 01.

Layer ID	Layer
11	Layer I
10	Layer II
01	Layer III
00	Reserved

protection_bit **Protection** 4
This bit indicates whether CRC has been added to the audio bit-stream. The L64111 can not detect CRC errors unless this bit is cleared to zero by the encoder.

bit_rate_index **Bit Rate Index** [3:0]
The bit_rate_index bit provides a pointer into a table indicating the bit rate. The table provides different values for a given pointer depending on the MPEG Layer. Illegal combinations of bit rate index, layer, and channel mode produce a syntax error on the L64111.

Index	Layer 1 Bit Rate	Layer 2 Bit Rate
0000	free format	free format
0001	32	32 †
0010	64	48 †
0011	96	56 †
0100	128	64
0101	160	80 †
0110	192	96
0111	224	112
1000	256	128
1001	288	160
1010	320	192
1011	352	224 ‡
1100	384	256 ‡
1101	416	320 ‡
1110	448	384 ‡
1111	reserved	reserved

1. † Mono (single channel) only.
2. ‡ Stereo, intensity stereo, dual channel only.

Parametric Data Word Register 2

Parametric Data Register 2 contains additional audio frame header data parsed from the stream. For additional details, consult ISO CD 11172-3.

Address $A[4:0] = 01010_2$

7	6	5	4	3	2	1	0
sampling_frequency [1:0]		padding_bit	extension_bit	mode [1:0]		mode_extension [1:0]	

sampling_frequency [1:0]

Sampling Frequency ID   [7:6]

This two-bit field indicates the sampling frequency as follows:

sampling_frequency	Frequency
00	44.1 KHz
01	48 KHz
10	32 KHz
11	Reserved

padding_bit   **Padding**   **5**
For MPEG stream decoder internal use.

extension_bit **Extension**   **4**
The value in this field is not used.

mode [1:0]   **Channel Mode**   **[3:2]**
Indicates the channel mode as follows:

Mode	Channel Mode Used
00	Stereo
01	Joint stereo (intensity stereo and/or ms stereo)
10	Dual channel
11	Single channel

mode_extension [1:0]
Mode Extension   **[1:0]**
This field is used in joint stereo mode. In Layer I and II this field indicates which subbands are in intensity stereo. All other sub-bands are coded in stereo.

Mode_Extension	Subbands
00	4-31 in intensity stereo
01	8-31 in intensity stereo
10	12-31 in intensity stereo
11	16-31 in intensity stereo

Parametric Data Word Register 3

Parametric Data Register 3 contains additional audio frame header data parsed from the stream. For more details, consult ISO CD 11172-3.

Address $A[4:0] = 01011_2$

7	6	5	4	3			0
copyright	original/home	emphasis [1:0]		Reserved			

copyright   **Copyright Flag**   **7**
A one in this bit indicates that the data is copyrighted. A zero indicates that the coded bitstream is not copyright protected.

original/home **Originator Copy**   **6**
A one in this bit indicates that the bitstream contains original data. A zero indicates that the bitstream is a copy.

emphasis	**Emphasis**								**[5:4]**

This field indicates the type of de-emphasis to be used:

Emphasis	Type of De-emphasis to Use
00	No emphasis
01	50/15 microsecond emphasis
10	Reserved
11	CCITT J.17

Reserved [3:0]

Reserved for future use.

4.7 Presentation Time Stamp (PTS) Registers

These five eight-bit registers contain the current Presentation Time Stamp. Each register may be read through Controller Interface data bits D[7:0]. This data is valid when the PTS AVAILABLE field, is set HIGH. It is over-written when the next presentation time stamp is parsed. The data stored here is as specified in Section 2.4.3 of the MPEG Systems CD 11172-1. This data is only valid if the L64111 is decoding a system stream, and is synchronized to that stream.

Address A[4:0]	Register #	7	6	5	4	3	2	1	0
01100_2	PTS1	pts[7:0]							
01101_2	PTS2	pts[15:8]							
01110_2	PTS3	pts[23:16]							
01111_2	PTS4	pts[31:24]							
10000_2	PTS5	0							pts32

4.8 Ancillary/User Data FIFO

This eight-bit register represents the top of a 16 by 8 bit FIFO that contains any Ancillary/User data from the current stream. Successive reads from this register will read the next byte in the FIFO.

The FIFO is filled in MSB order, that is, the first bit in the stream becomes bit 7 on the top of the FIFO, the second bit in the stream becomes bit 6 in the top of the FIFO, and so on. The ninth bit in the stream becomes bit 7 in

the second location in the FIFO, and so on. Ancillary data for the next frame is appended to that from the previous frame.

The FIFO is accessed through Controller Interface bits D[7:0]. The FIFO contains valid data as long as the ANC DATA VALID bit is HIGH.

Address $A[4:0] = 10001_2$

7	6	5	4	3	2	1	0
FIFO TOP BIT 7	FIFO TOP BIT 6	FIFO TOP BIT 5	FIFO TOP BIT 4	FIFO TOP BIT 3	FIFO TOP BIT 2	FIFO TOP BIT 1	FIFO TOP BIT 0

4.9 Channel Buffer Registers

The L64111 contains three registers that control the Channel Buffer. These registers are the Channel Buffer Status Counter, the Channel Buffer Write Counter, and the Channel Buffer Read Counter.

Channel Buffer Status Counter

The Channel Buffer Status Counter is a read-only register, which contains a seven-bit value that indicates the current storage capacity of the Channel Buffer. The Channel Buffer Status Counter is a counter ranging from 0 to 127 in Layer 1, and 0 to 63 in Layer 2. Each layer 2 frame occupies twice as much space as a layer 1 frame, but plays for twice as long.

This register may be read to determine whether the Channel Buffer is filling up too fast or slow with respect to the output rate.

The Channel Buffer Status Counter may be read on Controller Interface bits D[6:0].

Address $A[4:0] = 10010_2$

7	6	5	4	3	2	1	0
Reserved	CB_Status_Counter [6:0]						

Channel Buffer Write Counter

The Channel Buffer Write Counter is a double-buffered read/write register, which contains a seven-bit value used as a pointer to the location in the Channel Buffer of the current frame to be written. The pointer may be in the range zero to 127 (0 to 63 for Layer 2). The buffer is maintained as a circular buffer, thus location 0 is immediately after 127.

A write to this register sets the location of the next Channel Buffer write operation and determines where the next byte of data will be written in the Channel Buffer. This feature may be used in implementing cue and review. Once the register is written it will automatically increment as required. However, the Channel Buffer Status register will not necessarily reflect the true channel status, and the channel full/empty interrupts will not work. If cue and review is not required do not write to this register.

Address A[4:0] = 11010_2

| 7	6	5	4	3	2	1	0
Reserved	CB_Write_Counter [6:0]						
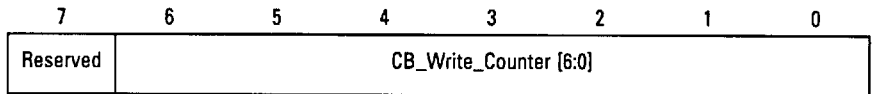
Channel Buffer Read Counter

The Channel Buffer Read Counter is a double-buffered read/write register, which contains a seven-bit value used as a pointer to the next audio frame to be read out of the Channel Buffer. The pointer may be in the range 0 to 127 (0 to 63 for Layer 2).

A write to this register sets the location of the next Channel Buffer read operation and determines where the following read in the Channel Buffer will be made. If the write falls after the clock set up then the new value is used only after the next clock cycle.

This feature is useful for cue and review; the user may control what sample should be read next and what samples should be skipped. The user can "skip" around in the frame. Note that while the frames may be played in reverse order for review, the samples themselves will be played in the forward direction. Once the register is written it automatically increments as required. However, the Channel Buffer Status register will not necessarily reflect the true channel status, and the channel full/empty interrupts will not work. If cue and review is not required do not write to this register.

Address A[4:0] = 11001_2

7	6	5	4	3	2	1	0
Reserved	CB_Read_Counter [6:0]						
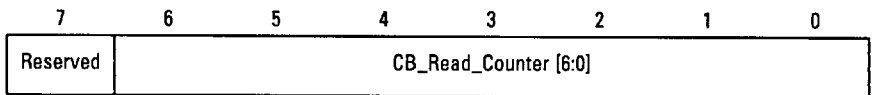
Chapter 5
Specifications

Chapter 5 presents specifications for the L64111 MPEG Audio Decoder. This chapter contains the following sections:

- Section 5.1, Electrical Characteristics
- Section 5.2, AC Timing
- Section 5.3, Pinouts
- Section 5.4, Mechanical Specifications
- Section 5.5, Ordering Information

5.1
Electrical
Characteristics

This section specifies the electrical requirements for the L64111. Electrical data is presented in the following categories:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Capacitance
- DC Characteristics
- Pin Description Summary

Table 5.1
Absolute Maximum
Ratings

Symbol	Parameter	Limits	Units
VDD	DC supply voltage	-0.3 to +7	V
VIN	Input voltage	-0.3 to VDD + 0.3	V
IIN	DC input current	10	mA
TSTGC	Storage temperature, ceramic	-65 to +150	°C
TSTGP	Storage temperature, plastic	-40 to +125	°C

Table 5.2
Recommended
Operating
Conditions

Symbol	Parameter	Limits	Units
VDD	DC supply voltage	+4.75 to +5.25	V
TA	Ambient temperature, commercial	0 to +70	°C

Table 5.3
Capacitance

Symbol	Parameter[1]	Min	Typ	Max	Units
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			10	pF
C_{IO}	I/O Bus Capacitance			15	pF

1. Measurement conditions are $V_{IN} = 5.0$ V, $T_A = 25°C$, and clock frequency = 1 MHz.

Table 5.4 DC Characteristics	Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
	VIL	Low TTL Input Voltage		-	-	0.8	V
	VIH	High Input Voltage: Commercial		2.0	-	-	V
	VT	Switching Threshold		-	1.5	-	V
	IIN	Input Current: CMOS TTL	VIN = VDD or VSS	-10	0	10	μA
		Pullup	VIN = VSS	-60	-105	-190	μA
		Pulldown	VIN = VDD	55	120	200	μA
	VOL	Low Output Voltage		-	0.2	0.4	V
	VOH	High Output Voltage		2.4	4.5	-	V
	IOS	Output Short-circuit Current:[2]					
		High Output Voltage	VO = VDD	30	70	120	mA
		Low Output Voltage	VO = VSS	-30	-60	-120	mA
	IDDQ	Quiescent Supply Current	VIN = VDD or VSS			10	mA
	IDD	Operating Supply Current	SYSCLK @ 30 MHz		300		mA

1. All DC characteristics are specified for VDD = 5V ± 5% over the specified temperature and voltage ranges.
2. Only one output should be shorted at a time. Duration of short circuit test must not exceed one second. Specified for Maximum VDD.

Table 5.5
Pin Description Summary

Mnemonic	Description	Input/Output	Drive (mA)	Active
A[4:0]	Address Bus	Input w/Pullup		
$\overline{\text{AS}}$	Address Strobe	Input w/Pullup		Low
BA[8:0]	Buffer Address	Output w/Moderate Slew Rate	4	
BD[3:0]	Buffer Data	3-state Bidirectional w/Pullup	4	
BYPASS	Decoder Bypass	Input w/Pullup		
$\overline{\text{CAS}}$	Column Address Strobe	Output w/Moderate Slew Rate	4	Low
$\overline{\text{CSLDS}}$	Chip Select and Lower Data Strobe	Input w/Pullup		Low
$\overline{\text{CSUDS}}$	Chip Select and Upper Data Strobe	Input w/Pullup		Low
D[15:0]	Data Bus	3-state Bidirectional w/Pullup	4	
DACLK	DAC Output Clock	Output	4	
$\overline{\text{DTACK}}$	Data Acknowledge	Output	4	Low
$\overline{\text{ERROR}}$	Error Indication	Input w/Pullup		Low
$\overline{\text{FALE}}$	FIFO Almost Empty Flag	Output	4	Low
$\overline{\text{FALF}}$	FIFO Almost Full Flag	Output	4	Low
$\overline{\text{FEMPTY}}$	FIFO Empty Flag	Output	4	Low
HDMUTE	Hard Mute	Input w/Pullup		High
INT/MOT	Selects Controller Interface Mode	Input w/Pulldown		
$\overline{\text{INTR}}$	System Interrupt/Error	Open-Drain Output	4	Low
LRCLKI/ DVALID	Left/Right Channel Indicator In/ Data Valid	Input w/Pullup		
LRCLKO	Left/Right Channel Indicator Out	Output	4	
$\overline{\text{RAS}}$	Row Address Strobe	Output w/Moderate Slew Rate	4	Low
READ	Read	Input w/Pullup		
RESET	Reset	Input w/Pullup		High
SCLKI	Serial Clock In	Input w/Pullup		
SCLKO	Serial Clock Out	Output	4	
SERI	Serial Data In	Input w/Pullup		
SERO	Serial Data Out	Output	4	
SSEL	Serial Select	Input w/Pullup		
STARTI	Start In	Input w/Pullup		
STARTO	Start Out	Output	4	
SYSCLK	System Clock	Input w/Pullup		
WCLKI	Word Clock In	Input w/Pullup		
WCLKO	Word Clock Out	Output	4	
$\overline{\text{WE}}$	Write Enable	Output w/Moderate Slew Rate	4	Low

5.2
AC Timing

This section presents AC timing information for the L64111. Table 5.6 lists the AC timing parameters for the timing waveforms shown in Figures 5.1 through 5.6. Note that the minimum clock cycle time is 33.33 ns. The maximum clock cycle time is $1/(384f_s)$ ns, where f_s is the sampling frequency (32 KHz, 44.1 KHz, or 48 KHz).

All parameters in the timing tables apply for TA = 0 °C to 70 °C, VDD = 4.75 to 5.25 volts.

Table 5.6
AC Characteristics

	Parameter	Description	Min	Max	Units
1	t_{DRASL}	Clock to $\overline{RAS}$ Low		22	ns
2	t_{DRADD}	Clock to Row Address		20	ns
3	t_{DCADD}	Clock to Column Address		20	ns
4	t_{DHD}	Write Data Hold	35		ns
5	t_D	Clock to Data		21	ns
6	t_{DCASH}	Clock to $\overline{CAS}$ High		22	ns
7	t_{SUD}	Write Data Setup before $\overline{CAS}$ Low	12		ns
8	t_{DRASH}	Clock to $\overline{RAS}$ High		17	ns
9	t_{DWE}	Clock to $\overline{WE}$ High		21	ns
10	t_{DCASL}	Clock to $\overline{CAS}$ Low		22	ns
11	$t_{SUBDCASH}$	BD Setup before SYSCLK High	2		ns
12	t_{SURCS}	READ Setup before $\overline{CSXDS}$ Low	4		ns
13	t_{SUA}	A[4:0] Setup before $\overline{AS}$ Low	8		ns
14	t_{HLDA}	A[4:0] Hold after $\overline{AS}$ Low	0		ns
15	t_{DCSDTL}	$\overline{CSXDS}$ Low to $\overline{DTACK}$ Low		$t_{CLK}+12$	ns
16	t_{HLDD}	Write Data Hold after $\overline{CSXDS}$ High or Low	0		ns
17	t_{CYCLE}	Minimum $\overline{CSXDS}$ Width	$2t_{CLK}$		ns
18	t_{SUD}	Write Data Setup before $\overline{CSXDS}$ Low	8		ns
19	t_{HLDD}	READ Hold after $\overline{CSXDS}$ High (Write)	0		ns
20	t_{HLDRCS}	READ Hold after $\overline{CSXDS}$ High (Read)	0		ns
21	t_{WRREC}	Write Recovery time	$2t_{CLK}$		ns
22	t_{DCSDTH}	$\overline{CSXDS}$ High to $\overline{DTACK}$ High		$t_{CLK}+8$	ns
23	t_{DELZL}	$\overline{CSXDS}$ Low to Data Driven	5	20	ns
24	t_{DELD}	$\overline{CSXDS}$ Low to Data Valid		$t_{CLK}+20$	ns
25	t_{DELLZ}	$\overline{CSXDS}$ High to Data 3-state	5	20	ns
26	t_{SUD}	Write Data Setup before $\overline{CSXDS}$ High	8		ns
27	t_{SULR}	LRCLKI Setup before SCLKI High	12		ns
28	t_{SUSERI}	SERI Setup before SCLKI High	12		ns

(Sheet 1 of 2)

Table 5.6 (Cont.)
AC Characteristics

	Parameter	Description	Min	Max	Units
29	$t_{HLDSERI}$	SERI Hold after SCLKI High	0		ns
30	t_{HLDLR}	LRCLKI Hold after SCLKI High	0		ns
31	$t_{DLYBYPASS}$	Delay from Input in BYPASS Mode		18	ns
32	t_{HLDW}	$\overline{AS}$ Hold after $\overline{CSXDS}$ Low	$2*t_{CLK}$		ns
33	t_{SUPCM}	SERO to SCLKO High	$5*t_{CLK}$		ns
34	t_{HLDPCM}	SCLKO High to SERO Change	$5*t_{CLK}$		ns
35	$t_{DLYPCMCTL}$	LRCLKO Change to SCLKO High	$5*t_{CLK}$		ns
36	t_{SUREAD}	READ Setup before $\overline{AS}$ Low	20		

(Sheet 2 of 2)

Figure 5.1
Channel Buffer
Write Cycle
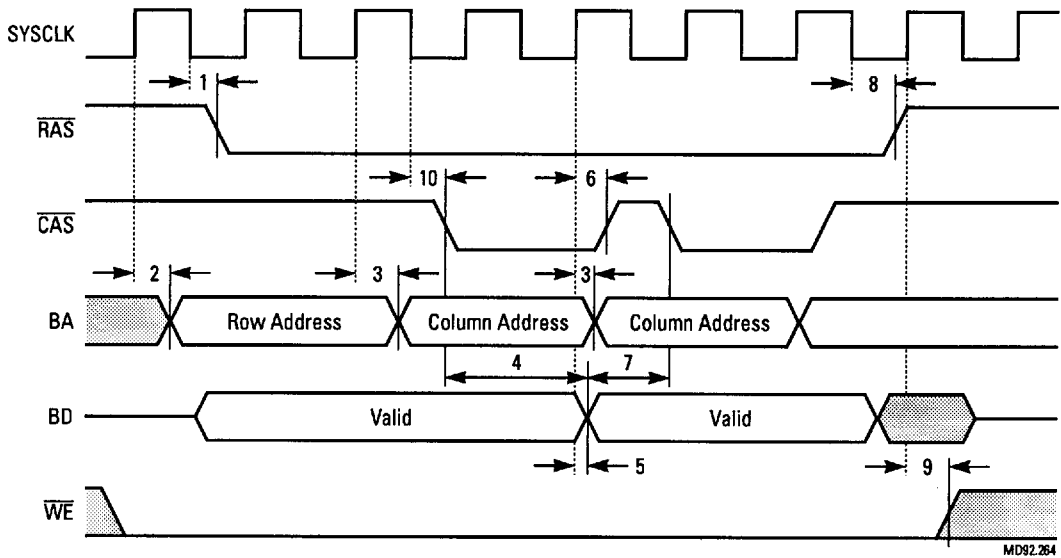
MD92.264

Figure 5.2
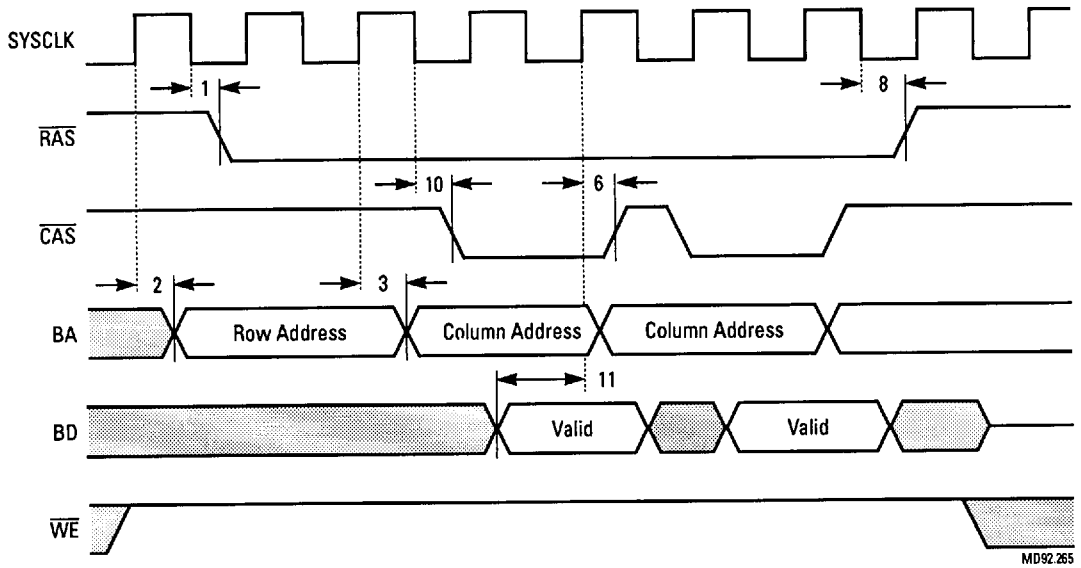Channel Buffer Read
Cycle

MD92.265

Figure 5.3
Controller Interface
Write Cycle

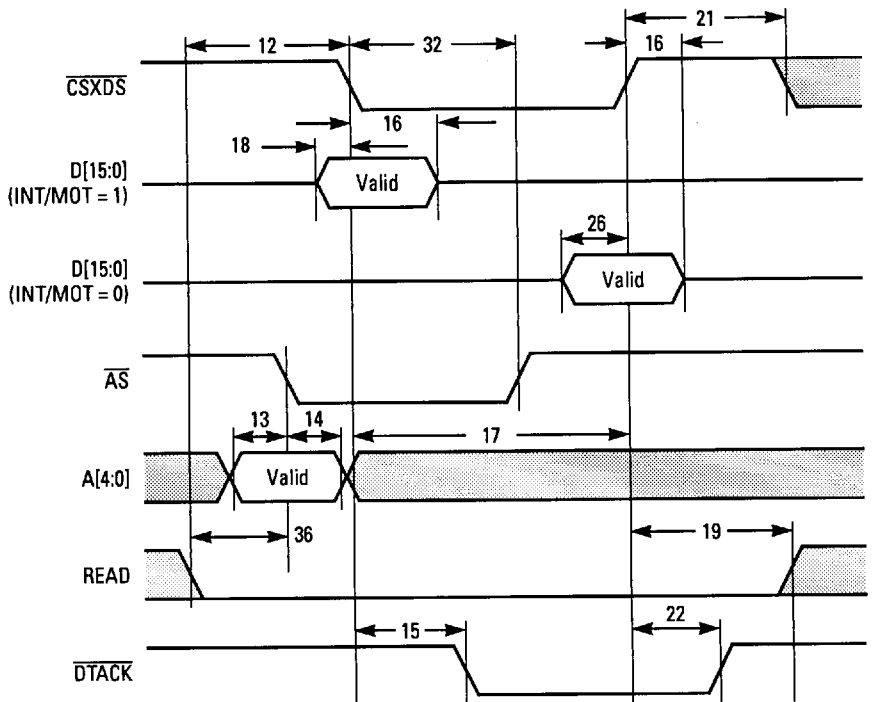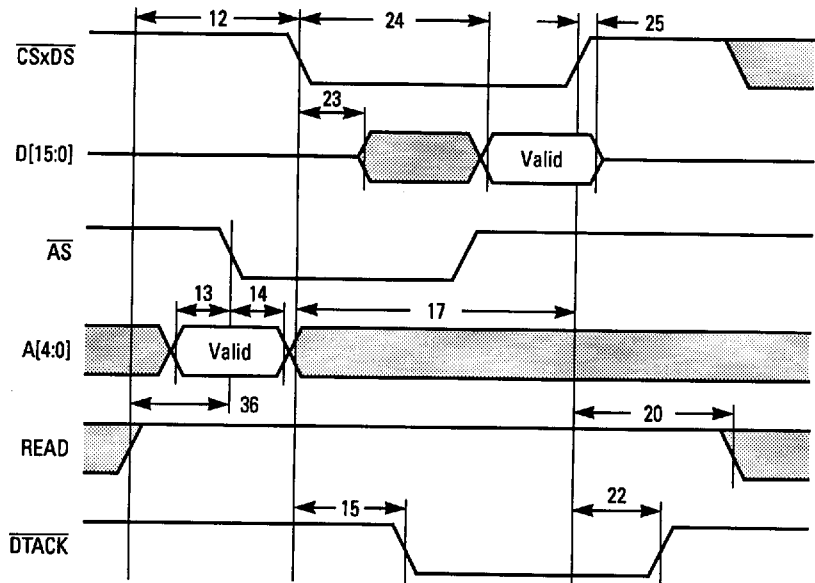Figure 5.4
Controller Interface
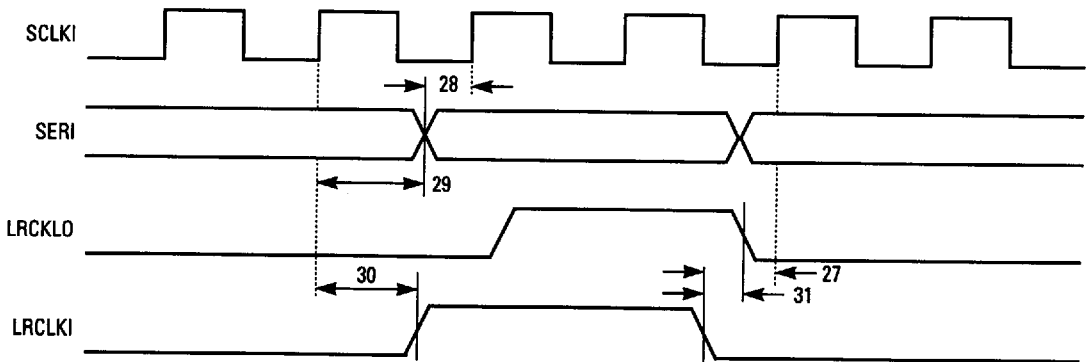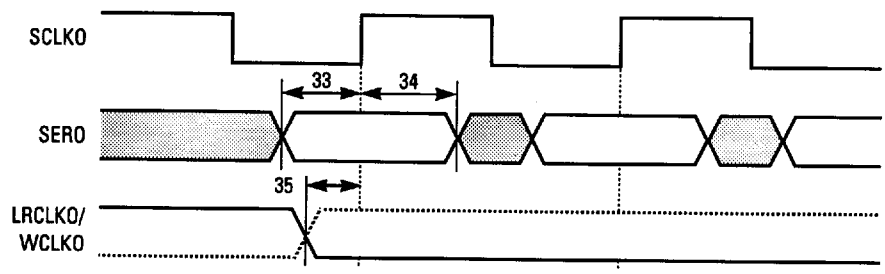Read Cycle

Figure 5.5
Input Timing

Figure 5.6
Serial PCM Data Out
Timing

5.3
Pinouts

This section provides pinout tables for the L64111 package. The L64111 is available in a 100-pin plastic quad flat package (PQFP).

Table 5.7
100-pin PQFP
Pinout by Pin
Number

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	A2	26	VDD	51	SERO	76	*NC*[1]
2	VDD	27	*NC*	52	VDD	77	VDD
3	VDD	28	VDD	53	VDD	78	VDD
4	VDD	29	VDD	54	VDD	79	VDD
5	INT/MOT	30	D7	55	$\overline{\text{FEMPTY}}$	80	BA8
6	A1	31	D6	56	VSS	81	BA7
7	A0	32	D5	57	$\overline{\text{FALF}}$	82	BA6
8	$\overline{\text{AS}}$	33	D4	58	$\overline{\text{FALE}}$	83	BA5
9	SSEL	34	D3	59	VSS	84	BA4
10	DACLK	35	VSS	60	RESET	85	BA3
11	READ	36	D2	61	HDMUTE	86	BA2
12	$\overline{\text{CSUDS}}$	37	D1	62	VDD	87	BA1
13	$\overline{\text{CSLDS}}$	38	D0	63	VDD	88	BA0
14	VDD	39	$\overline{\text{INTR}}$	64	SYSCLK	89	VDD
15	VSS	40	VSS	65	VSS	90	VSS
16	*NC*	41	VDD	66	VSS	91	VDD
17	D15	42	$\overline{\text{DTACK}}$	67	VDD	92	$\overline{\text{CAS}}$
18	D14	43	*NC*	68	$\overline{\text{ERROR}}$	93	$\overline{\text{RAS}}$
19	D13	44	VDD	69	WCLKI	94	$\overline{\text{WE}}$
20	D12	45	VDD	70	LRCLKI	95	BD3
21	D11	46	STARTO	71	SCLKI	96	BD2
22	D10	47	STARTI	72	SERI	97	BD1
23	D9	48	WCLKO	73	BYPASS	98	BD0
24	VSS	49	LRCLKO	74	VDD	99	A4
25	D8	50	SCLKO	75	VSS	100	A3

1. NC pins are not connected and are reserved.

Table 5.8
100-pin PQFP
Pinout by Pin Name

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
A0	7	D2	36	$\overline{RAS}$	93	VDD	53
A1	6	D3	34	READ	11	VDD	54
A2	1	D4	33	RESET	60	VDD	62
A3	100	D5	32	SCLKI	71	VDD	63
A4	99	D6	31	SCLKO	50	VDD	67
$\overline{AS}$	8	D7	30	SERI	72	VDD	74
BA0	88	D8	25	SERO	51	VDD	77
BA1	87	D9	23	SSEL	9	VDD	78
BA2	86	D10	22	STARTI	47	VDD	79
BA3	85	D11	21	STARTO	46	VDD	89
BA4	84	D12	20	SYSCLK	64	VDD	91
BA5	83	D13	19	WCLKI	69	VSS	15
BA6	82	D14	18	WCLKO	48	VSS	24
BA7	81	D15	17	$\overline{WE}$	94	VSS	35
BA8	80	DACLK	10	VDD	2	VSS	40
BD0	98	$\overline{DTACK}$	42	VDD	3	VSS	56
BD1	97	$\overline{ERROR}$	68	VDD	4	VSS	59
BD2	96	$\overline{FALE}$	58	VDD	14	VSS	65
BD3	95	$\overline{FALF}$	57	VDD	26	VSS	66
BYPASS	73	$\overline{FEMPTY}$	55	VDD	28	VSS	75
$\overline{CAS}$	92	HDMUTE	61	VDD	29	VSS	90
$\overline{CSLDS}$	13	INT/MOT	5	VDD	41	NC[1]	16
$\overline{CSUDS}$	12	$\overline{INTR}$	39	VDD	44	NC	27
D0	38	LRCLKI	70	VDD	45	NC	43
D1	37	LRCLKO	49	VDD	52	NC	76

1. NC pins are not connected and are reserved.

5.4 Mechanical Specifications

Figure 5.7 shows the mechanical dimensions for the L64111 100-pin PQFP package.

Figure 5.7
100-pin PQFP
Mechanical
Dimensions

Top View

Side View

No. of Pins = 30

No. of Pins = 20

Mark
Index

Detail Y

Detail W

Detail X

(Note 4)
– H –

(Note 7)

(Note 3)

(Note 3)

e (Note 4)
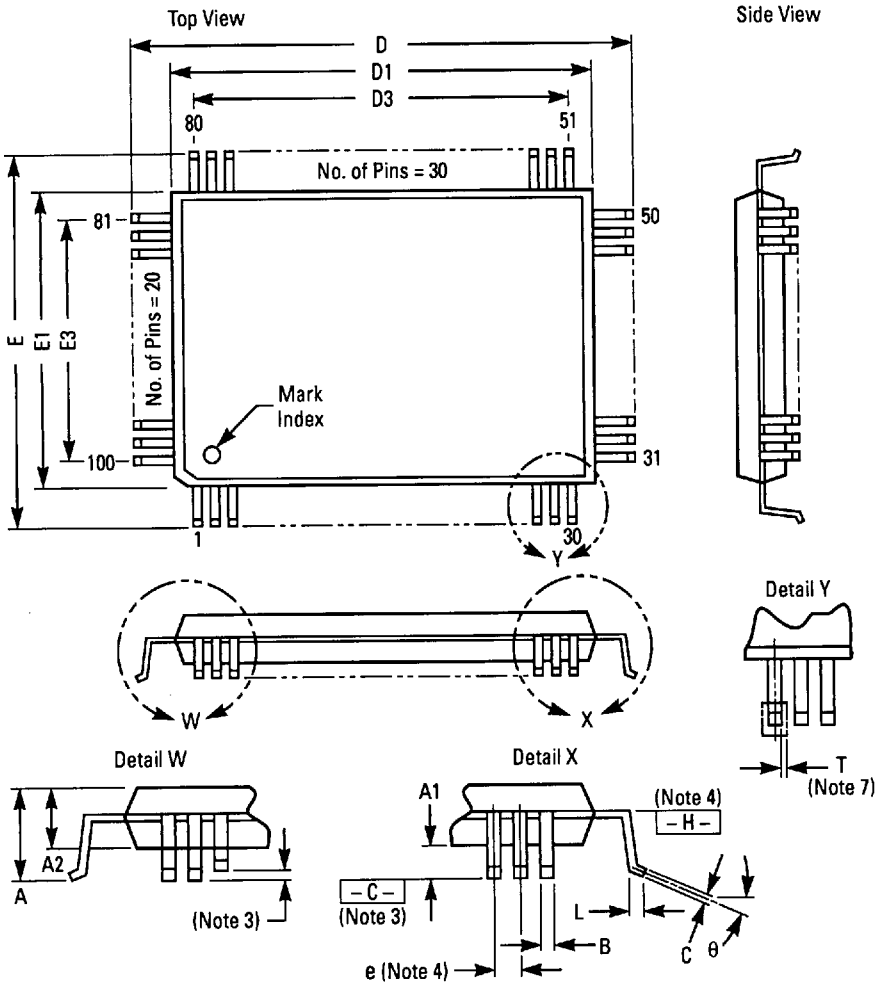
Dimension		mm
A	Max	3.40
A1	Min	0.25
	Max	0.35
A2	Min	2.55
	Nom	2.80
	Max	3.05
B	Min	0.22
	Nom	0.30
	Max	0.38
C	Min	0.12
	Max	0.25
D	Min	23.65
	Nom	23.90
	Max	24.15
D1	Min	19.90
	Nom	20.00
	Max	20.10
D3	Ref	18.85
e	BSC	0.65
E	Min	17.65
	Nom	17.90
	Max	18.15
E1	Min	13.90
	Nom	14.00
	Max	14.10
E3	Ref	12.35
L	Min	0.65
	Nom	0.80
	Max	0.95
T	Max	0.10
θ	Min	0°
	Max	7°

Note:
1. Total number of pins is 100.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. Dimensions D3 and E3 to be centered relative to dimensions D1 and E1, respectively, ±0.200 mm.
7. Tolerance window for lead skew from true position is determined at seating plane – C –.
8. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code PB.

MD92.PB

5.5
Ordering
Information

This section presents ordering information for the L64111 MPEG Audio Decoder. The part number uses the following format:

L64111 Q C

Temperature Range/ Flow Option
C = Commercial (0 °C to 70 °C)

Package Code
Q = 100-pin PQFP

Device Type
MPEG Audio Decoder
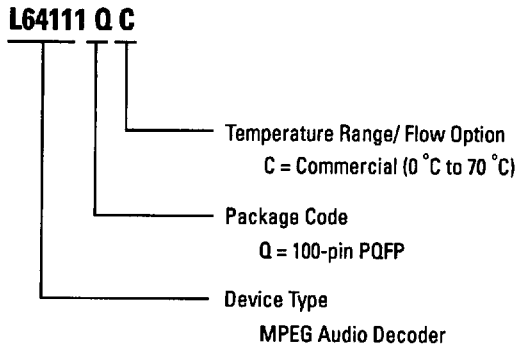
Chapter 6
Applications

This chapter discusses L64111 applications and design requirements. It covers use of the L64111 in stand-alone applications (without an external controller) and in applications where a separate controller is used. The L64111 can also support applications requiring video synchronization or cue and review functions, which require an external controller.

This chapter contains the following sections:

■ Section 6.1, External Controller Operation

■ Section 6.2, Stand-alone Operation

■ Section 6.3, DAC Interfacing

■ Section 6.4, Audio/Video Application

6.1 External Controller Operation

Applications requiring a system controller may use an 8- or 16-bit controller or a dedicated state machine. The L64111 Audio Decoder can accept input data in 8- or 16-bit parallel format through the Controller Interface data I/O pins. To ensure compatibility with eight-bit controllers, all control registers are eight bits wide and are always accessed through D[7:0]. The L64111 can be used with either 8- or 16-bit controllers but provides a higher data throughput with a 16-bit controller.

Figure 6.1 is an example of the L64111 with a 16-bit controller. An external controller is required for all operations which need non-default initialization of registers, reading of registers (for example the buffer status or the PTS), and interrupt handling.
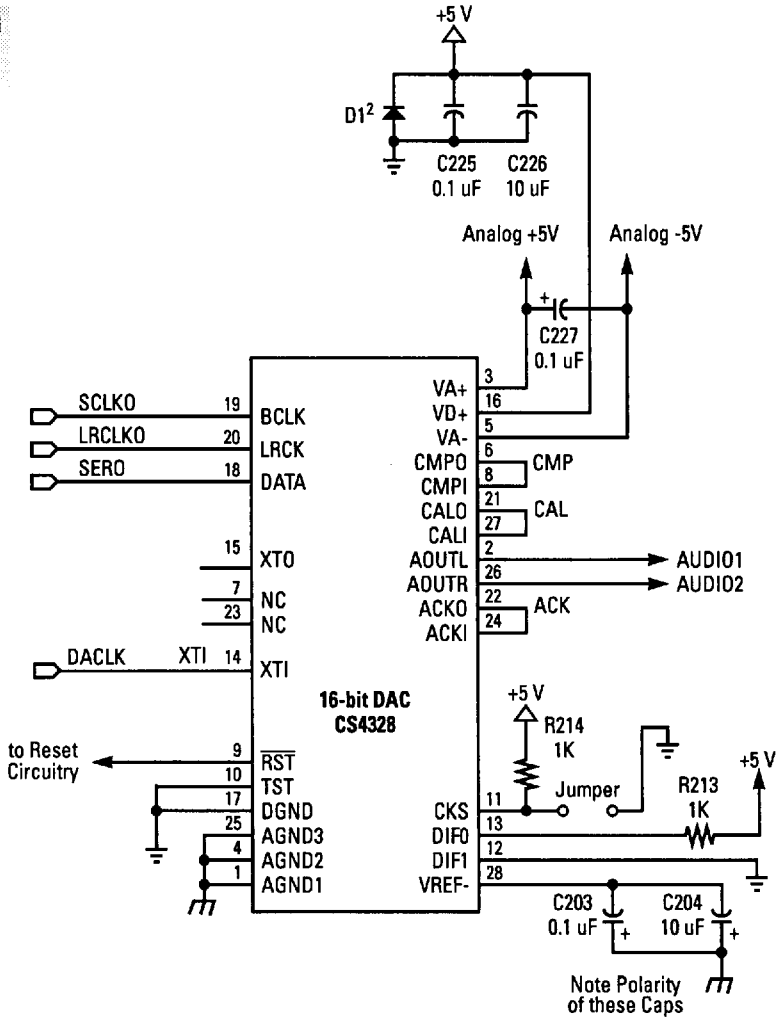
Figure 6.1
Application Using
External Controller
(Sheet 1 of 2)
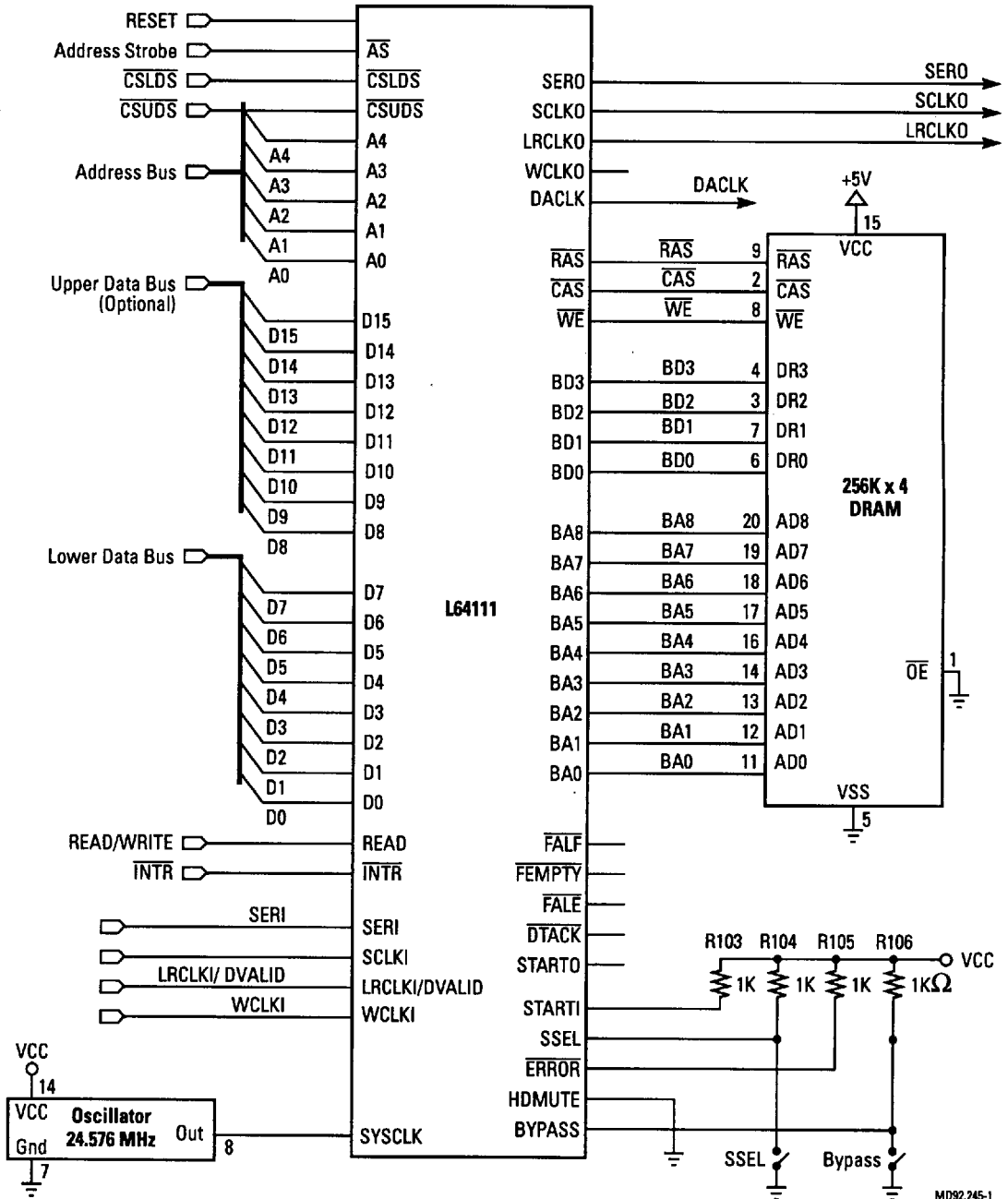
Figure 6.1
Application Using
External Controller
(Sheet 2 of 2)

r/t = Analog Ground

= Digital Ground

6.2
Stand-alone
Operation

The L64111 is designed to support stand-alone operation. This section discusses the system architecture and the chip features that support this application. Figure 6.2 illustrates the design of a prototypical stand-alone decoder application. The main components are:

- L64111 MPEG Audio Decoder
- DRAM Channel Buffer
- PCM Digital to Analog Converter (DAC)

Not shown are auxiliary circuit components such as an oscillator, power supply, or passive components. The following sections discuss aspects of using this design.

Figure 6.2
Stand-alone
Operation
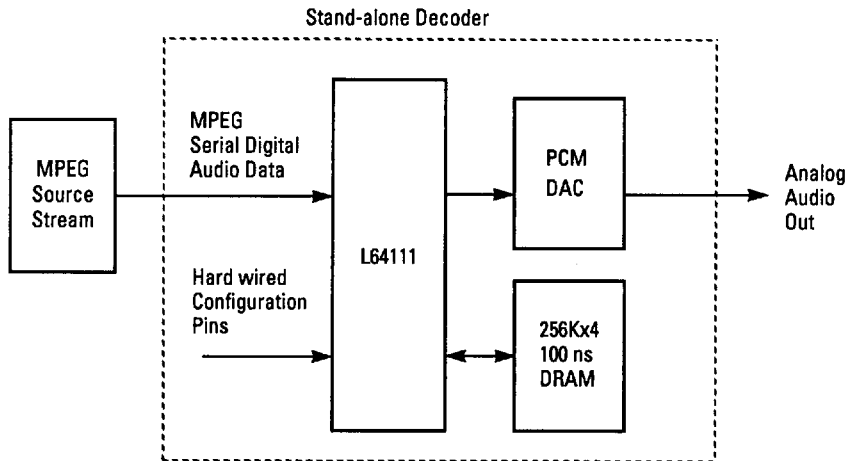
In stand-alone operation, the L64111's configuration and operating parameters may be selected via hard wired input pins or by utilizing the default values in its registers. The following discusses specific items.

Stream Type Selection

In stand-alone applications, address line A4 may be hard wired to select whether L64111 functions as an ISO System Stream decoder or as an audio stream decoder. When A4 is high, the L64111 operates with audio streams only. When A4 is low, the L64111 operates with system streams only. For more information, see the description of the AUDIO ONLY field of Control Register 2 on page 4-7 and also Table 6.2 below. One of the two forms of decoding must be chosen.

Setting Output Frequency

Registers TCR, TORH, and TORL must be loaded with a value that determines the output bit rate. A divisor is entered that is applied to the system clock. To enable these values to be set on the rising edge of RESET, the address lines and the data lines write directly into the TOR and TCR registers as shown in Table 6.1.

Table 6.1
Hardwiring Values
Using Input Pins

Input Pins	Name of Register Being Written to	Register Field/Bits
A4	Control Register 2	AUDIO ONLY, bit 3; 0 = decode at system stream layer 1 = decode audio stream only
A[3:0]	TCR	TCR[3:0]
D[15:8]	TORH	TOR[15:8]
D[7:0]	TORL	TOR[7:0]

When the A and D lines in Table 6.1 are hardwired to the appropriate levels, the L64111 stores the configuration values when the RESET pin is asserted. Once these values are latched, the L64111 can function using its serial port for the data stream and it ignores the pins listed in Table 6.1. Note that if other register bits need to be changed from their default values stand-alone mode cannot be used.

6.3
DAC Interfacing

This section discusses the DAC to interface to the L64111. The L64111 is designed to interface to a wide, variety of bit-serial DACs that are commonly used in consumer products such as audio CD and DAT players.

There are two basic families of audio DAC: baseband and oversampling DACs. Baseband DACs operate at the audio sample rate, typically 44.1 KHz. They vary in the conversion technique employed, but from the perspective of the L64111 are distinguished by the fact that the highest speed clock provided to them is the bit clock, SCLKO. Baseband DACs generally require a sophisticated analog filter on their output to remove images of the reconstructed signal at multiples of the sample frequency.

Oversampling DACs can simplify the implementation of the analog post filter by interpolating the signal digitally prior to conversion, and performing the conversion at a higher rate. This rate is typically eight times the sampling frequency, f_s (hence the term 8x oversampling), which causes the images of the reconstructed signal to appear centered about multiples of 8 f_s instead of f_s. The images can now be easily removed with a simple ana-

log filter. From the perspective of the L64111, oversampling DACs are distinguished by the fact that they generally require a very accurate clock, which is typically 256 to 384 times the sample clock rate, in addition to the SCLKO signal.

The L64111 is able to synthesize a SCLKO signal over a wide frequency range by using an internal fractional counter, which allows the L64111 to provide different SCLKO clock rates from the same SYSCLK. In this manner, different output sample rates are supported from a single oscillator. Variable sample rates are very useful in a system that may transmit coded MPEG data at 32 KHz, 44.1 KHz, or 48 KHz. A fractional divider cannot be used with most oversampling DACs because there is usually a strict relationship between the SCLK frequency and the DAC operating frequency, which may not be met with a fractional divider. It is therefore recommended to use only an integer divisor to generate the SCLKO frequency when using oversampling DACs.

Table 6.2 shows recommended operating frequencies for the L64111 when used with oversampling DACs at different sampling rates. Note that a single clock can be used for 32 KHz and 48 KHz operation if the DAC can switch between 256 f_s and 384 f_s operation (which is fairly common).

Table 6.2 Recommended Operating Frequencies Using Oversampling DACs

Sample Rate	256 f_s Mode DACs		384 f_s Mode DACs	
	Clock Frequency	TCR reg	Clock Frequency	TCR reg.
32 KHz	16.384 MHz	8	24.576 MHz	8
44.1 KHz	22.5792 MHz	8	16.9344 MHz	6
48 KHz	24.576 MHz	8	18.432 MHz	6

Another consideration must be made when selecting a DAC. In some systems there is no feedback possible between the encoder and the decoder regarding possible mismatch between the encoder clock and the decoder clock. This lack of feedback is true of most broadcast or narrow cast applications, or any application in which the L64111 is operating in stand-alone mode. The basic problem is that any clock mismatch accumulates over time, and ultimately results in the overflow or underflow of the channel buffer at the decoder. The clocks must be locked together to prevent this if a reliable system is to be built.

Lock can be achieved either by phase or frequency lock to the channel clock, or by using timestamps embedded in the bitstream to modulate an error term used to correct the local clock frequency. When using an over-

sampling DAC, it is necessary to modulate the oversampling clock to the DAC (and hence the L64111 SYSCLK) to correct the errors. This modulation can be achieved with a well designed VCO/PLL combination or, for best results, a VCXO. Note that this is only an issue for oversampling DACs in a broadcast system. Oversampling DACs in a locally sourced system, or baseband DACs in either system do not require an external PLL, because baseband DACs will work with fractional divisors in the TCR register for reasons described earlier.

Calculating the Output Sample Rate

The output sampling rate of the L64111 is typically one of three frequencies: 32 KHz, 44.1 KHz, or 48 KHz. The actual bit rate of the PCM serial output data signal, SDATA, is selectable between 32, 48, and 64 times the output sampling rate. The data is presented MSB first with sign extension, allowing for compatibility with most bit serial DACs. The output sampling rate is provided on pin LRCLKO and its corresponding bit rate is provided on pin SCLKO (Serial Clock Out).

TCR, TORH, and TORL store a clock divisor value, which the L64111 uses to calculate the PCM Serial Output Clock rate (SCLKO). To use them, calculate the appropriate value for each register using the formula given here and then use these values to initialize the three registers. The computed values are dependent on the input SYSCLK frequency and the required Serial Output Clock rate (SCLKO).

First determine the SCLK rate required by the DAC. This may be either 32, 48 or 64 times the sampling frequency. Next determine the output sampling frequency, this will be either 32 KHz, 44.1 KHz or 48 KHz. Use these values in the formula to determine the values of TCR, TORH and TORL.

The four-bit value in the TCR register is used as a terminal count. The 16-bit value in the combination of the TORH and TORL registers is used as the correction fraction. To calculate what these values need to be, the clock rate (in SYSCLK units) is divided by the desired output sampling rate (LRCLKO). The integer portion is stored in the TCR and the fractional portion is stored in the TORH and TORL. During operation, corrections can be made to the values in TORH, TORL, or TCR to adjust the frequency of the output if using a baseband DAC.

TCR Calculation

The equation for determining the value of TCR is shown in Equation 6.1.

Equation 6.1
TCR Calculation

$$TCR = INT\left(\frac{SYSCLK}{2 \times samplerate \times SCLKratio}\right)$$

For example, let the input clock, SYSCLK, equal 28 MHz, the SCLK over-sampling ratio equal 32 and the required output sample rate equal 32 kHz. The value for TCR is then found in Equation 6.2.

Equation 6.2
TCR Example

$$TCR = INT\left(\frac{28MHz}{2 \times 32KHz \times 32}\right) = INT(13.671875) = 13$$

The TCR value in binary ($13 = 0xD = 1101_2$) is written to address $A[4:0] = 00110_2$.

Timer Offset Registers (TORH and TORL) Fraction Value

The fraction value, TOR, is a 16-bit value formed from the 8-bit values in the TORH and TORL registers. The L64111 uses TOR to correct for the error in the TCR register. TORH contains the eight most significant bits of the fraction TOR, and TORL contains the eight least significant bits of TOR. The equation for determining the fraction is found in Equation 6.3.

Equation 6.3
TOR Calculation

$$TOR = fractional\ part\ of\left(\frac{SYSCLK}{2 \times samplerate \times SCLKratio}\right)$$

Using the values from the TCR example given previously, the fractional part of TOR is given in Equation 6.4.

Equation 6.4
TOR Example

$$TOR\ Fraction\ Value = Fract\left(\frac{28MHz}{2 \times 32KHz \times 32}\right) = Fract(13.671875) = 0.671875$$

The value in the TOR register pair is stored as a binary fraction with 16 significant digits. When using a calculator, convert this fractional value to hexadecimal by multiplying the value by 2^{16} and then converting to hex; the hexadecimal point will fall to the left of the most significant digit.

Calculating this value out in binary to 16 significant digits yields (in hex and binary) yields the result shown in Equation 6.5.

Equation 6.5
TOR Hex and Binary
Values

$$TOR\ Fraction\ Value = 0.671875 = 0x0.(AC00) = 0.1010110000000000$$

Thus the value $0xAC = 10101100_2$ should be stored in TORH and the value $0x00 = 00000000_2$ should be stored in TORL.
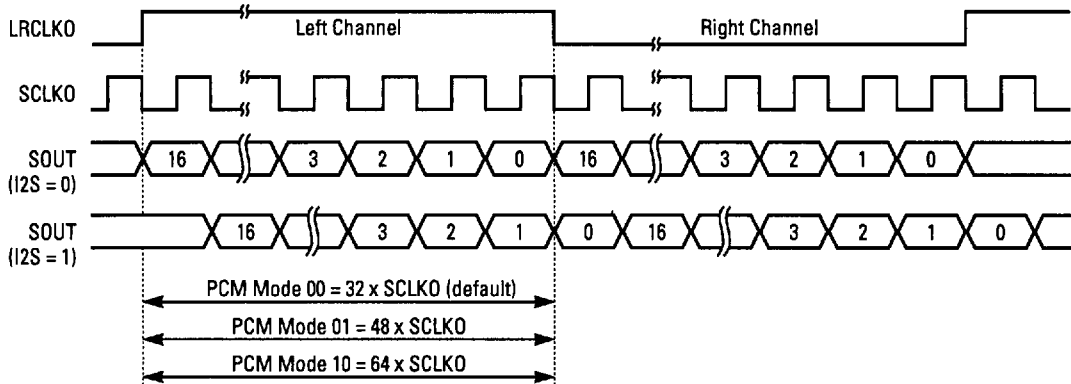
This fractional value is added to an internal 16-bit register every time TCR counts down to zero. Each time this internal register exceeds one, a SYSCLK cycle delay is added to the transition of the output serial clock (SCLKO). On the next cycle the TOR value is added to the remaining fraction and the cycle continues. In this way the fractional corrections continue to be made to the output clock.

Note that a fractional value is not recommended if you are using an over-sampling DAC. In this case, choose an integer value for TCR (typically 8) and set TORL and TORH to zero. Then calculate the required SYSCLK. Note that for correct operation, TCR >= 6.
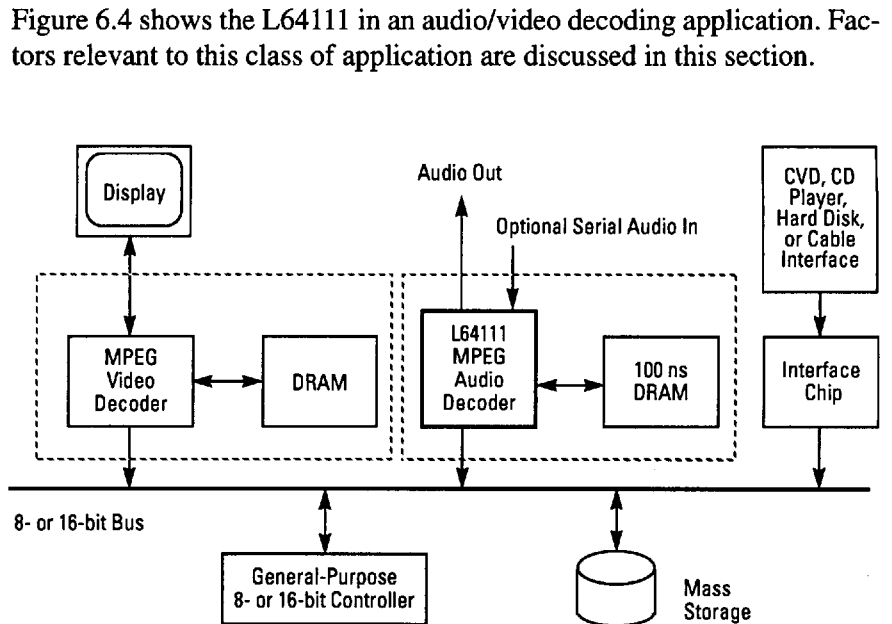

Setting the PCM Output Mode

The PCM data is always sign extended MSB first. The SCLK rate can be set by writing to the PCM MODE bits in Control Register 2. If you are using a DAC compatible with Philips I2S protocol, set the I2S bit in Control Register 2.

Figure 6.3
PCM Output Modes

6.4
Audio/Video
Application

Figure 6.4 shows the L64111 in an audio/video decoding application. Factors relevant to this class of application are discussed in this section.

Figure 6.4
Audio/Video
Application
Elements

For applications including both audio and video, audio/video synchronization is achieved through the use of a system controller. The controller reads timestamp information from the audio and the video decoders and periodically issues a decode start command to the appropriate chip. The following section discusses the process.

Synchronization Using Timecodes

Synchronization of audio and video elementary streams may be performed using the timecode information called the presentation time stamp (PTS) that may optionally be included in every MPEG packet.

When the L64111 recognizes an audio packet, it captures the PTS data and makes it available to be read in its PTS registers. A system controller may acquire this data and use it to synchronize audio and video.

The system controller must read the PTS from both an audio decoder and a video decoder. When the controller detects that the PTS for the audio coincides with the PTS for the video, the controller can send a STARTI signal to both devices (throughput delays must be accounted for).

The assertion of the STARTI signal ensures that the audio is synchronized to the video as long as both audio and video channel buffers are maintained

with enough data (though not allowed to overflow). The controller should occasionally monitor the PTS data so that the two decoders maintain synchronization in case the original sampling frequency and the output sampling frequency drift.

It is not necessary for the video PTS and audio PTS to exactly coincide on every check by the controller, especially because audio packets contain different sample sizes than the video packets

It is possible to advance or delay the audio decoder in two ways. If you are using a baseband DAC, the audio sample rate can be increased or decreased slightly by using the fractional part of the TCR register, which brings the chips back into sync at the cost of a very slight change in pitch. It is also possible to skip an audio frame, or play the same audio frame twice using the Cue and Review feature, explained on page 6-12. Using Cue and Review may produce audible artifacts if done too often. It is also possible to modify the frequency of operation using an external VCO or VCXO, which is the recommended solution in professional quality audio systems.

Note that although up to one second of audio data can be stored in the Channel Buffer, auditory changes are quite noticeable while visual changes may be less obvious. Video should be corrected in order to achieve synchronization with audio rather than audio to video.

Input Buffering Considerations

In applications using parallel data transfer to the L64111, the system controller must regulate its delivery of data to the decoder.

The system controller may monitor the status of the L64111's Input Data FIFO and regulate parallel data transfers to the buffer by means of three FIFO flags. The Input Data FIFO has three flags that allow the external controller to monitor its status: the FIFO Almost Full Flag ($\overline{\text{FALF}}$), the FIFO Almost Empty Flag ($\overline{\text{FALE}}$), and the FIFO Empty Flag ($\overline{\text{FEMPTY}}$).

When $\overline{\text{FALF}}$ goes LOW, the system controller must stop transferring data to the L64111, as the FIFO is almost full and an overflow may occur.

It is important that the channel buffer not underrun or overrun in normal operation because incorrect decoding could result. The most audible artifact is a clicking sound. Note that if the encoder is supplying data even marginally slower than the rate at which the decoder processes it, the buffer will eventually underrun, which results in the output being muted.

Once the buffer has underrun in this way, the decoder must be reset and the channel buffer allowed to fill to a satisfactory level before decoding begins again. If the encoder is supplying data even marginally faster than the decoder processes it, the buffer will overrun, which produces a click, and the decoder continues to play. In systems with a local source of encoded data it is easy to prevent channel overrun or underrun by examining the channel buffer status register, then reducing or increasing the data transfer rate. In systems with a remote encoder with no feedback to it, the situation is more complex. Refer to Section 6.3, "DAC Interfacing," for more details.

Cue and Review

Timestamp information that is part of an audio packet is stored in the Presentation Time Stamp registers. The data in the PTS registers can be used for fast forwarding, cueing, or reviewing.

The L64111 supports Cue and Review control by allowing the system controller to read and write the Channel Buffer's read and write pointers. A complex scheme of cue and review can be implemented by writing new values to the read and write pointers as needed.

The number of frames stored by the Channel Buffer depends on the type of Layer being decoded. The number of frames for Layer I is 128 and the number of frames for Layer II is 64. Note that the L64111 will always play each frame of data in the forward direction, even if the read pointer is being moved backwards through the channel buffer. It is only possible to reorder the frames, not the data within the frames.

Appendix A
Customer Feedback

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