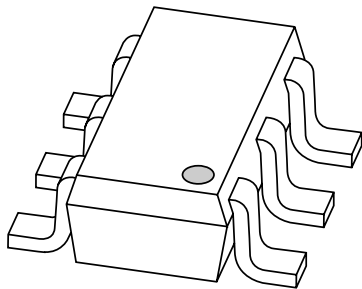


DATA SHEET



PIMH9

NPN resistor-equipped double
transistor; $R1 = 10\text{ k}\Omega$, $R2 = 47\text{ k}\Omega$

Product specification

2001 Sep 13

NPN resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

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FEATURES

- Transistors with built-in bias resistors (R1 typ. 10 kΩ and R2 typ. 47 kΩ)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

NPN resistor-equipped double transistor in an SC-74 (SOT457) plastic package.

MARKING

TYPE NUMBER	MARKING CODE
PIMH9	H9

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	50	V
I _{CM}	peak collector current	100	mA
R1	bias resistor	10	kΩ
R2	bias resistor	47	kΩ

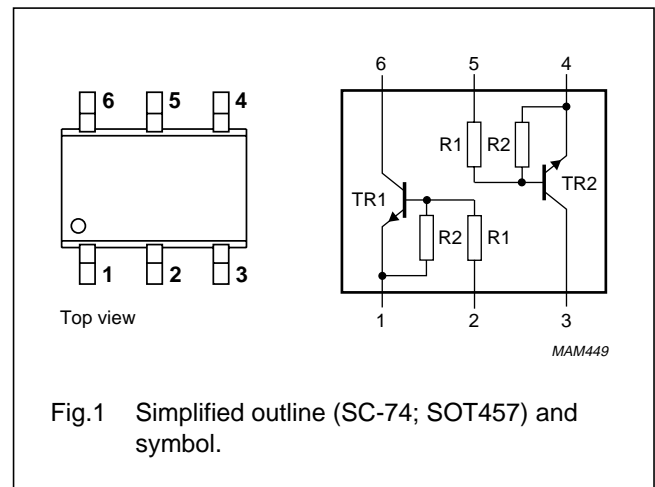


Fig.1 Simplified outline (SC-74; SOT457) and symbol.

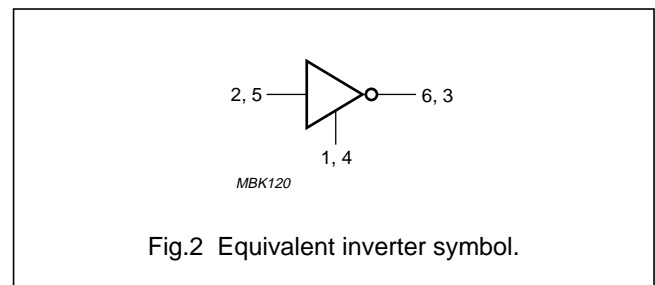


Fig.2 Equivalent inverter symbol.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_I	input voltage		–	+40	V
			–	–10	V
I_O	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		–65	+150	$^\circ\text{C}$
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1	–	600	mW

Note

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	208	K/W

Note

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².

NPN resistor-equipped double transistor;
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CHARACTERISTICS

$T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor						
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = 50 \text{ V}$; $I_{\text{E}} = 0$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = 50 \text{ V}$; $I_{\text{B}} = 0$	–	–	1	μA
		$V_{\text{CE}} = 30 \text{ V}$; $I_{\text{B}} = 0$; $T_{\text{j}} = 150 \text{ }^\circ\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = 5 \text{ V}$; $I_{\text{C}} = 0$	–	–	150	μA
h_{FE}	DC current gain	$V_{\text{CE}} = 5 \text{ V}$; $I_{\text{C}} = 5 \text{ mA}$	100	–	–	
V_{CEsat}	saturation voltage	$I_{\text{C}} = 5 \text{ mA}$; $I_{\text{B}} = 0.25 \text{ mA}$	–	–	100	mV
$V_{\text{i(off)}}$	input off voltage	$V_{\text{CE}} = 5 \text{ V}$; $I_{\text{C}} = 100 \mu\text{A}$	–	0.7	0.5	V
$V_{\text{i(on)}}$	input on voltage	$V_{\text{CE}} = 0.3 \text{ V}$; $I_{\text{C}} = 1 \text{ mA}$	1.4	0.8	–	V
R_1	input resistor		7	10	13	$\text{k}\Omega$
$\frac{R_2}{R_1}$	resistor ratio		3.7	4.7	5.7	
C_{c}	collector capacitance	$I_{\text{E}} = i_{\text{e}} = 0$; $V_{\text{CB}} = 10 \text{ V}$; $f = 1 \text{ MHz}$	–	–	2.5	pF

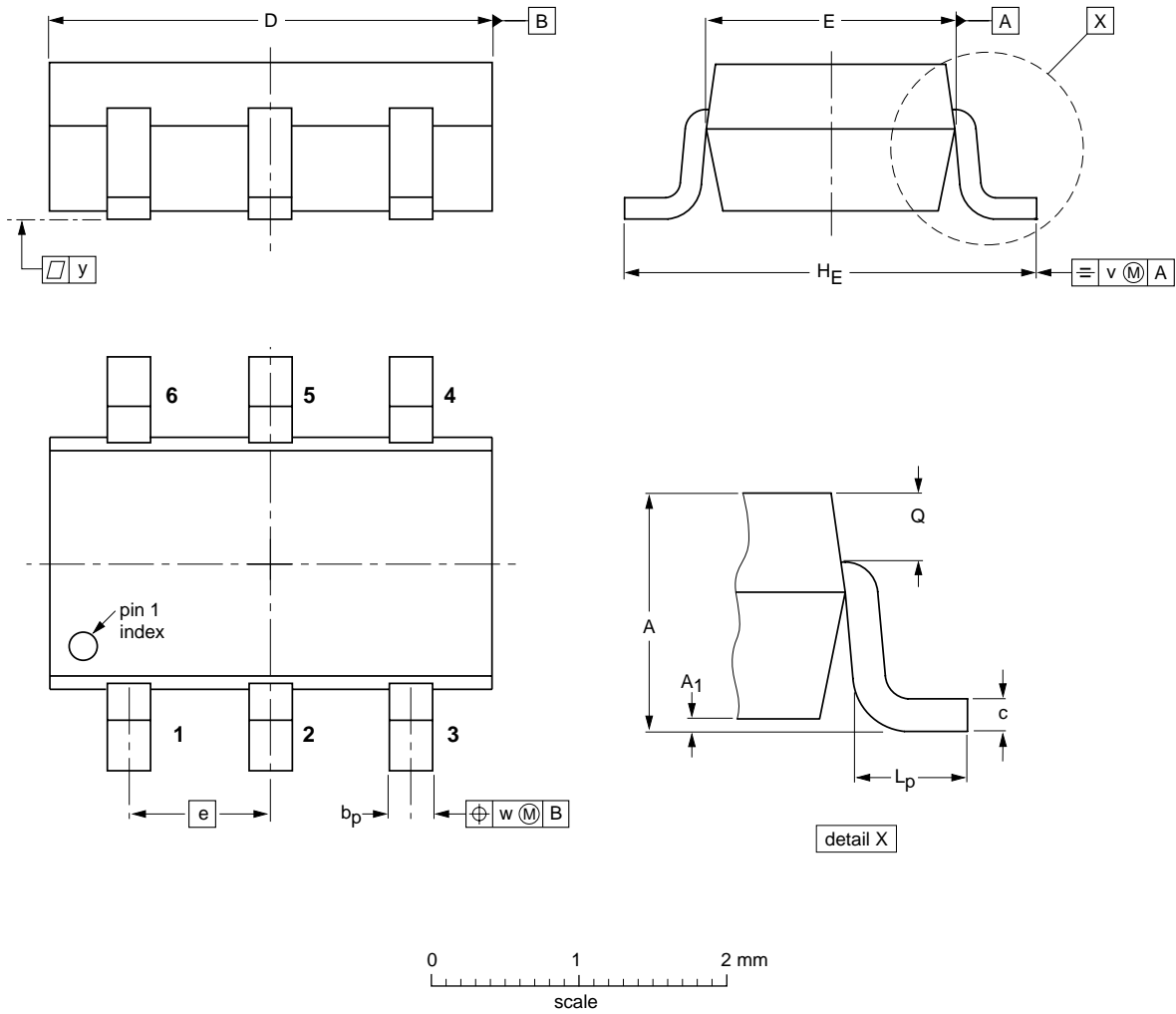
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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			-97-02-28- 01-05-04

NPN resistor-equipped double transistor;
R1 = 10 kΩ, R2 = 47 kΩ

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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