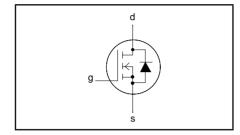
PSMN020-150W

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$$V_{DSS} = 150 \text{ V}$$
 $I_D = 73 \text{ A}$
 $R_{DS(ON)} \le 20 \text{ m}\Omega$

GENERAL DESCRIPTION

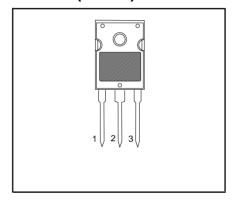
N-channel enhancement mode field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PSMN020-150W is supplied in the SOT429 (TO247) conventional leaded package.

PINNING

PIN	DESCRIPTION	
1	gate	
2	drain	
3	source	
tab	drain	

SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T _i = 25 °C to 175°C	-	150	V
V_{DGR}	Drain-gate voltage	$T_i = 25 ^{\circ}\text{C}$ to 175 $^{\circ}\text{C}$; $R_{GS} = 20 \text{k}\Omega$	-	150	V
V _{GS}	Gate-source voltage	, , , , , , , , , , , , , , , , , , , ,	-	± 20	V
l _D	Continuous drain current	$T_{mb} = 25 ^{\circ}C$	-	73	Α
		T _{mb} = 100 °C	-	51	Α
I _{DM}	Pulsed drain current	$T_{mb}^{mb} = 25 ^{\circ}C$	-	290	Α
P _D	Total power dissipation	T _{mb} = 25 °C	-	300	W
	Operating junction and		- 55	175	°C
, s.g	storage temperature				

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E _{AS}	Non-repetitive avalanche	Unclamped inductive load, I _{AS} = 64 A;	-	1255	mJ
I _{AS}	Non-repetitive avalanche current	$\begin{array}{l} t_p = 0.2 \text{ ms; } T_j \text{ prior to avalanche} = 25 ^{\circ}\text{C;} \\ V_{DD} \leq 25 \text{ V; } R_{GS} = 50 \Omega; V_{GS} = 5 \text{ V} \end{array}$	1	73	А

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
R _{th j-mb}	Thermal resistance junction		-	0.5	K/W
R _{th j-a}	to mounting base Thermal resistance junction to ambient	in free air	45	-	K/W

ELECTRICAL CHARACTERISTICS

T_i= 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA};$	150	-	-	V
	voltage	$T_j = -55^{\circ}C$	133	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1 \text{ mA}$	2.0	3.0	4.0	V
		$T_{j} = 175^{\circ}C$ $T_{i} = -55^{\circ}C$	1.0	-	-	V
_			-	-	4.4	V
$R_{DS(ON)}$	Drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}$	-	18	20	mΩ
	resistance	$T_{j} = 175^{\circ}C$	-	-	57	mΩ
I _{GSS}	Gate source leakage current	$V_{GS} = \pm 10 \text{ V}; V_{DS} = 0 \text{ V}$	-	2	100	nA
I _{DSS}	Zero gate voltage drain	$V_{DS} = 150 \text{ V}; V_{GS} = 0 \text{ V};$	-	0.05	10 500	μΑ
	current	$T_j = 175^{\circ}C$	-	-	500	μΑ
$Q_{g(tot)}$	Total gate charge	$I_D = 73 \text{ A}; V_{DD} = 120 \text{ V}; V_{GS} = 10 \text{ V}$	-	164	-	nC
Q_{gs}	Gate-source charge		-	30	-	nC
Q_gd	Gate-drain (Miller) charge		-	77	-	nC
t _{d on}	Turn-on delay time	$V_{DD} = 75 \text{ V}; R_D = 3 \Omega;$	-	50	-	ns
t _r	Turn-on rise time	$V_{GS} = 10 \text{ V}; R_G = 5 \Omega$	-	114	-	ns
t _{d off}	Turn-off delay time	Resistive load	-	214	-	ns
t _f	Turn-off fall time		-	114	-	ns
L _d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nΗ
L _d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nΗ
Ls	Internal source inductance	Measured from source lead to source	-	7.5	-	nΗ
•		bond pad				
C _{iss}	Input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	-	6429	7000	pF
Coss	Output capacitance	,	-	785	810	pF
Crss	Feedback capacitance		-	435	500	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_i = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	73	Α
I _{SM}	Pulsed source current (body diode)		-	-	290	Α
V_{SD}	Diode forward voltage	$I_F = 25 \text{ A}; V_{GS} = 0 \text{ V}$ $I_F = 75 \text{ A}; V_{GS} = 0 \text{ V}$	1 1	0.85 1.1	1.2 -	V V
t _{rr} Q _{rr}	Reverse recovery time Reverse recovery charge	$I_F = 20 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s};$ $V_{GS} = 0 \text{ V}; V_R = 30 \text{ V}$	-	200 1.5	-	ns μC

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MECHANICAL DATA

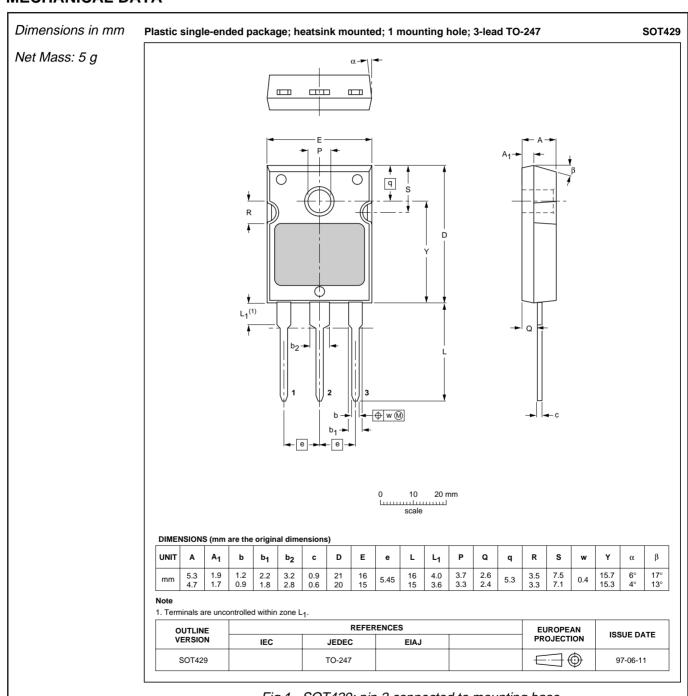


Fig.1. SOT429; pin 2 connected to mounting base.

Notes

- 1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
- 2. Refer to mounting instructions for SOT429 envelope.
- 3. Epoxy meets UL94 V0 at 1/8".

PSMN020-150W

DEFINITIONS

Data sheet status		
Objective specification	This data sheet contains target or goal specifications for product development.	
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.	
Product specification This data sheet contains final product specifications.		
Limiting values		

Limiting values

Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

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