HARRIS Semiconductor

HS-565ARH

Radiation Hardened High Speed, Monolithic Digital-to-Analog Converter

March 1996

Features

- **Devices QML Qualified in Accordance with MIL-PRF-38535**
- **Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96755 and Harris' QM Plan**
- **DAC and Reference on a Single Chip**
- **Pin Compatible with AD-565A and HI-565A**
- **Very High Speed: Settles to 0.50 LSB in 500ns Max**
- **Monotonicity Guaranteed Over Temperature**
- **0.50 LSB Max Nonlinearity Guaranteed Over Temperature**
- **Low Gain Drift (Max., DAC Plus Reference) 50ppm/^{o}C**
- **Total Dose Hardness to 100K RAD**
- **±0.75 LSB Accuracy Guaranteed Over Temperature (±0.125 LSB Typical at +25^{o}C)**

Applications

- **High Speed A/D Converters**
- **Precision Instrumentation**
- **Signal Reconstruction**

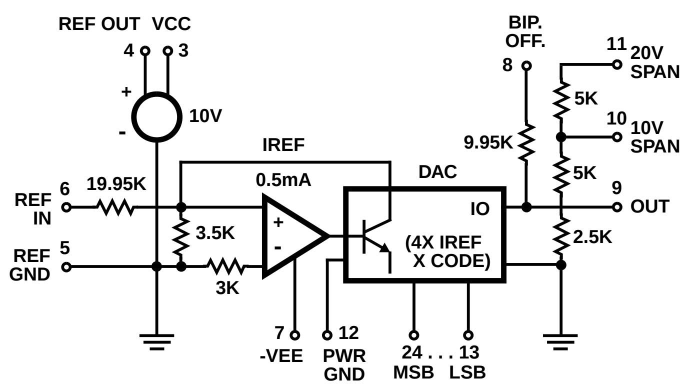
Description

The HS-565ARH is a fast, radiation hardened 12-bit current output, digital-to-analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Harris Semiconductor Dielectric Isolation process provides latch-up free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HS-565ARH die are laser trimmed for a maximum integral nonlinearity error of ±0.25 LSB at +25^{o}C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

Functional Diagram



Ordering Information

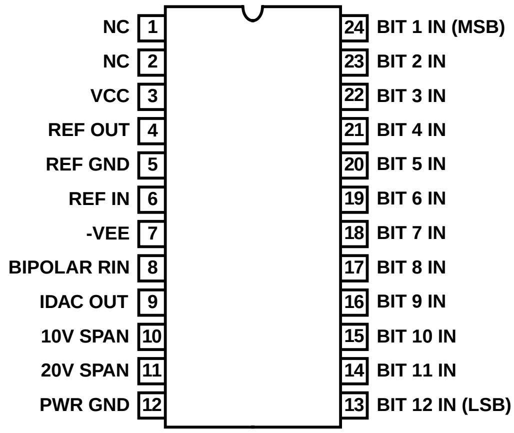
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962R9675501VJC	-55^{o}C to +125^{o}C	MIL-PRF-38535 Level V	24 Lead SBDIP
5962R9675501VXC	-55^{o}C to +125^{o}C	MIL-PRF-38535 Level V	24 Lead Ceramic Flatpack
HS1-565ARH (SAMPLE)	+25^{o}C	Sample	24 Lead SBDIP
HS9-565ARH (SAMPLE)	+25^{o}C	Sample	24 Lead Ceramic Flatpack

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

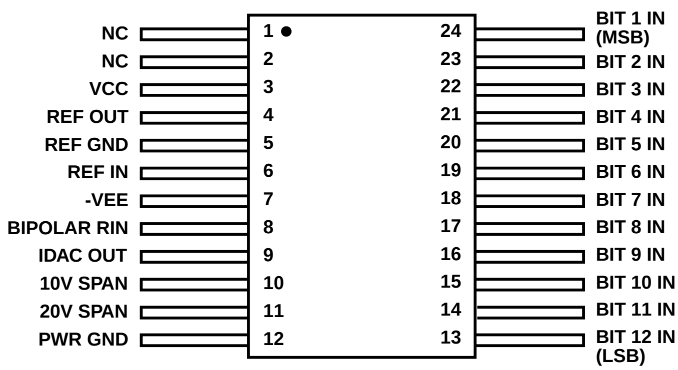
Spec Number **518795**
File Number **3278.2**

Pinouts

HS1-565ARH
MIL-STD-1835 CDIP2-T24
(SBDIP)
TOP VIEW



H59-565ARH
MIL-STD-1835 CDFP4-F24
(CERAMIC FLATPACK)
TOP VIEW



Absolute Maximum Ratings

VCC to Power Ground . . . . 0V to +18V
VEE to Power Ground . . . . 0V to -18V
Voltage on DAC Output (Pin 9). -3V to +12V
Digital Input (Pins 13 - 24) to Power Ground . . . . -1V to +7V
Ref In to Reference Ground . . . . ±12V
Bipolar Offset to Reference Ground . . . . ±12V
10V Span R to Reference Ground. . . . . ±12V
20V Span R to Reference Ground. . . . . ±24V
Junction Temperature (TJ) (Max) . . . . +175°C
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering 10s). +300°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	60	17
Ceramic Flatpack Package	80	15

Maximum Package Power Dissipation at +125°C
SBDIP Package 0.83W
Ceramic Flatpack Package 0.62W

If Device Power Exceeds Package Dissipation Capability, Provide Heat Sinking or Derate Linearly at the Following Rate:
SBDIP Package 16.67mW/°C
Ceramic Flatpack Package 12.5mW/°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VCC) . . . . +11.4V to +16.5V
Operating Voltage Range (VEE). . . . . -11.4V to -16.5V
Operating Temperature Range . . . . -55°C to +125°C
Digital Input Low Voltage. . . . . 0V to +0.8V
Digital Input High Voltage . . . . +2.2V to +5.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUP	TEMPERATURE	LIMITS MIN	TYP	MAX	UNITS
Resolution		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	-	12	Bits
Accuracy	ILE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Error Relative to Full Scale	1, 2, 3	-55°C to +125°C	-	±0.125	±0.75	LSB
Digital Input High Current	IIH	VSSD = VSSA = 0V, VIN = 5.5V VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	0.01	+1.0	µA
Digital Input Low Current	IIL	VSSD = VSSA = 0V, V_{IN} = 0V VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-20	-2.0	-	µA
Differential Nonlinearity	DLE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, +25°C (Monotonicity Guaranteed Over Temp)	1, 2, 3	-55°C to +125°C	-	±0.25	±0.50	LSB
Power Supply Currents VCC	ICC	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	9.0	11.8	mA
VEE	IEE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-14.5	-9.5	-	mA
Reference Output Voltage	Ref Out	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	9.9	10	10.1	V
Reference Output Current	IREF	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Available for external loads	1, 2, 3	-55°C to +125°C	1.5	2.5	-	mA
Output Current Unipolar	I_{OUT1}	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, All Bits On	1, 2, 3	-55°C to +125°C	-1.6	-2.0	-2.4	mA
Bipolar	I_{OUT2}	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, All Bits On or Off	1, 2, 3	-55°C to +125°C	±0.8	±1.0	±1.2	mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUP	TEMPERATURE	LIMITS MIN	TYP	MAX	UNITS
Output Offset								
Unipolar	VOS	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V Figure 3, R2 = 50Ω Fixed	1, 2, 3	-55°C to +125°C	-	±0.01	±0.05	% of F.S.
Bipolar	BPOE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, R3 and R4 = 50Ω Fixed Figure 4	1, 2, 3	-55°C to +125°C	-	±0.05	±0.15	% of F.S.
Power Supply Gain Sensitivity								
VCC	+PSS	Note 3	1, 2, 3	-55°C to +125°C	-	3	10	ppm of F.S./%
VEE	-PSS	Note 3	1, 2, 3	-55°C to +125°C	-	15	25	ppm of F.S./%
Temperature Coefficients								
Unipolar Zero		With Internal Reference	1, 2, 3	-55°C to +125°C	-	1	2	ppm/°C
Bipolar Zero		With Internal Reference	1, 2, 3	-55°C to +125°C	-	5	20	ppm/°C
Gain (Full Scale)		With Internal Reference	1, 2, 3	-55°C to +125°C	-	10	50	ppm/°C
External Adjustments	AE	Fixed 50Ω Resistor for R2 Figures 3	1, 2, 3	-55°C to +125°C	-	±0.10	±0.25	% of F.S.
Gain Error	BPAE	Fixed 50Ω Resistor for R3 and R4, Figure 4	1, 2, 3	-55°C to +125°C	-	±0.10	±0.25	% of F.S.
Bipolar Zero Error	BPZE	Fixed 50Ω Resistor for R3 and R4, Figure 4	1, 2, 3	-55°C to +125°C	-	±0.05	±0.10	% of F.S.

NOTES:

1. All voltages referenced to VSSD = VSSA = 0V
2. Unless otherwise specified VCC = +15V and VEE = -15V.
3. The Power Supply Gain Sensitivity is tested in reference to a VCC = +15V and VEE = -15V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Specifications in Table 3

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	TYP	MAX	UNITS
Output Capacitance	COUT	f = 1MHz	1, 2	+25°C	-	20	-	pF
Output Compliance Voltage			1	-55°C to +125°C	-1.5	-	10	V
Programmable Output Ranges			1	-55°C to +125°C	0	-	5	V
			1	-55°C to +125°C	-2.5	-	2.5	V
			1	-55°C to +125°C	0	-	10	V
			1	-55°C to +125°C	-5	-	5	V
			1	-55°C to +125°C	-10	-	10	V
Gain Adjustment Range		Figures 3, 4	1	-55°C to +125°C	±0.25	-	-	% of F.S.
Bipolar Zero Adjustment Range		Figure 4	1	-55°C to +125°C	±0.15	-	-	% of F.S.
Reference Input Impedance	RREF	VSSD = VSSA = 0V, -15 VCC = +15V, VEE = -15V	1	-55°C to +125°C	15K	20K	25K	Ω
Output Resistance	ROUT	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Exclusive of Span Resistors	1	-55°C to +125°C	1.8K	2.5K	3.2K	Ω

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	TYP	MAX	UNITS
Settling Time (Note 3)	TS1	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, High Z External Load	1	-55°C to +125°C	-	350	500	ns
	TS2	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, 75Ω External Load	1	-55°C to +125°C	-	150	250	ns
Full Scale Transition								
Rise Time	TRISE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1	-55°C to +125°C	-	15	30	ns
Fall Time	TFALL	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1	-55°C to +125°C	-	30	60	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process and are not tested. These parameters are characterized upon initial design release.
2. 24 lead DIP package only.
3. Reference the Settling Time discussion and Figure 3.

TABLE 4. POST 100 K RAD ELECTRICAL PERFORMANCE

Post 100K RAD Electrical Performance Is Per Table 1 (+25°C Only) Except As Follows:

PARAMETER	SYMBOL	CONDITIONS: +25°C ONLY	LIMITS MIN	MAX	UNITS
DIGITAL INPUTS					
Low Current	I_{IL}	V_{IN} = 0.0V	-40	-	µA
Low Voltage	V_{IL}	(Note 1)	-	0.5	V
High Voltage	V_{IH}	(Note 1)	2.5	-	V
UNIPOLAR					
Full Scale Error	AE	Figure 3, R2 = 50Ω Fixed	-	±0.85	% of F.S.
BIPOLAR					
Offset Error	BPOE	Figure 4, R3 and R4 = 50Ω Fixed	-	±0.25	% of F.S
Zero Error	BPZE	Figure 5, R3 and R4 = 50Ω Fixed	-	±0.25	% of F.S.
Full Scale Error	BPAE	Figure 5, R3 and R4 = 50Ω Fixed	-	±0.85	% of F.S.
Differential Nonlinearity	DLE	Monotonicity Guaranteed	-	±1.0	LSB
Accuracy	ILE	Error Relative to Full Scale	-	±1.0	LSB

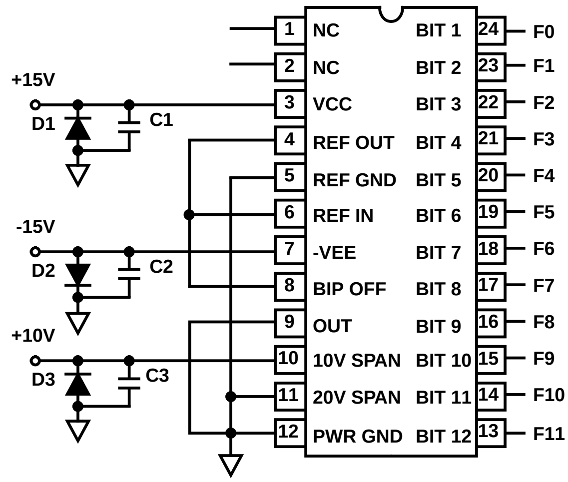
NOTES:

1. This parameter is an applied condition of test.

TABLE 5. BI DELTA PARAMETERS (±25°C)

PARAMETER	DELTA LIMIT
I_{CC}	±1.18mA
I_{EE}	±1.45mA
I_{OUT1}	±240µA
I_{OUT2}	±240µA
VOS	±0.02%
AE	±0.15%
BPOE	±0.10%
BPZE	±0.10%
I_{IL}	±1.0µA
I_{IH}	±40nA

Burn-In Bias Circuit



NOTES:

D1 = D2 = D3 = IN4002 or Equivalent

F0 to F11: VIH = 5.0V ±0.5V

VIL = 0.0V ±0.5V

F0 = 100kHz ±10% (50% Duty Cycle)

F1 = F0/2 F7 = F0/128

F2 = F0/4 F8 = F0/256

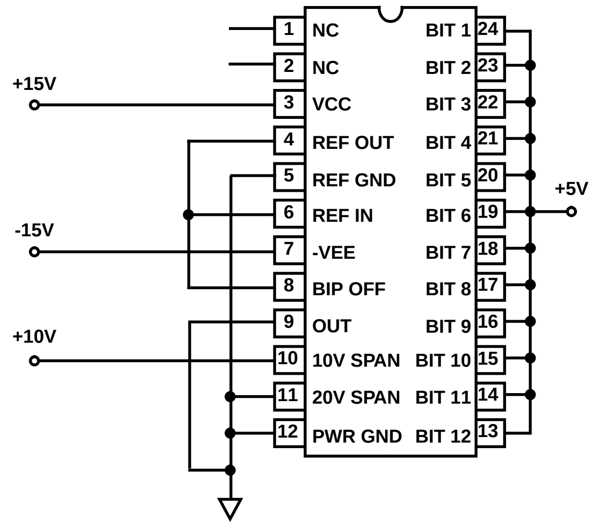
F3 = F0/8 F9 = F0/512

F4 = F0/16 F10 = F0/1024

F5 = F0/32 F11 = F0/2048

F6 = F0/64

Radiation Bias Circuit



NOTE:

Power Supply Levels are ±0.5V

Definitions of Specifications

Digital Inputs

The HS-565ARH accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, Two's Complement (see note below), or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
MSB . LSB	STRAIGHT BINARY	OFFSET BINARY	(NOTE) TWO'S COMPLEMENT
000 . . . 000	Zero	-FS (Full Scale)	Zero
100 . . . 000	0.50 FS	Zero	-FS
111 . . . 111	+FS - 1LSB	+FS - 1LSB	Zero - 1LSB
011 . . . 111	0.50 FS - 1LSB	Zero - 1LSB	+FS - 1LSB

NOTE: Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

Nonlinearity - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

Differential Nonlinearity - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

Settling Time

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 0.50 LSB of final value.

Drift

Gain Drift - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per ^oC (ppm of FSR/^oC). Gain error is measured with respect to +25^{o}C at high (TH) and low (TL) temperatures. Gain drift is calculated for both high (TH - 25^{o}C) and low ranges (+25^{o}C - TL) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

Offset Drift - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^oC (ppm of FSR/^oC). Offset error is measured with respect to +25^{o}C at high (TH) and low (TL) temperatures. Offset drift is calculated for both high (TH - 25^{o}C) and low (+25^{o}C - TL) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half scale or the major carry code transition from 011 . . . 1 to 100 . . . 0 or vice versa. For example, if turn ON is greater than turn OFF for 011 . . . 1 to 100 . . . 0, an intermediate state of 000 . . . 0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HS-565ARH

OP AMP Selection

The HS-565ARH's current output may be converted to voltage using the standard connections shown in Figures 3 and 4. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy. Remember settling time for the DAC-amplifier combination is

$$\sqrt{(t_D)^2 + (t_A)^2}$$

where t_D, t_A are settling times for the DAC and amplifier.

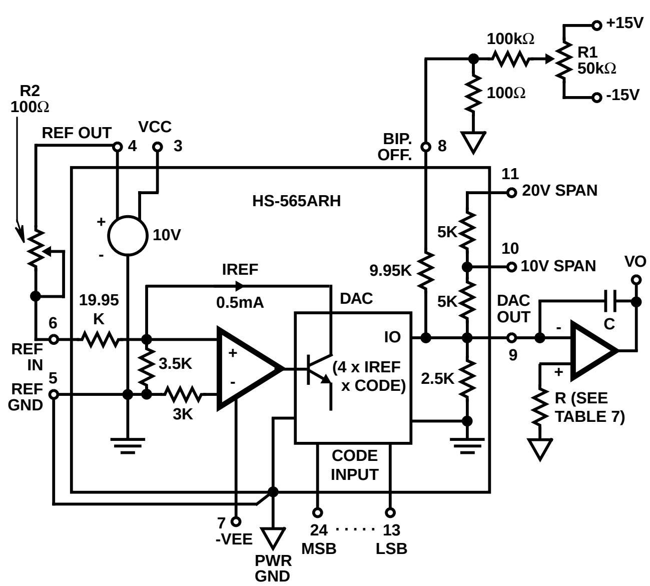


FIGURE 3. UNIPOLAR VOLTAGE OUTPUT

No Trim Operation

The HS-565ARH will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 3 replace R2 with 50Ω; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 4, replace R3 and R4 with 50Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, “External Adjustments”. Typical unipolar zero will be ±0.50 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

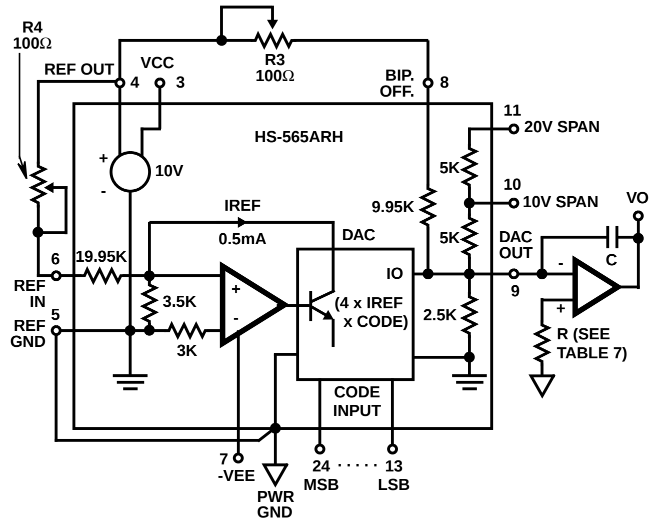


FIGURE 4. BIPOLAR VOLTAGE OUTPUT

Calibration

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero, For the HS-565ARH, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 7 for the voltage output case, along with Figure 3 or 4.

Calibration is a two step process for each of the five output ranges shown in Table 7. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum values is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test methods before using the specified settling time as a basis for design.

The approach used for several years at Harris calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814mV for the HS-565ARH, which provides the comparator with enough overdrive to establish an accurate ±0.50 LSB window about the final settled value. Also, the required test conditions simulate the DACs environment for a common application - use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (tON) or on-to-off (tOFF). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of 0.50 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) tON, to final value +0.50 LSB

(b) tON, to final value -0.50 LSB

(c) tOFF, to final value +0.50 LSB

(d) OFF, to final value -0.50 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 0.50 LSB). For example, refer to Figures 5A and5B for the measurement of case (d).

Procedure

As shown in Figure 5B, settling time equals tX plus the comparator delay (tD = 15ns). To measure tX,

- Adjust the delay on generator number 2 for a tX of several microseconds. This assures that the DAC output has settled to its final wave.
- Switch on the LSB (+5V)
- Adjust the VLSB supply for 50% triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 5B. Note DVM reading.
- Switch to LSB to Pulse (P)
- Readjust the VLSB supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the VLSB supply to reduce the DVM reading by 5 LSBs (DVM reads 10X, so this sets the comparator to sense the final settled value minus 0.50 LSB). Comparator output disappears.
- Reduce generator number 2 delay until comparator output reappears, and adjust for “equal brightness”.
- Measure tX from scope as shown in Figure 5B. Settling time equals tX + tD, i.e. tX + 15ns.

TABLE 7. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS				CALIBRATION		
	OUTPUT RANGE	PIN 10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET VO
Unipolar (See Figure 3)	0 to +10V	VO	Pin 10	1.43K	All 0’s All 1’s	R1 R2	0V +9.99756V
	0 to +5V	VO	Pin 9	1.1K	All 0’s All 1’s	R1 R2	0V +4.99878V
Bipolar (See Figure 4)	±10V	NC	VO	1.69K	All 0’s All 1’s	R3 R4	-10V +9.99512V
	±5V	VO	Pin 10	1.43K	All 0’s All 1’s	R3 R4	-5V +4.99756V
	±2.5V	VO	Pin 9	1.1K	All 0’s All 1’s	R3 R4	-2.5V +2.49878V

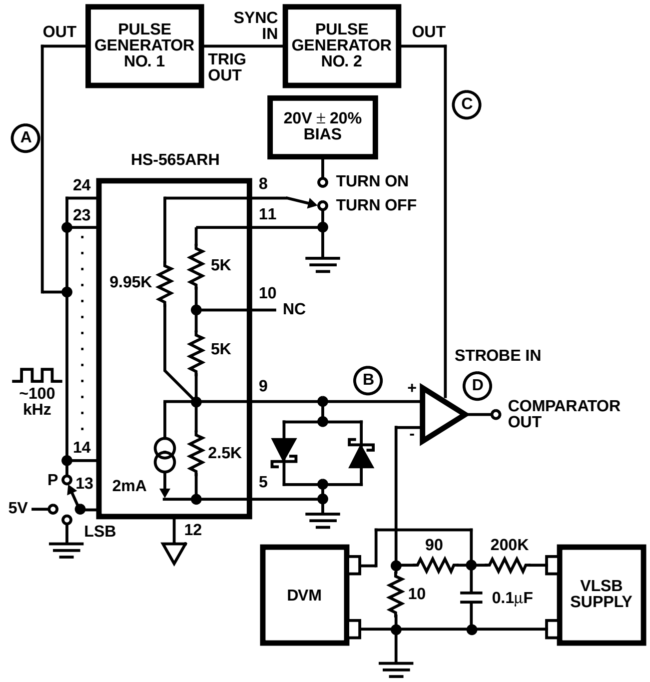


FIGURE 5A.

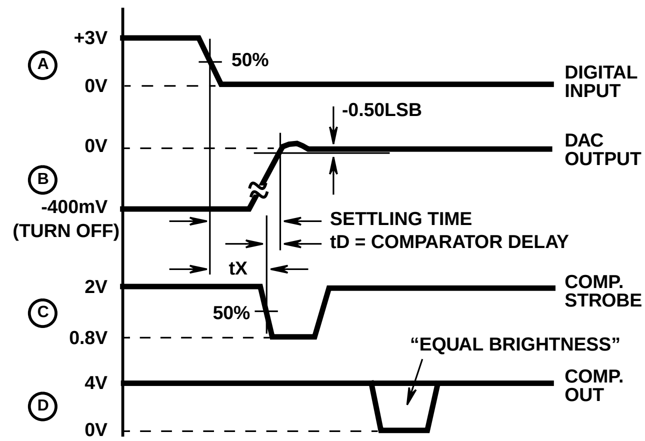


FIGURE 5B.

Other Considerations

Grounds

The HS-565ARH has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near zero DC (Note); but pin 12 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/ signal and digital/power grounds.

NOTE: Current cancellation is a two step process within the HS-565ARH in which code dependent variations are eliminated, the resulting DC current is supplied internally. First an auxiliary 9-bit R-2R ladder is driven by the complement of the DACs input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of the DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

Layout

Connections to pin 9 (IOUT) on the HS-565ARH are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change of additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

Bypass Capacitors

Power supply bypass capacitors on the op amp will serve the HS-565ARH also. If no op amp is used, a 0.01µF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

Die Characteristics

Transistor Count 200
Die Size . . . . 179 mils x 107 mils
Tie Substrate to .Reference Ground
Process. . . . . Bipolar - DI

Die Characteristics

DIE DIMENSIONS:
179 mils x 107 mils x 19 mils

METALLIZATION:
Type: Al/Copper
Thickness: 16kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2

Metallization Mask Layout

HS-565ARH