Austria Mikro Systeme International AG

ASCell3912

ISM 868 MHz, 433 MHz and 315 MHz FSK Receiver Cell

Preliminary Data Sheet

Key Features

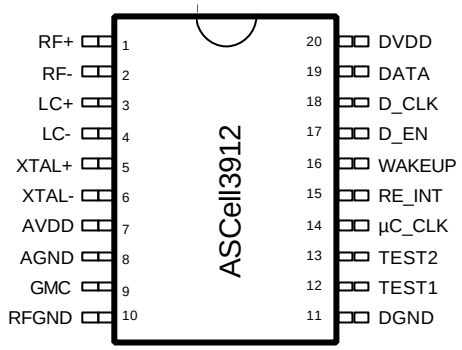
- Supports triple band operation: Europe 868 MHz and 433 MHz-, US and Japan 315 MHz ISM band.
- Designed to be conform to EN 300 220, and FCC 47 CFR Ch.1 par.15 requirements.
- Provides highly reliable packet oriented data transmission in blocks of 128 bit.
- Event oriented single message transmission and status oriented and continuous message transmission supported.
- Special transmission protocol for high reliability even in presence of burst interferer (e.g. GSM) implemented.
- RX sensitivity of the receiver typical -100 dBm.
- Supports clock for an external µC and allows clock free total shut down of the whole system.
- Wide supply range between 2.7 to 5.5 V.
- Low RX current, typical 10 mA @ 2.4 V.
- Low idle mode current, typical 1.2mA.
- Wide operating temperature range from –40 °C to +85 °C.
- Only a low cost XTAL for 25 ppm (868 MHz) or 50 ppm (433 and 315 MHz) reference frequency tolerance required.
- Minimum only 1 XTAL and 4 capacitors externally required.

General Description

The ASCell3912 is a low power, triple ISM band (868 / 433 / 315 MHz), single channel FSK receiver designed to work in a remote control link together with the SC3911 transmitter system cell.
The ASCell3912 performs packet oriented data transmission, in a single message- or continuos-message mode using a special protocol to ensure high reliability even in presence of strong pulsed interferers in close adjacent bands like e.g. GSM.
A general bi-directional micro-controller (µC) interface is provided, to support the µC with clock- and reset- signal, and to operate the highly efficient power up/down management.
As external components the SC3911 need at minimum only a reference XTAL, and 4 capacitors.

Applications

- Key-less car entry systems.
- Short range packet oriented data transmission.
- Security applications and alarm systems.
- Domestic remote control systems.
- Industrial remote control systems.
- Remote metering.



TSSOP-20

This pin-out is preliminary and will change for the real implementation!

This document contains information on products under development. Austria Mikro Systeme International AG reserves the right to change or discontinue this product without notice.

1 Functional Description

The Figure 1 shows the block diagram of the ASCell3912. The analog part of the ASCell3912 consists of a direct conversion receiver, a triple band RF synthesizer and the DC-cancellation. The digital part includes the burst interference resistant protocol decoder the control logic and the µC interface.

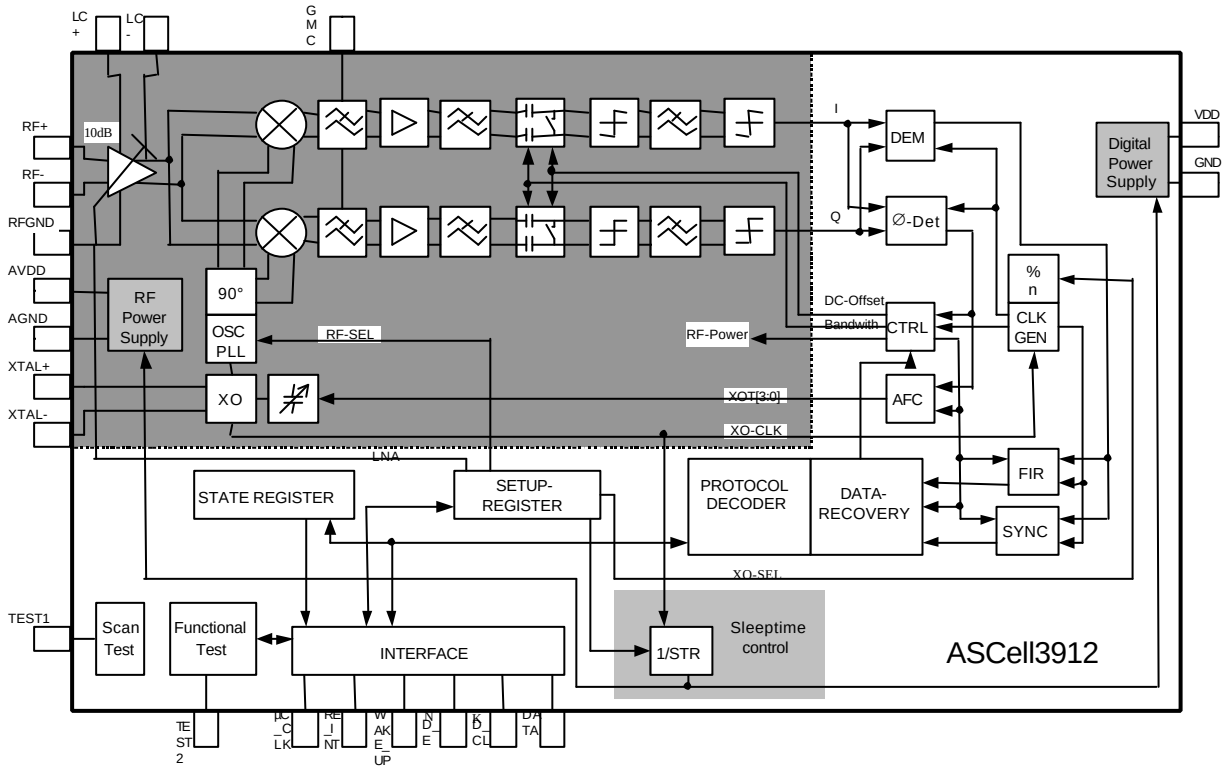


Figure 1: Block diagram of the ASCell3912.

1.1 Analog Receiver Part

The input signal is a low to moderately high modulation index continuous phase frequency shift keying modulated RF signal around a carrier Fc. This signal is amplified by the low noise amplifier (LNA) and fed to the In-phase and Quadrature-phase mixers (I/Q mixers). The mixers convert the RF signal directly to base band. The local oscillator signal for the I/Q mixers is generated by the on-chip PLL.
The two base band signals (signals I and Q) are filtered and further amplified. After DC offset cancellation to remove the static and quasi-static DC offsets and to ensure fast wake-up of the receiver, the signals are hard limited. The rectangular signals I' and Q' are fed to the digital part where demodulation and the further signal processing is applied.

1.1.1 RF Synthesizer

Frequency synthesis is performed by a conventional synthesizer consisting of a phase detector, a charge pump, a voltage controlled oscillator working at 315~868.3 MHz, and a feedback divider by 16 (315.00MHz); 32 (315, 433.92MHz), or 64 (868.3MHz). A truth table for the different frequencies is given in Table 1.

F_{XOSC} / MHz	Multiplier	F_C/ MHz	FB1	FB0	RF-SEL	XO-SEL
19,6875	16	315.000	H	L	L	L
13.5600	32	433.920	L	H	L	H
13.5672	64	868.300	L	L	H	H

Table 1: Quartz and RF output frequencies.

Note: XO-SEL and RF-SEL are intenal generated Signals from the FB[1:0] bits of the setup information.

1.1.2 LNA

The amplification of the LNA can be switched in two states. The gain can be switched of about 10dB with the LNA bit of the setup command.

Note: LNA is one bit of the setup information.

1.1.3 I/Q Down Converter

The ASCell3912 contains a high performance quadrature down converter with low DC offset and high isolation of RF- and LO-ports.

1.1.4 Base Band Filter

To achieve optimum blocking performance, the base band filter is realized in two separated circuit blocks. The first filter block removes high level blocking signals out of receive band, the second filter block serves for high selectivity of adjacent interferers.

1.1.5 DC-Cancellation and Adjustment of Lower Cut-Off Frequency

The DC offset is removed by a first order high-pass with switchable limit frequency. In the first step the frequency offset of transmitter and receiver is not compensated, therefore the lower band limit is about 10 kHz. In the second step, the receiver frequency is adjusted and the lower limit frequency of the DC-block is set to about 40 kHz and therefore the total bandwidth of pass band is reduced. At the output of the DC block is a switch to initialize the DC-offset in the power-up instant, at the instant of switching, and after appearance of high level interfering signals.

1.2 Digital Controller

The principal function of the digital controller is demodulation, bit synchronization and the detection of the received data protocol, according to the definition of transmitted bits. Furthermore, a first syntax check and plausibility check of detected data is provided. A data protocol received completely is put into a receive buffer, where a micro controller (µC) can read it out via a serial interface.
The receiver can be externally configured with several operation parameters, LNA gain setting, used frequency band, and timing constant for the watch dog timer. The serial interface also allows to configure the digital controller by the µC.
The receiver writes the state information into a status register. This status information can be read out from the µC out of the status register of the receiver.

1.2.1 Microprocessor Clock

The microprocessor clock frequency F_{CLK} is generated by dividing the XTAL frequency F_{XOSC} by 4 if XO-SEL is ´H´ and by dividing the XTAL frequency F_{XOSC} by 6 if XO-SEL is ´L´.

Note: XO-SEL and RF-SEL are internal generated signals from the FB[1:0] bits of the setup information.

1.2.2 ASCell3912 Digital Part Timing

In Figure 2 the timing of a complete receive sequence can be seen. Transmission starts at an arbitrary point in time. First the crystal oscillator is switched on. A minimum time of 5 ms is allowed for the frequency to settle to the final value. Then the receiver executes a wake-up sequence consisting of 6 wake-up bursts. The wake-up bursts are unequally spaced to guarantee interference free detection of an ongoing transmission also in the presence of burst interferers. During a wake-up burst the receiver scans for an active transmission on the air interface. The wake-up sequence is optimized to combat GSM and CT2 type interferers.

After an ongoing transmission has been detected the receiver goes to receiving mode, the WAKE_UP line goes high, and reception of data starts. Depending on the number of interferers present, reception of all data may take up to 3 data blocks. As soon as all data has been detected successfully, the RE_INT pin issues a positive pulse, to indicate the availability of data, and the internal data ready flag (DR) in the ASCell3912 state register is set. The RE_INT line may be used to trigger a interrupt procedure, which is executed at the availability of data. When data is read out by the micro controller the internal data ready flag (DR) in the RX-status register is cleared and it is only set, when a complete data sequence has received again. No further pulse is issued on the RE_INT line, but the micro controller has to poll for new data during an ongoing reception. If transmission stops, the WAKE_UP line goes low and a pulse is issued on the RE_INT line to indicate the termination of transmission at CMT.

In Figure 2 also the timing where the microprocessor clock (µC_CLK) is active is shown. The clock is active with the start of the detection phase of the SC3911. The clock is shut down 16 clock cycles (T_{CAI}) after the falling edge of the second interrupt on the RE_INT pin.

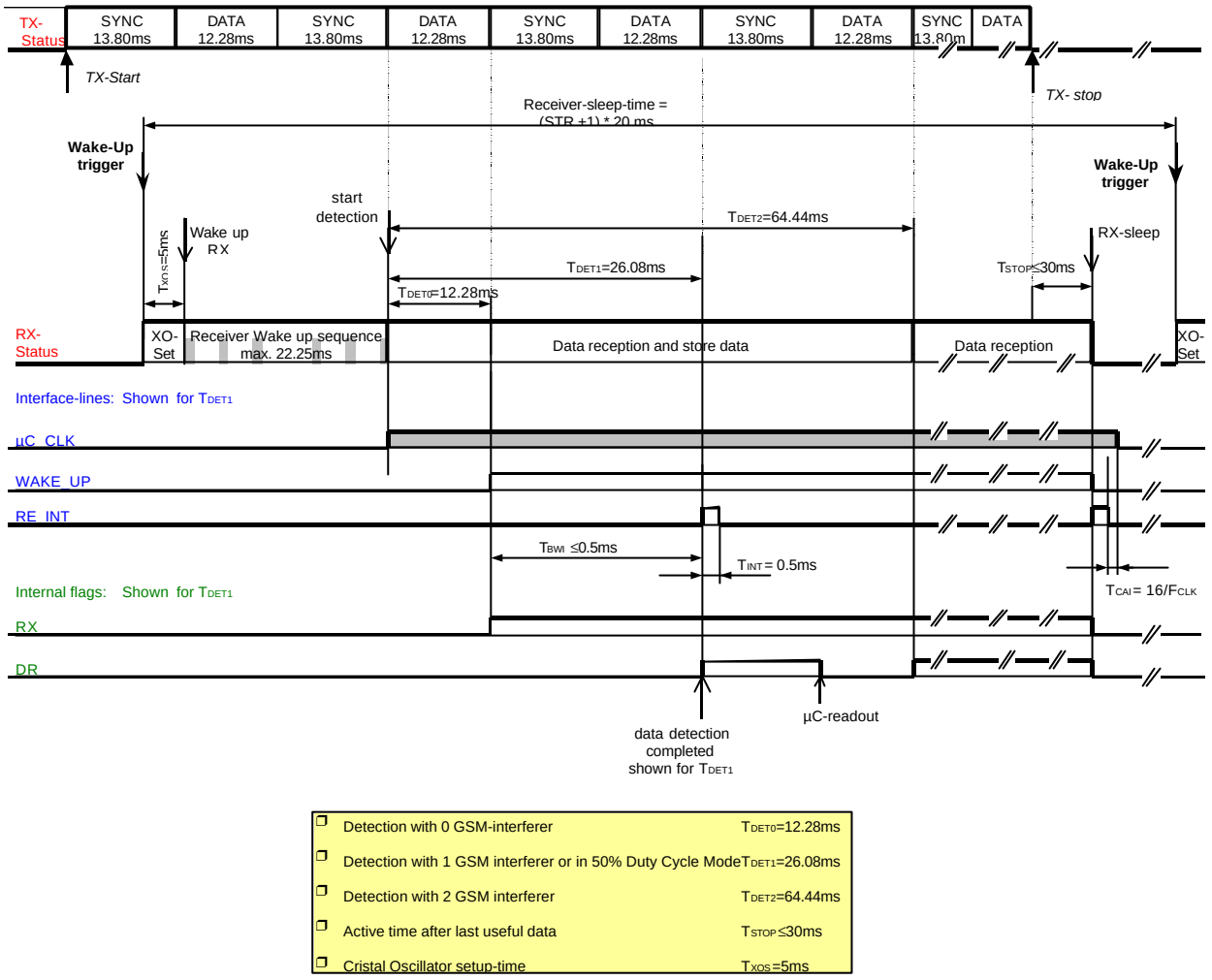


Figure 2: ASCell3912 basic timing.

Note: The Interface timing and the timing of the internal flags are shown in Figure 2 for a detection time of T_{DET1}.

1.2.3 Receiver Configuration

The configuration register can be loaded from a µC via the serial interface. The Table 2 below shows the contents of the configuration register. Bit b0 is the first transmitted bit. The setup contains the LNA set, frequency band and the sleep time interval of the receiver.

bit #	Name	Description	Configuration	Comments
0	LNA	LNA gain switch	L= LNA Gain is high H= LNA Gain is -10dB	default
[1..2]	FB[1:0]	Frequency band select with FB1 is MSB	L, L (FB1, FB0) = 868.3 MHz L, H = 433.92 MHz H, L = 315 MHz H, H = not used	default
[3..8]	STR[5:0]	Sleep time interval set of the receiver, with STR5 is MSB	t_{sleep} = (STR + 1) * 20ms	Note: for STR = 00h the witing period between two consecutive wake-up cycles will be 148 bit.

Table 2: Format of the configuration Register

1.2.4 Receiver Status

Table 3 below shows the format of the state register. Bit b0 is the first which is transmitted by a readout of the µC. The status register contains the information about a successful received date, active receiver and the information about the quality of the received signal.

bit #	Name	Description	Status	Comments
0	DR	Data received a complete message was received	L= no data received H= data received successfully	
1	RX	Receiver is active	L= receiver not active H= data reception in progress	Note: This bit is set by the receiver when 6 bytes of a packet are correct. This bit in the status register is neces-sary for the comfort-orientated functions of the central locking functions.
[2..3]	RQ[1:0]	Signal quality indicates how many data packets are necessary for a com-plete message	L, L (RQ1, RQ0) = 1 packet L, H = 2 packets H, L = 3 packets H, H =4 packets	

Table 3: Format of the status register.

1.2.5 µC Interface

The ASCell3912 contains a direct interface to a micro controller (µC). The µC interface of the ASCell3912 consist of the following five pins:

”Transmit/Received data input/output” (DATA). A bi-directional serial data line, with states ”H” (recessive, or weak pull-up) and ”L” (dominant).

“Active ”H” transmit data enable” (D_EN)

”Transmit data clock input” (D_CLK).

”Active ”H” µC interrupt output ” (RE_INT).

”Active ”H” µC wakeup output ” (µC_WAKEUP).

”µC clock output ” (µC_CLK).

1.2.5.1 Instruction Set

The following table shows the instruction set of the interface. The first two bits are the operation code, which determine the direction of the data transfer and which data is transferred.

Operation code	Instruction or Data											Comment
0	1	LNA	FB1	FB0	STR5	STR4	STR3	STR2	STR1	STR0		Write ASCell3912 setup
0	0	Z	LNA	FB1	FB0	STR5	STR4	STR3	STR2	STR1	STR0	Read ASCell3912 setup
1	0	Z	DR	RX	RQ1	RQ0						Read ASCell3912-State
1	1	Z	B0-b0								B15-b7	Read ASCell3912-Data

Table 4: Overview of the instruction set.

1.2.6 Timing Diagrams

The following Figure 3 shows the timing for the write operation into the configuration register. First the opcode is transmitted and it is followed by 9 instruction bits.

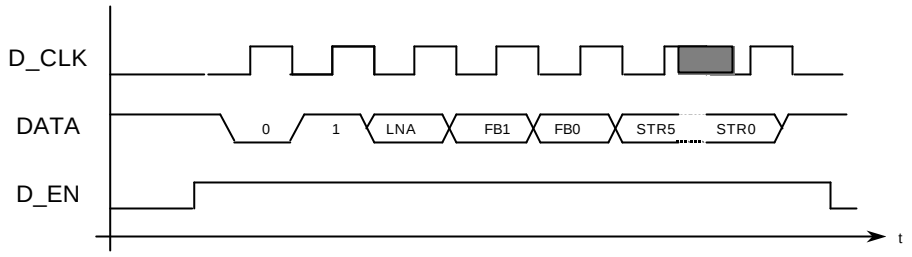


Figure 3: Write timing for the configuration register..

The following Figure 4 shows the timing of a read operation from the status register. After writing the operation code to the ASCell3912, the ASCell3912 stays in high impedance state for one more clock cycle and starts transmission of the selected bit sequence after that period.

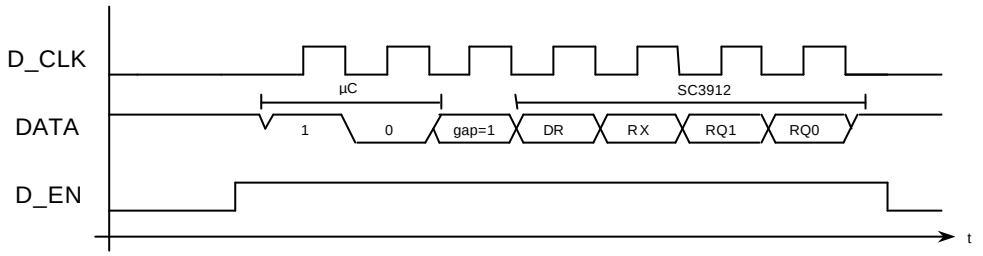


Figure 4: Read timing for status register.

In the following Figure 5 shows read out of the received data. In the example `Bx-bz` stands for bit ´z´ of Byte ´y´, so B7-b5 depicts bit 5 of byte 7.

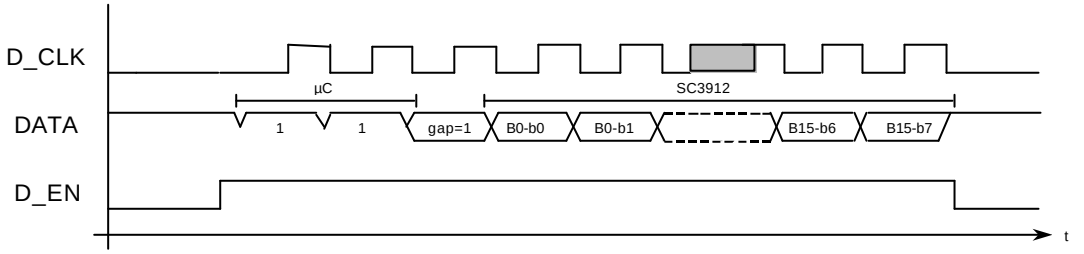


Figure 5: Read out timing for received data (16 Bytes).

1.2.7 Interrupt and Wake-Up Pins

To provide the micro controller with time-critical information the receive/end transmission interrupt (RE_INT) line is used. Figure 2 shows the timing of the RE_INT and WAKE_UP signals during the reception. A high pulse is issued on this line, when one of the both conditions appear:

- The reception of data is completed for the first time after a receiver wake-up.
- The transmission of data has stopped. This interrupt is necessary status oriented CMT for comfort orientated central locking functions (like window closing).

To distinguish between the two interrupt sources, the WAKE_UP line is used, as listed in the following table.

RE_INT	WAKE_UP	Interrupt source
0→1	1	Message received completely
0→1	0	Transmission stopped

Table 5: Interrupt sources and their meaning.

2 Electrical Characteristics

Absolute Maximum Ratings (non operating)

Symbol	Parameter	Min	Max	Units	Note
VDD; AVDD	Positive supply voltage	-0.5	6	V	
GND; AGND	Negative supply voltage	0	0	V	
Vin	Voltage at every input pin	Gnd-0.5	VCC+0.5	V	
Iin	Input current into any pin except supply pins	-10	10	mA	
ESD	Electrostatic discharge		1k	V	1) 3)
Tstg	Storage temperature	-55	125	°C	
Tlead	Lead temperature		260	°C	2)

1) Test according to MIL STD 883C, Method 3015.7: HBM: R=1.5 kΩ, C=100 pF, 5 positive pulses per pin against supply pins, 5 negative pulses per pin against supply pins [C2].
2) 260 °C for 10 sec (Reflow and Wave Soldering), 360 °C for 3 sec (Manual soldering).
3) All pins, pins XTAL+,XTAL-, RF+,RF-,LC+ and LC- have 500 V ESD protection

Operating Conditions

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
VDD=AVDD	Positive supply voltage		2.7		5.5	V
GND=AGND	Negative supply voltage		0	0	0	V
TA	Operating temperature		-40		+85	°C.
IP_{run}	Supply current into VDDA and VDDD pin	Everything on			10	mA
IP_{idle}	Average supply current in idle mode.				1.2	mA
IP_{sleep}	Average supply current in sleep mode.				0,5	µA
$P_{in,max}$	Maximum input power level	Above this level circuit could be destroyed		30		dBm

2.3 Receiver Operation

TA = 23 °C, VDD, AVDD = 3.6 V, unless specified otherwise. Devive functional for TA= -40 to +85 °C.

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
F_C	Carrier Frequency	Depends on different external crystals.		315.000 433.920 868.300		MHz MHz MHz
R_{in}	Input impedance	Capacitive part t.b.d.		200~ 400		Ω
? F	Nominal FSK frequency deviation	315, 433.92, 868.3MHz	61		69	kHz
F_{xosc}	Crystal oscillator (XOSC) frequency	315,000 MHz: max +/- 50ppm 433.920 MHz: max +/- 50ppm 868.300 MHz: max +/-25ppm		19,6875 13.5600 13.5672		MHz MHz MHz
TF_{xosc}	Crystal oscillator (XOSC) frequency tolerance	315,000 MHz: (-40~+85 °C), 433.920 MHz: (-40~+85 °C), 868.300 MHz: (-40~+85 °C).			50 50 25	ppm ppm ppm
$D_{R,gross}$	Gross Data Rate	Including protocol.		18.235		kbps
RF_{Sens} [1)]	Receiver sensitivity	-10 °C<TA<+70 °C	-96	-100		dBm
RF_{SensT}	Temperature sensitivity reduction	-40<TA<-10 °C. or +70>TA>+85 °C.			4	dB
$RF_{Sens}F_{offim}$	Receiver sensitivity reduction caused by frequency offset	@maximum receiver sensitivity reduction @ 44 kHz offset			7	dB
$RF_{SensLNA}$	Sensitivity reduction caused by LNA gain switching			10		dB
BI_{200KHz} [2)]	Blocking immunity 200 kHz – 1 MHz	Without external filter.	0			dB
BI_{1MHz} [2)]	Blocking immunity 1-10 MHz	Without external filter	21			dB
BI_{10MHz} [2)]	Blocking immunity @ >10 MHz	Without external filter	63			dB
P_{LOfeed}	LO @ F_C power available at LC+ and LC- nodes				-28	dBm

1) Standard Receive Quality (SRQ): Message reception successfully finished after <80 ms in 80% of all transmission trails.

2) CW blocking signal relative to applied useful signal with –94dBm power level and SRQ. Measured without frequency offset and at +25 °C

Receiver Timing

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
T_{Dni}	Time to received FSK data	Configured for fast response (receiver sleep time = 0)	27		80	ms
T_{Dwi}	Time to received FSK data	Using low idle duty cycle the (receiver sleep time >0)	40		92	ms
T_{stop}	RX switch off time	Timeout for comfort functions		30		ms

2.5 Digital Pin Characteristics

T_{AMB} = 23 °C, VDD = 3.6 V, unless specified otherwise. GND is the 0 V reference.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
µC_CLK (µC clock output)						
VOH	High level output voltage	IOH =-1 mA	VDD-0.5	-		V
VOL	Low level output voltage	IOL =1 mA		-	0.3	V
tr	Rise time	CLoad = 10 pF		20		ns
td	Fall time	CLoad = 10 pF		20		ns
jcc	Cycle to cycle jitter				+/-5	%
DATA(serial data input), D_EN (serial data enable input), D_CLK (serial data clock input)						
VIH	High level input voltage		VDD-0.5	-		V
VIL	Low level input voltage			-	0.3	V
IIH	High level input current	VIH= VDD			1	µA
IIL	Low level input current	VIL =0 V	-1			µA
F_{D_CLK}	D_CLK frequency		3			kHz
RE_INT (interrupt output); WAKEUP (µC wakeup output)						
VOH	High level output voltage	IOH = -1mA	VDD-0.5	-		V
VOL	Low level output voltage	IOL = 1mA		-	0.3	V

3 Pin-out Information

Note: pin numbers have arbitrary ordering and numbering - will be defined during design

Pin	Name	Type	Description
1	RF+	I	LNA input
2	RF-	I	LNA input
3	LC+	I/O	LNA tank
4	LC-	I/O	LNA tank
5	XTAL+	I	XTAL oscillator input
6	XTAL-	O	XTAL oscillator output
7	AVDD	P	Analog positive supply
8	AGND	P	Analog negative supply
9	GMC	I/O	Base-Band Low Pass frequency set
10	RFGND	I	RF GND
11	DGND	P	Digital negative supply
12	TEST1	I/O	pin for test purposes
13	TEST2	I/O	pin for test purposes
14	uC_CLK	O	Clock output for micro controller
15	RE_INT	O	Interrupt at first received data block and receive end
16	WAKEUP	O	Micro controller wake up; high during ongoing reception

Pin	Name	Type	Description
17	D_EN	O	Enable data bus
18	D_CLK	I	Clock for serial interface
19	DATA	I/O	Data Input / Output for serial interface
20	DVDD	P	Digital positive supply

4 Application Schematic

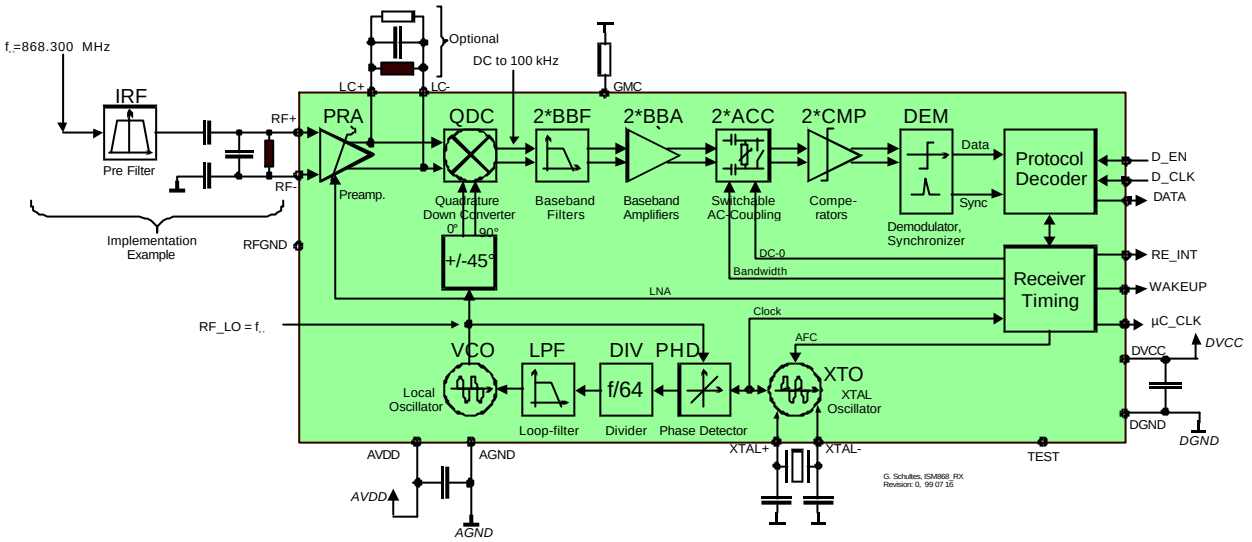


Figure 6: Basic application schematic of the ASCell3912.

5 Package Information

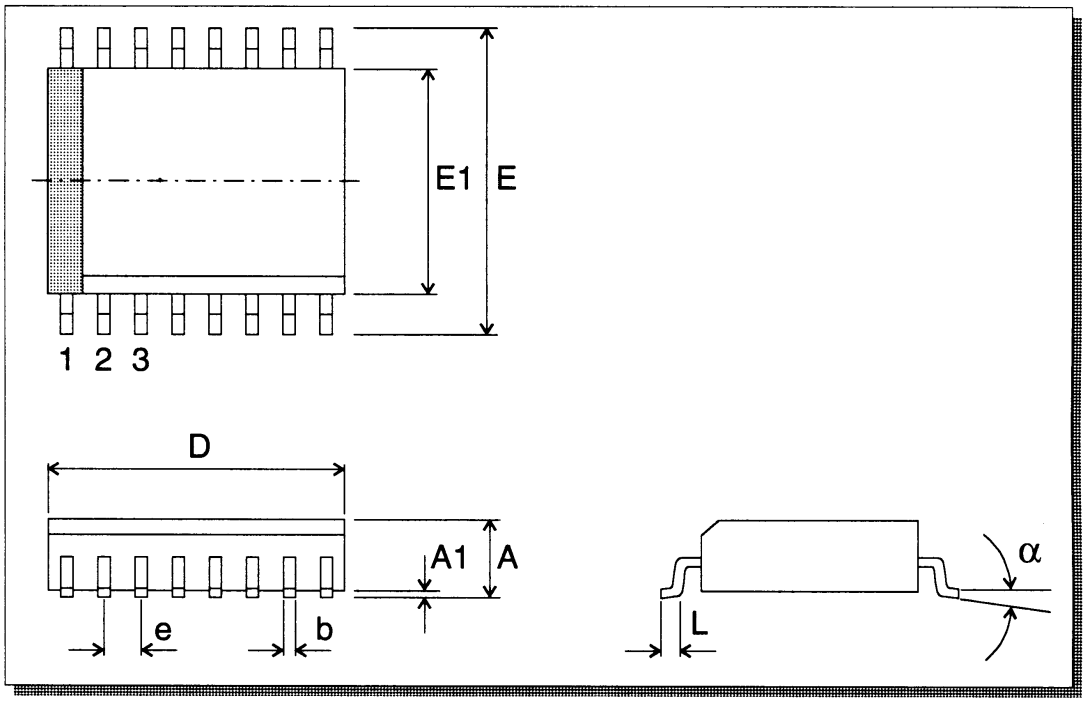


Figure 7: Physical dimensions of TSSOP-20.

Symbol	Common Dimensions		
	Minimal (mm/mil)	**Nominal (mm/mil)**	**Maximal (mm/mil)**
A	-	-	1.10/0.0433
A1	0.05/0.002	0.10/0.004	0.15/0.006
b	0.19/0.0075	-	0.30/0.0118
D			
e	0.65 BSC		
E	6.25/0.246	6.40/0.252	6.50/0.256
E1	4.30/0.169	4.40/0.173	4.50/0.177
L	0.50/0.020	0.60/0.024	0.70/0.028
?	0°	4°	8°

ASCell's are functional and in-spec circuits, which are usually available as samples with documentation and demoboard. However they are intentionally to be used as a basis for ASIC derivatives. If an ASCell fits into a customer's application as it is, it will be immediately qualified and transfered to an ASSP to be ordered as a regular AS product.