ICL7115

# ICL7115
## 14-Bit High-Speed CMOS μP-Compatible A/D Converter

INTERSIL

T-51-10-90

### GENERAL DESCRIPTION

The ICL7115 is the first monolithic 14-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 13-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard $\overline{\text{WRite}}$ and $\overline{\text{ReaD}}$ cycle timing and control signals, combined with $\overline{\text{Chip Select}}$ and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8 and 16-bit systems.

The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +5V input with a −5V reference or 0V to −5V input with a +5V reference.

### FEATURES

- **14-Bit Resolution (LSB = 305μV)**
- **No Missing Codes**
- **Microprocessor Compatible Byte-Organized Buffered Outputs**
- **Fast Conversion (40μs)**
- **Auto-Zeroed Comparator for Low Offset Voltage**
- **Low Linearity and Gain Tempco (1.5ppm/°C, 5ppm/°C)**
- **Low Power Consumption (60mW)**
- **No Gain or Offset Adjustment Necessary**
- **Provides 3% Useable Overrange**
- **FORCE/SENSE and Separate Digital and Analog Ground Pins for Increased System Accuracy**

### ORDERING INFORMATION

| Part Number | Resolution with No Missing Codes | Temp. Range | Package |
|---|---|---|---|
| ICL7115JCDL | 12 Bits | 0°C to +70°C | 40 Pin Ceramic |
| ICL7115KCDL | 13 Bits | 0°C to +70°C | 40 Pin Ceramic |
| ICL7115JIDL | 12 Bits | −25°C to +85°C | 40 Pin Ceramic |
| ICL7115KIDL | 13 Bits | −25°C to +85°C | 40 Pin Ceramic |
| ICL7115JMDL | 12 Bits | −55°C to +125°C | 40 Pin Ceramic |
| ICL7115KMDL | 13 Bits | −55°C to +125°C | 40 Pin Ceramic |
| ICL7115JMLL | 12 Bits | −55°C to +125°C | 40 Pin LCC |
| ICL7115KMLL | 13 Bits | −55°C to +125°C | 40 Pin LCC |



301659-003

*NOTE: All typical values have been characterized but are not tested.*

# ICL7115

INTERSIL

T-51-10-90



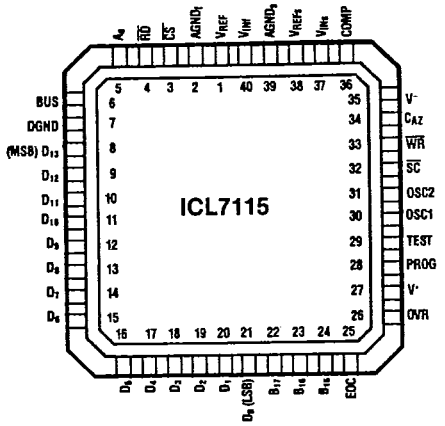
## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage $V^+$ to DGND ..... −0.3V to +6.5V
Supply Voltage $V^-$ to DGND ..... +0.3V to −6.5V
$V_{REFS}$, $V_{REFf}$, $V_{INS}$, $V_{INf}$ to DGND ..... +25V to −25V
$AGND_S$, $AGND_f$ to DGND ..... +1V to −1V
Current in FORCE and SENSE Lines ..... 25mA
Digital I/O Pin Voltages ..... −0.3V to $V^+$ +0.3V
PROG to DGND Voltage ..... $V^-$ to $V^+$ +0.3V

Operating Temperature Range
ICL7115XCXX ..... 0°C to +70°C
ICL7115XIXX ..... −25°C to +85°C
ICL7115XMXX ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation ..... 500mW
derate above 70°C @ 100mW/°C
Lead Temperature (Soldering, 10sec) ..... 300°C

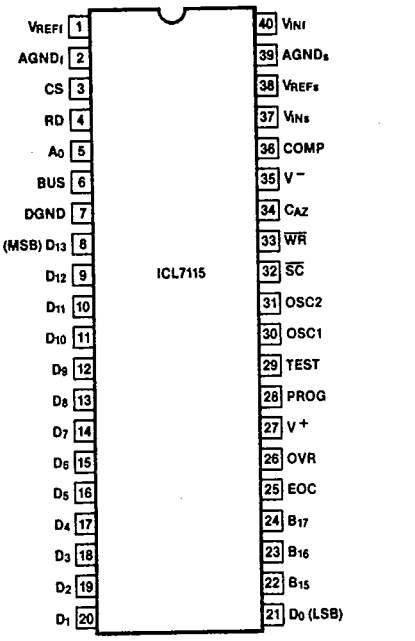
**NOTE 1:** All voltages with respect to DGND, unless otherwise noted.

**NOTE:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*




0337-17

(Outline DWG LL)




0337-1

(Outline DWG DL)

**Figure 1: Pin Configuration**



*NOTE: All typical values have been characterized but are not tested.*

# ICL7115

INTERSIL

T-51-10-90

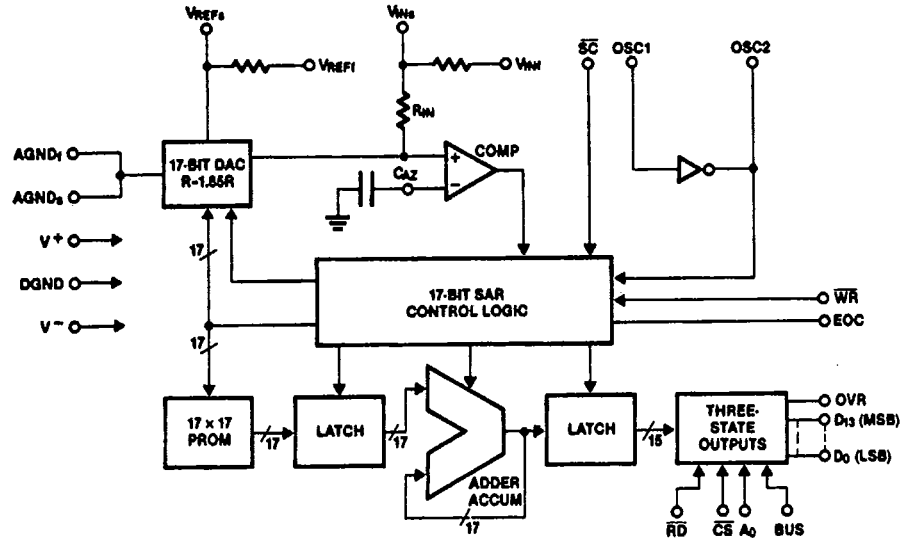



**Figure 2: ICL7115 Functional Diagram**



*NOTE: All typical values have been characterized but are not tested.*

# ICL7115

INTERSIL

T-51-10-90



## ELECTRICAL CHARACTERISTICS

**DC ELECTRICAL CHARACTERISTICS** $V^+ = +5.0V$, $V^- = -5.0V$, $V_{REFs} = -5.0V$, $T_A = +25°C$, $f_{CLK} = 500kHz$, $\overline{SC} = V_{IH}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | Resolution | $\overline{SC} = V_{IH}$ | | 14 | | | Bits |
| | | $\overline{SC} = V_{IL}$ | | 12 | | | |
| $I_{LE}$ | Integral Linearity Error | Note 1 | J | | | ±0.018 | %FSR |
| | | | K | | | ±0.012 | |
| $T_{C(ILE)}$ | Temperature Coefficient of $I_{LE}$ | TA = Operating Range | | | 1 | 1.5 | ppm/°C |
| $RES_{(NMC)}$ | Min Resolution with No Missing Codes | $T_A = 25°C$ | J | 12 | | | Bits |
| | | | K | 13 | | | |
| | | $T_A$ = Operating Range (Note 2) | J | 11 | | | |
| | | | K | 12 | | | |
| FSE | Full Scale Calibration Error (Adjustable to Zero) | | J | | | ±0.1 | %FSR |
| | | | K | | | ±0.08 | |
| $T_{C(FSE)}$ | Temperature Coefficient of FSE | $T_A$ = Operating Range | | | 2 | 5 | ppm/°C |
| ZE | Zero Error | Notes 1,2 | | | | ±1 | LSB |
| $T_{C(ZE)}$ | Temperature Coefficient of ZE | $T_A$ = Operating Range | | | | 1 | ppm/°C |
| PSRR | Power Supply Rejection Ratio | $T_A = 25°C$ | | | ±½ | ±1 | LSB |
| | | $T_A$ = Operating Range | | | | ±2 | |
| $V_{IN}$ | Analog Input Range ($V_{INs}$, $V_{REFs}$) | | | 0 to +5 | | | V |
| $R_{IN}$ | Input Resistance ($V_{INs}$, $V_{REFs}$) | Note 3 | | 4 | | 9 | kΩ |
| $T_C(R_{IN})$ | | $T_A$ = Operating Range | | | −300 | | ppm/°C |
| $I_{SUPPLY}$ | Supply Current, I+, I− | $T_A = 25°C$ | | | 2 | 4 | mA |
| | | $T_A$ = Operating Range | | | | 6 | |
| $V_{SUPPLY}$ | Supply Voltage Range | Functional Operation Only | | ±4.5 | | ±6.0 | V |
| $V_{IL}$ | Low State Input Voltage | Operating Temperature Range | | | | 0.8 | V |
| $V_{IH}$ | High State Input Voltage | Operating Temperature Range | | 2.4 | | | V |
| $I_{LIH}$ | Logic Input Current | $0 < V_{IN} > V+$ | | | 1 | 10 | µA |
| $V_{OL}$ | Low State Output Voltage | $I_{OUT} = 1.6mA$ Operating Temperature Range | | | | 0.4 | V |
| $V_{OH}$ | High State Output Voltage | $I_{OUT} = -200µA$ Operating Temperature Range | | 2.8 | | | V |
| $I_{OX}$ | Three-State Output Current | $0 < V_{OUT} > V_+$ | | | 1 | | µA |
| $C_{IN}$ | Logic Input Capacitance | | | | 15 | | pF |
| $C_{OUT}$ | Logic Output Capacitance | Three-State | | | 15 | | |

**NOTES:** 1. Full-scale range (FSR) is 5V (reference adjusted).
2. Assume all leads soldered or welded to printed circuit board.
3. Assume all leads soldered or welded to printed circuit board.



*NOTE: All typical values have been characterized but are not tested.*

ICL7115

# ICL7115

INTERSIL

T-51-10-90

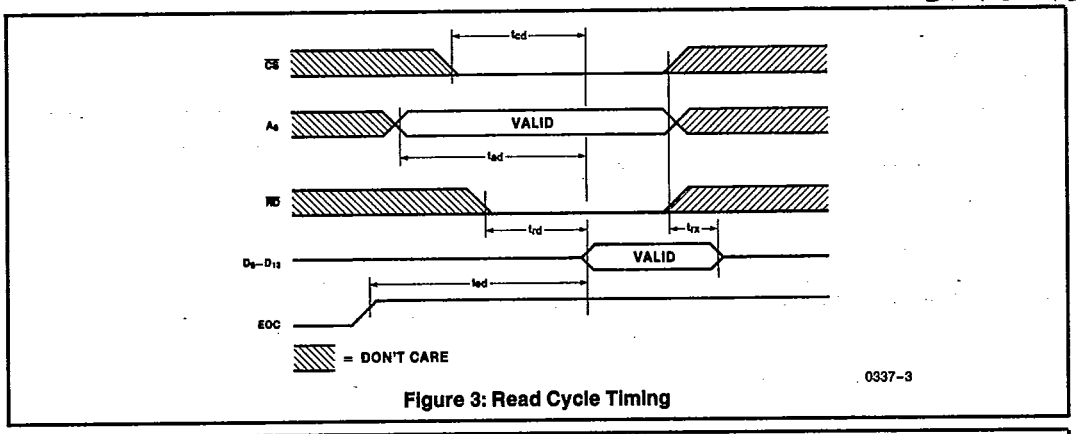



**Figure 3: Read Cycle Timing**

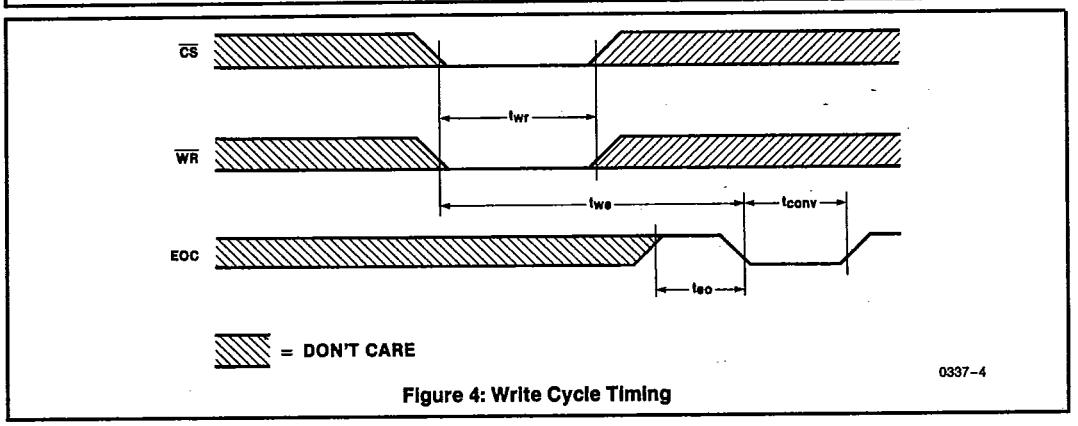



**Figure 4: Write Cycle Timing**

## AC ELECTRICAL CHARACTERISTICS

$V^+ = +5.0V$, $V^- = -5.0V$, $T_A = +25°C$, $f_{clk} = 500kHz$ unless otherwise noted. Data derived from extensive characterization testing. Parameters are not 100% production tested.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **READ CYCLE TIMING** | | | | | | |
| $t_{cd}$ | Prop. Delay $\overline{CS}$ to Data | $\overline{RD}$ Low, $A_0$ Valid | | | 200 | ns |
| $t_{ad}$ | Prop. Delay $A_0$ to Data | $\overline{CS}$ Low, $\overline{RD}$ Low | | | 200 | |
| $t_{rd}$ | Prop. Delay $\overline{RD}$ to Data | $\overline{CS}$ Low, $A_0$ Valid | | | 200 | |
| $t_{rx}$ | Prop. Delay Data to Three State | | | | 100 | |
| $t_{ed}$ | Prop. Delay EOC High to Data | | | | 200 | |
| **WRITE CYCLE TIMING** | | | | | | |
| $t_{wr}$ | $\overline{WR}$ Low Time | | 100 | | | ns |
| $t_{we}$ | Prop. Delay $\overline{WR}$ Low to EOC Low | Wait Mode | 1 | | 2 | 1/fclk |
| $t_{eo}$ | EOC High Time | Free-Run Mode | 0.5 | | 1.5 | |
| $t_{conv}$ | Conversion Time | $\overline{SC} = V_{IH}$ | | | 20 | |
| | | $\overline{SC} = V_{IL}$ | | | 18 | |



*NOTE: All typical values have been characterized but are not tested.*

# ICL7115

## TABLE 1: PIN DESCRIPTIONS

| PIN | NAME | FUNCTION | |
|---|---|---|---|
| 1 | $V_{REFf}$ | FORCE line for reference input. | |
| 2 | $AGND_f$ | FORCE input for analog ground | |
| 3 | $\overline{CS}$ | Chip Select enables reading and writing (active low) | |
| 4 | $\overline{RD}$ | $\overline{ReaD}$ (active low) | |
| 5 | $A_0$ | Byte select (low = $D_0 - D_7$, high = $D_8 - D_{13}$, OVR) | |
| 6 | BUS | Bus select (low = outputs enabled by $A_0$, high = all outputs enabled together) | |
| 7 | DGND | Digital GrouND return | |
| 8 | $D_{13}$ | Bit 13 (most significant) | High Byte |
| 9 | $D_{12}$ | Bit 12 | |
| 10 | $D_{11}$ | Bit 11 | |
| 11 | $D_{10}$ | Bit 10 | |
| 12 | $D_9$ | Bit 9 — Output | |
| 13 | $D_8$ | Bit 8 — Data | |
| 14 | $D_7$ | Bit 7 — Bits | Low Byte |
| 15 | $D_6$ | Bit 6 — (High = True) | |
| 16 | $D_5$ | Bit 5 | |
| 17 | $D_4$ | Bit 4 | |
| 18 | $D_3$ | Bit 3 | |
| 19 | $D_2$ | Bit 2 | |
| 20 | $D_1$ | Bit 1 | |
| 21 | $D_0$ | Bit 0 (least significant) | |
| 22 | $B_{15}$ | Used for programming only (leave open) | |
| 23 | $B_{16}$ | | |
| 24 | $B_{17}$ | | |
| 25 | EOC | End Of Conversion flag (low = busy, high = conversion complete) | |
| 26 | OVR | OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte) | |
| 27 | V+ | Positive power supply input | |
| 28 | PROG | Used for programming only. Tie to V+ for normal operation | |
| 29 | TEST | Used for programming only. Tie to V+ for normal operation | |
| 30 | OSC1 | Oscillator inverter input | |
| 31 | OSC2 | Oscillator inverter output | |
| 32 | $\overline{SC}$ | Short cycle input (high = 14-bit, low = 12-bit operation) | |
| 33 | $\overline{WR}$ | $\overline{WR}$ite pulse input (low starts new conversion) | |
| 34 | $C_{AZ}$ | Auto-zero capacitor connection | |
| 35 | V− | Negative power supply input | |
| 36 | COMP | Used in test, tie to V− | |
| 37 | $V_{INs}$ | SENSE line for input voltage | |
| 38 | $V_{REFs}$ | SENSE line for reference input | |
| 39 | $AGND_s$ | SENSE line for analog ground | |
| 40 | $V_{INf}$ | FORCE line for input voltage | |

## TABLE 2: I/O CONTROL

| $\overline{CS}$ | $\overline{WR}$ | $\overline{RD}$ | $A_0$ | BUS | FUNCTION |
|---|---|---|---|---|---|
| 0 | 0 | x | x | x | Initiates a Conversion |
| 1 | x | x | x | x | Disables all Chip Commands |
| 0 | x | 0 | 0 | 0 | Low Byte is Enabled |
| 0 | x | 0 | 1 | 0 | High Byte is Enabled |
| 0 | x | 0 | x | 1 | Low and High Bytes Enabled Together |
| x | x | 1 | x | x | Disables Outputs (High-Impedance) |

## TABLE 3: TRANSFER FUNCTION

| INPUT VOLTAGE | EXPECTED OUTPUT CODE | | | |
|---|---|---|---|---|
| $V_{REF} = -5.0V$ | OVR | MSB | | LSB |
| 0 | 0 | 0 | 000000000000 | 0 |
| +0.0003 | 0 | 0 | 000000000000 | 1 |
| +0.150 | 0 | 0 | 000011110101 | 1 |
| +2.4997 | 0 | 0 | 111111111111 | 1 |
| +2.500 | 0 | 1 | 000000000000 | 0 |
| +4.9994 | 0 | 1 | 111111111111 | 0 |
| +4.9997 | 0 | 1 | 111111111111 | 1 |
| +5.000 | 1 | 0 | 000000000000 | 0 |
| +5.0003 | 1 | 0 | 000000000000 | 1 |
| +5.150 | 1 | 0 | 000011110101 | 1 |



*NOTE: All typical values have been characterized but are not tested.*

# ICL7115

INTERSIL

T-51-10-90

## DETAILED DESCRIPTION

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 2 shows the functional diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB ($B_{16}$) and the MSB-4 bit ($B_{12}$). The sequence continues for each bit pair, $B_x$ and $B_{x-4}$, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion. When the Short Cycle ($\overline{SC}$) input is low, 18 clock cycles are required to complete a 12-bit conversion.

The overflow output of the 17-bit full-adder is also the OVerRange (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

## OPTIMIZING SYSTEM PERFORMANCE

The FORCE and SENSE inputs for $V_{IN}$ and $V_{REF}$ are also shown driven by external op-amps. This technique eliminates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than 300mΩ of total series resistance, the result can be a voltage error equivalent to 1LSB. If no op-amps are used for $V_{IN}$ and $V_{REF}$, connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the $V_{IN}$ and $V_{REF}$ pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

When using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115 as shown in Figures 5 and 6. In Figure 5 the FORCE line is the only point that is connected to system analog ground. In Figure 6, the op-amp $A_3$ forces the voltage at AGND to be equal to analog system ground. The addition of this op-amp overcomes the main deficiency of the arrangement in Figure 5: the $V_{IN}$ and $V_{REF}$ sources are not referenced to true analog system ground.

The clamp diodes in Figure 6 are required because spurious op-amp output on AGNDf during power-on can exceed the absolute max rating of ±1.0V between AGDf and DGND. The two inverse-parallel diodes clamp the voltage between AGNDs and DGND to ±0.7V.

## INPUT WARNING

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7115 until the ±5V power supplies have stabilized.

## INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and bus select inputs ($A_0$ and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and $A_0$ lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a $\overline{WR}$ pulse (pin 33) when $\overline{CS}$ (pin 3) is low. Data is enabled on the bus when the chip is selected and $\overline{RD}$ (pin 4) is low.

Figure 7 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the $\overline{WR}$ input to the ICL7115 after the I/O or memory-mapped address decoder has brought the $\overline{CS}$ input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on $A_0$ enables the LSBs and a high level enables the MSBs.



*NOTE: All typical values have been characterized but are not tested.*

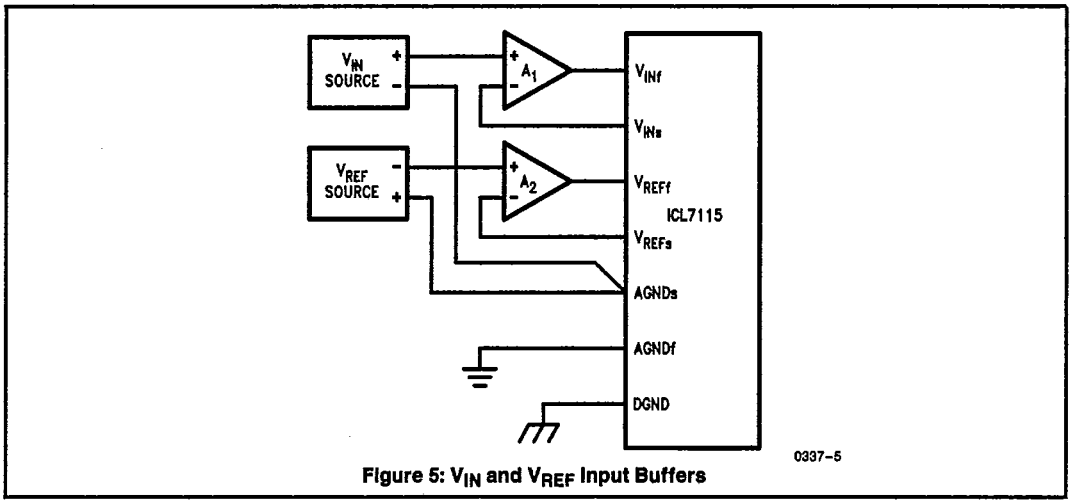



**Figure 5: $V_{IN}$ and $V_{REF}$ Input Buffers**

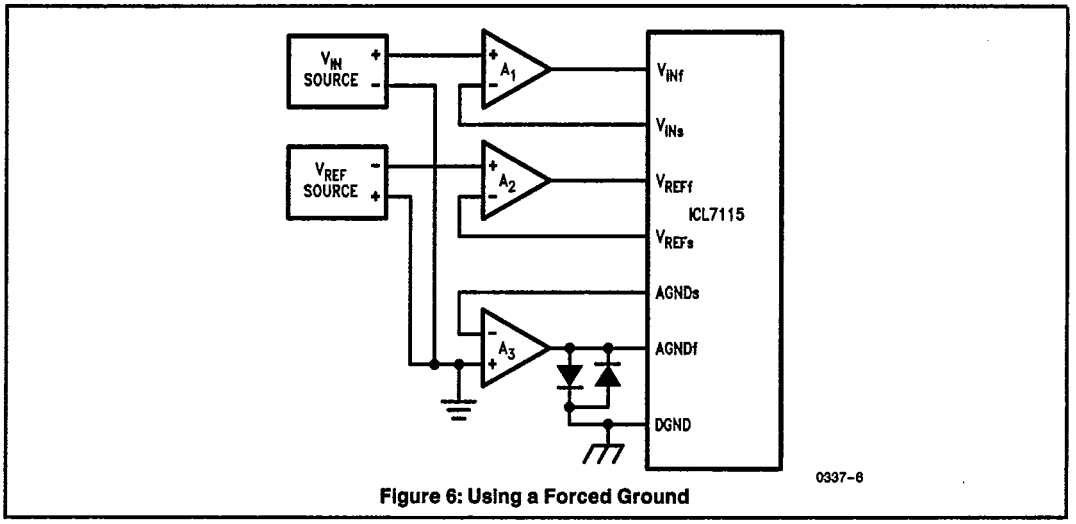



**Figure 6: Using a Forced Ground**

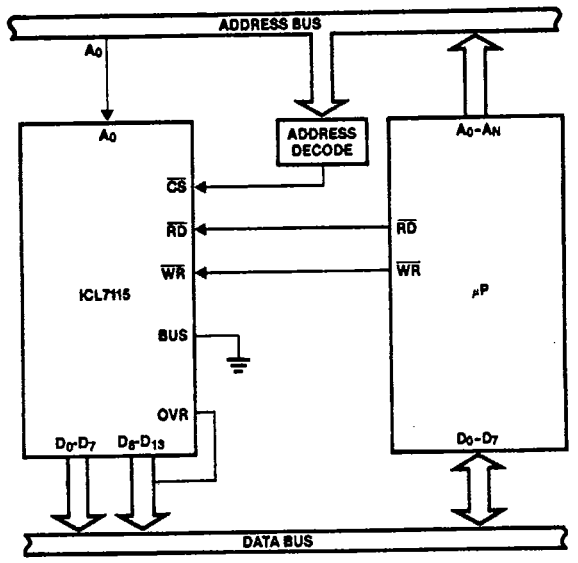


*NOTE: All typical values have been characterized but are not tested.*

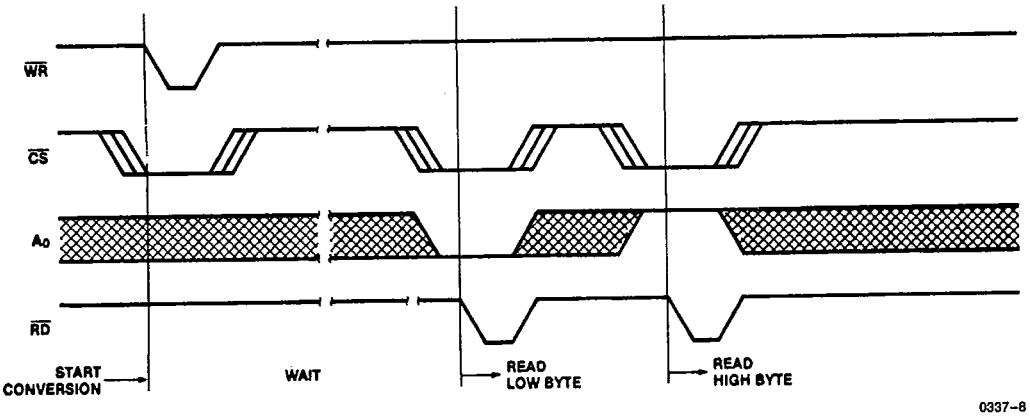
# ICL7115

INTERSIL

T-51-10-90




0337-7




0337-8

Figure 7: "Start and Wait" Operation



*NOTE: All typical values have been characterized but are not tested.*

# ICL7115



By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 8). In this mode, the $A_0$ and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the $\overline{WR}$ line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 9. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 9.

## APPLICATIONS

Figure 11 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of +5V to −5V is the result of using the current through $R_2$ to force a ½ scale offset on the input amplifier ($A_2$). The output of $A_2$ swings from 0V to −5V. The overall gain of the A/D is varied by adjusting the 100kΩ trim resistor, $R_5$. Since the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/°C and stable external resistors are used.

In Figure 11, note that the 0.22μF auto-zero capacitor is connected directly between the $C_{AZ}$ pin and analog ground SENSE. $A_3$ forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground. It is important to note that since the 7115's DAC current flows in $A_1$, $A_2$ and $A_3$ these amplifiers should be wideband (GBW>20MHz) types to minimize errors.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for a conversion time of 40μs. Output data is controlled by the BUS and $A_0$ inputs. Here they are set for 8-bit bus operation with BUS grounded and $A_0$ under the control of the address decode section of the external system.

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 12 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 11, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of $A_1$. A flip-flop in $IC_3$ sets $IC_2$'s Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from $IC_1$, $IC_2$, and $A_1$. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

The ICL7115 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}} \text{ for 14-bit operation}$$

and

$$f_{CLK} = \frac{18}{t_{conv}} \text{ for 12-bit operation}$$



*NOTE: All typical values have been characterized but are not tested.*

# ICL7115

INTERSIL

T-51-10-90

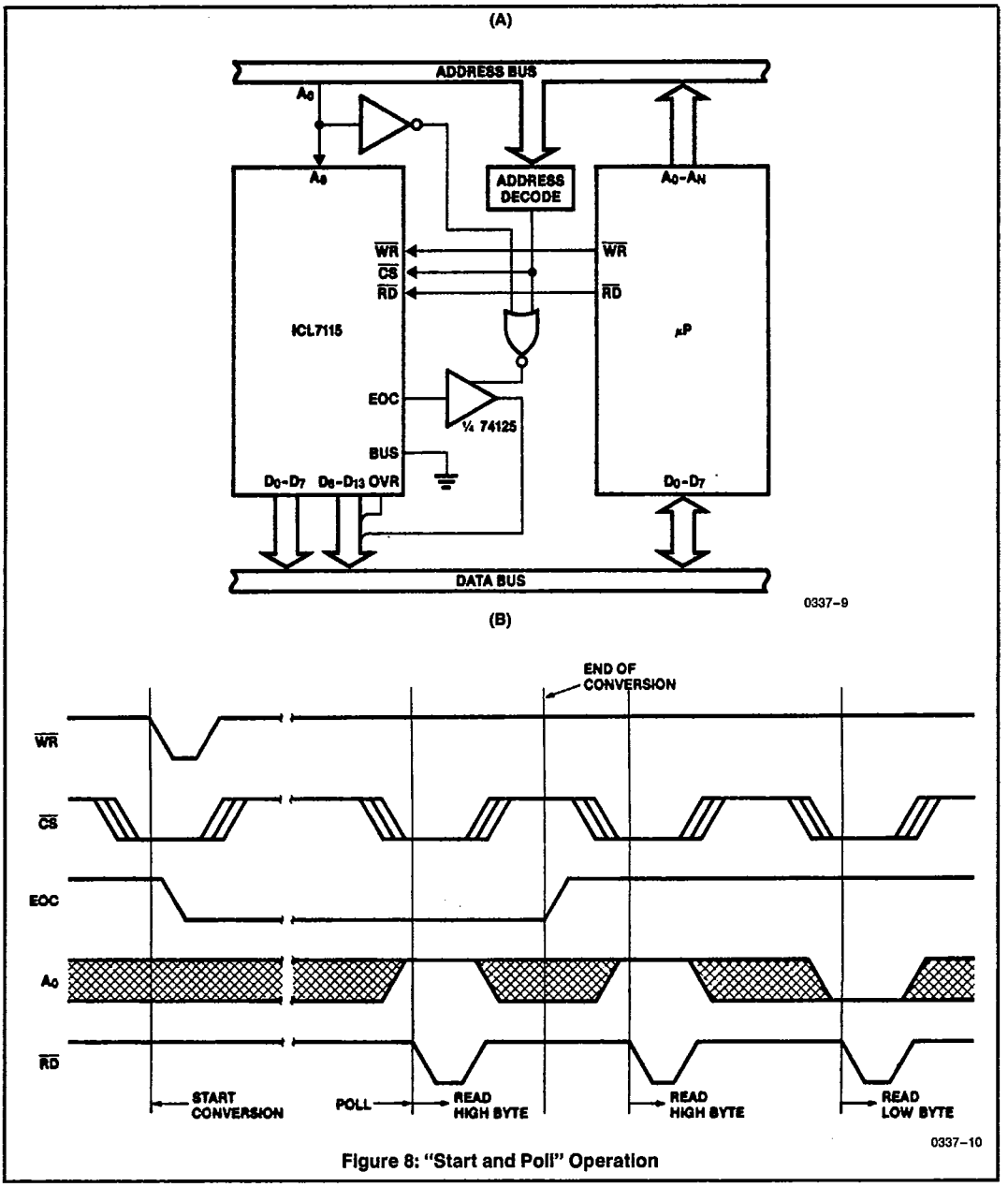
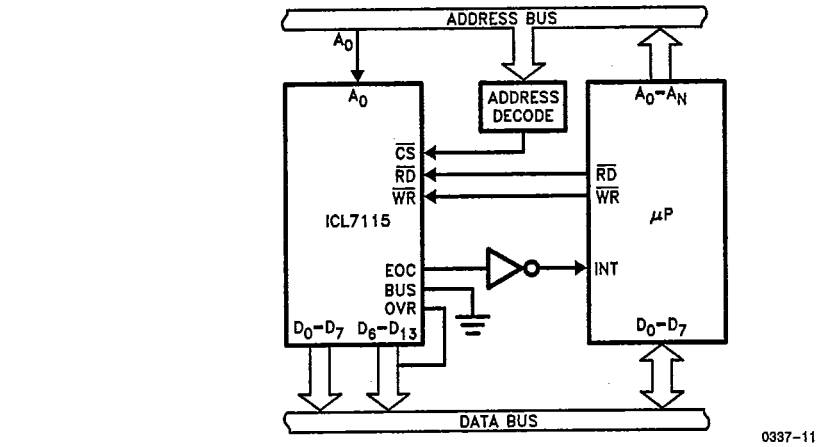


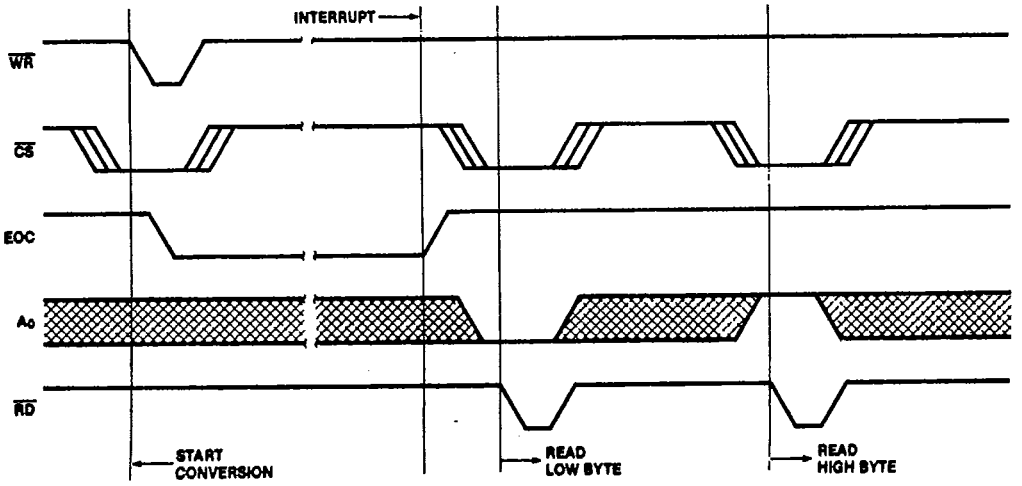

**Figure 8: "Start and Poll" Operation**



*NOTE: All typical values have been characterized but are not tested.*




0337-11




0337-12

**Figure 9: Using EOC as an Interrupt**

3



*NOTE: All typical values have been characterized but are not tested.*

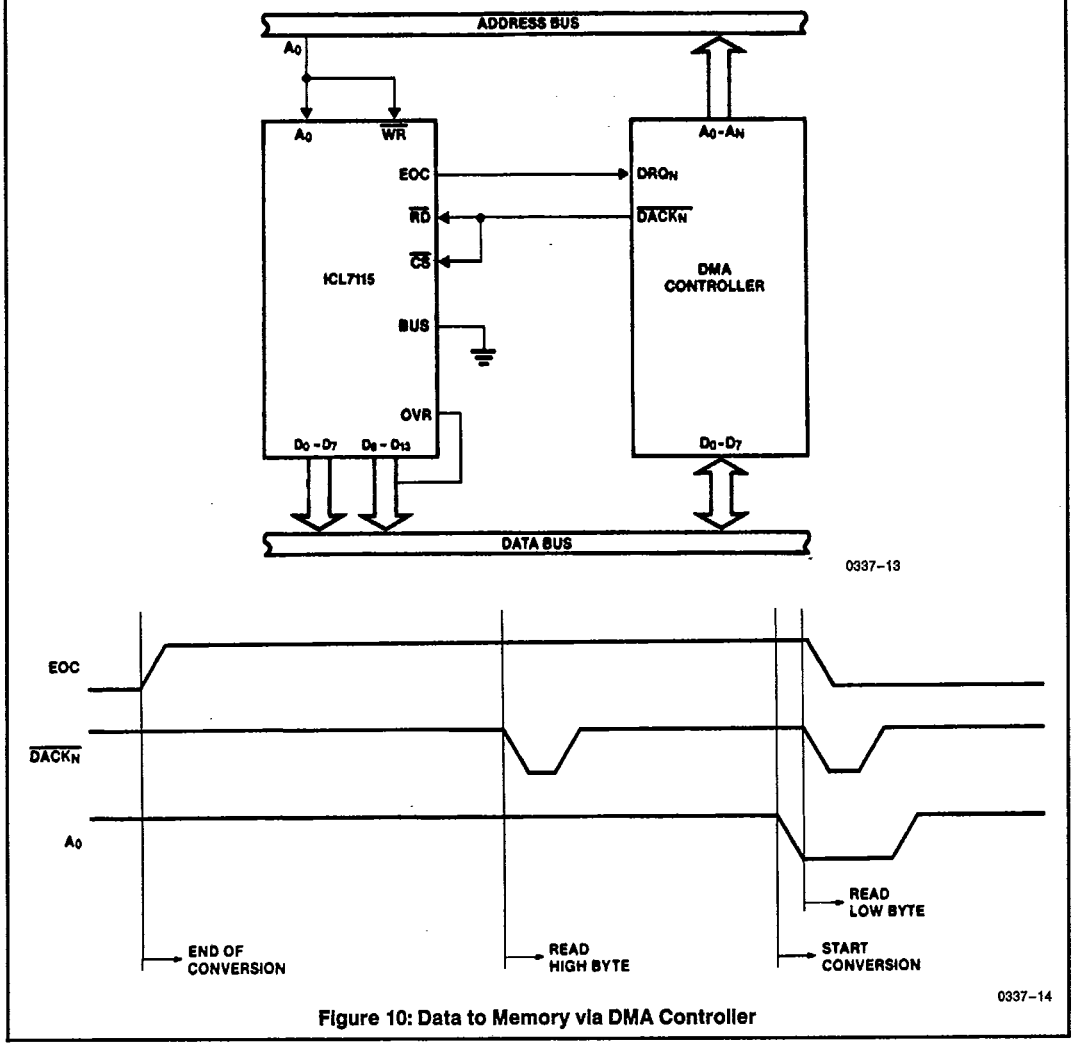



**Figure 10: Data to Memory via DMA Controller**



*NOTE: All typical values have been characterized but are not tested.*

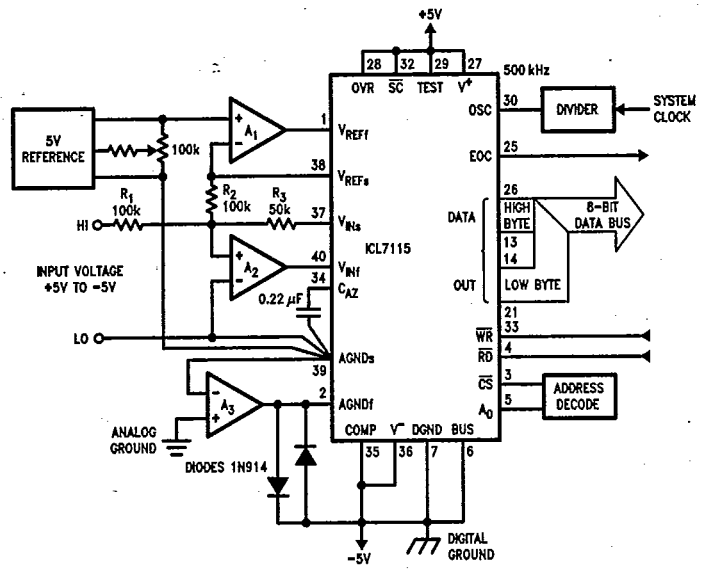



**Figure 11: Typical Application with Bipolar Input Range, Forced Ground, and 5 Volt Ultra-Stable Reference**

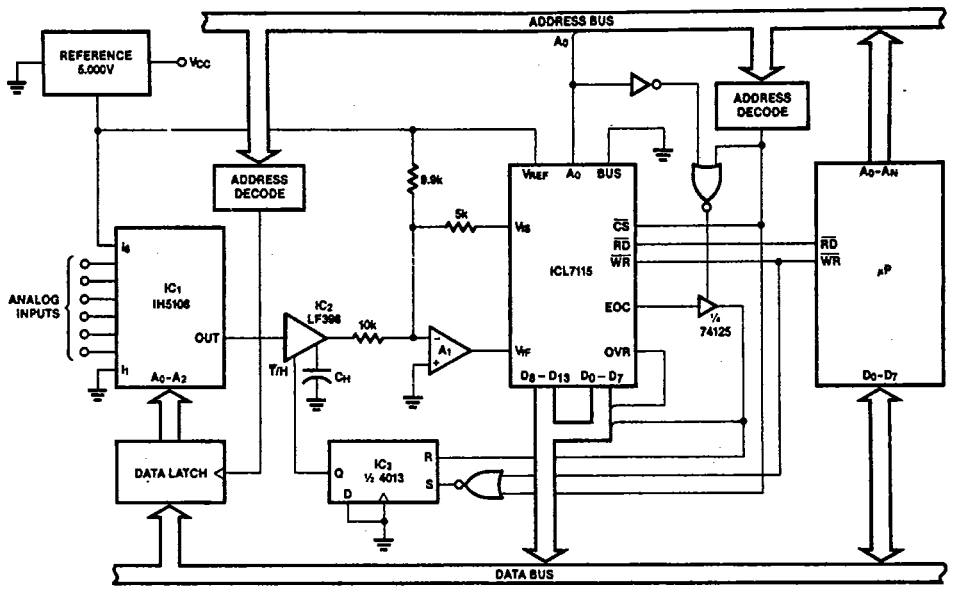



**Figure 12: Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction**



*NOTE: All typical values have been characterized but are not tested.*