MB86931

930 Series 32–BIT RISC EMBEDDED PROCESSOR/ INTERRUPT CONTROLLER/TIMER/USART

FUJITSU

MAY 24, 1994

FEATURES

- 40 MHz (25ns/cycle) operating frequency
- SPARC high performance RISC processor
  - 2 Kbytes 2–way set associative instruction and data caches.
  - Flexible cache data locking mechanism.
  - Harvard architecture
  - 8 window, 136 word register file
  - Fast interrupt response time
  - 247 address spaces, 4 Gbyte each
  - User and supervisor modes
  - Buffered writes and instruction pre–fetching
  - Fast page–mode DRAM support
  - Programmable address decoder and wait–state generator
  - On–chip clock generator circuit
  - JTAG test interface
  - Emulator support hardware
  - Single vector trapping
- 15–channel Interrupt Request Controller
  - Individual interrupt masks
  - Positive and negative level and edge trigger options for each channel
- Four independent 16–bit timers
  - Prescalers for two timers
  - Five modes of operation for each timer
- Two Serial Data Transmitter and Receiver Units
  - Compatible with MB89251
  - Synchronous and asynchronous operation
  - 5 to 8 bit character length selection
  - Parity bit option
  - Internal or external synchronous mode options
  - One (MONOSYNCH) or two (BISYNC) synchronous character options
- 0.8 micron gate CMOS technology.

GENERAL DESCRIPTION

The MB86931 features a high–performance processor combined with a 15–channel interrupt request controller, five independent 16–bit timers, and two independent serial data transmitters/receivers.

The processor is based on the SPARC architecture, is upward code compatible with previous processor implementations, and executes with 40 MIPs peak and 37 MIPs sustained performance at 40 MHz. On–chip data and instruction caches help decouple the processor from external memory latency. Separate on–chip instruction and data paths provide a high bandwidth interface between the IU and caches.

The interrupt controller supports 15 maskable, prioritized interrupts. The system processor can program each interrupt channel to trigger in response to a high level, a low level, a rising edge, or a falling edge. The IRC latches the interrupt requests and asserts the encoded level number of the highest–priority interrupt on the IRL<3:0> Interrupt Request Bus to interrupt the processor and identify the interrupt.

Four timers can each generate periodic interrupts and square waves, and each features two watchdog modes. They can be clocked by two prescalers, by external clocks, or by an internal MB86931 clock. A fifth timer generates an underflow signal, and is typically used for memory refresh timing.

The two Serial Data Transmitter and Receiver (SDTR) units support both synchronous and asynchronous modes, and are program–compatible with standard serial communication devices. They operate independently and can be clocked with the internal clock, with external clocks, or with clocks generated by the on–chip timers. Each SDTR supports the communication protocol and handshaking signals necessary for modem interface and control.

PIN ASSIGNMENT — 256-PIN SQFP

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	–RTS1	O	53	ADR < 11 >	O	105	XTAL1	I	157	D < 12 >	I/O
2	SYBRK1	I/O	54	ADR < 12 >	O	106	VSS	—	158	D < 11 >	I/O
3	VSS	—	55	ADR < 13 >	O	107	CLKOUT1	O	159	VSS	—
4	VSS	—	56	VDD	—	108	VDD	—	160	D < 10 >	I/O
5	VDD	—	57	VSS	—	109	CLKOUT2	0	161	D < 9 >	I/O
6	RCVDT1	I	58	ADR < 14 >	O	110	VSS	—	162	D < 8 >	I/O
7	RCLK1	I	59	ADR < 15 >	O	111	VDD	—	163	VDD	—
8	–TCLK1	I	60	ADR < 16 >	O	112	VSS	—	164	VSS	—
9	–CTS1	I	61	ADR < 17 >	O	113	ICEBRK	I	165	VSS	—
10	–DSR1	I	62	VSS	—	114	VSS	—	166	VDD	—
11	VSS	—	63	VDD	—	115	VDD	—	167	D < 7 >	I/O
12	NC	—	64	ADR < 18 >	O	116	ICESD < 3 >	I/O	168	D < 6 >	I/O
13	NC	—	65	ADR < 19 >	O	117	ICESD < 2 >	I/O	169	D < 5 >	I/O
14	–CS < 0 >	O	66	ADR < 20 >	O	118	ICESD < 1 >	I/O	170	D < 4 >	I/O
15	–CS < 1 >	O	67	ADR < 21 >	O	119	VSS	—	171	VSS	—
16	–CS < 2 >	O	68	VDD	—	120	VDD	—	172	VDD	—
17	–CS < 3 >	O	69	VSS	—	121	ICESD < 0 >	I/O	173	D < 3 >	I/O
18	–CS < 4 >	O	70	ADR < 22 >	O	122	ICED < 3 >	I/O	174	D < 2 >	I/O
19	VDD	—	71	ADR < 23 >	O	123	ICED < 2 >	I/O	175	D < 1 >	I/O
20	–CS < 5 >	O	72	ADR < 24 >	O	124	ICED < 1 >	I/O	176	D < 0 >	I/O
21	–SAME_PAGE	O	73	ADR < 25 >	O	125	ICED < 0 >	I/O	177	VDD	—
22	VSS	—	74	VSS	—	126	–ICEENBL	I	178	–RESET	I
23	VDD	—	75	VDD	—	127	VSS	—	179	–BREQ	I
24	–BE < 3 >	O	76	VDD	—	128	VDD	—	180	VSS	—
25	VSS	—	77	VSS	—	129	D < 31 >	I/O	181	–MEXC	I
26	–BE < 2 >	O	78	ADR < 26 >	O	130	D < 30 >	I/O	182	–READY	I
27	–BE < 1 >	O	79	ADR < 27 >	O	131	D < 29 >	I/O	183	VSS	—
28	–BE < 0 >	O	80	ADR < 28 >	O	132	VDD	—	184	VDD	—
29	ASI < 0 >	O	81	ADR < 29 >	O	133	D < 28 >	I/O	185	–BGRNT	O
30	VSS	—	82	ADR < 30 >	O	134	D < 27 >	I/O	186	VDD	—
31	VDD	—	83	ADR < 31 >	O	135	VSS	—	187	–ERROR >	O
32	ASI < 1 >	O	84	VSS	—	136	D < 26 >	I/O	188	–LOCK	O
33	ASI < 2 >	O	85	VDD	—	137	D < 25 >	I/O	189	–RD/WR	O
34	ASI < 3 >	O	86	TEST3*		138	D < 24 >	I/O	190	–AS	O
35	VDD	—	87	TEST2*		139	VSS	—	191	VSS	—
36	ASI < 4 >	O	88	TEST1*	—	140	VDD	—	192	NC	—
37	ASI < 5 >	O	89	TEST0*	—	141	VDD	—	193	NC	—
38	ASI < 6 >	O	90	VSS	—	142	D < 23 >	I/O	194	–DSR0	I
39	ASI < 7 >	O	91	CLKEXT	I	143	D < 22 >	I/O	195	–CTS0	I
40	ADR < 2 >	O	92	TDI		144	D < 21 >	I/O	196	–TCLK0	I
41	ADR < 3 >	OI	I 93	TRST	I	145	D < 20 >	I/O	197	RCLK0	I
42	ADR < 4 >	O	94	TCK	I	146	D < 19 >	I/O	198	RCVDT0	I
43	ADR < 5 >	O	95	TMS	I	147	VSS	—	199	VSS	—
44	VDD	—	96	VDD	—	148	D < 18 >	I/O	200	VDD	—
45	VSS	—	97	VSS	—	149	D < 17 >	I/O	201	SYBRK0	I/O
46	ADR < 6 >	O	98	VDD	—	150	D < 16 >	I/O	202	–RTS0	O
47	ADR < 7 >	O	99	TDO	O	151	VDD	—	203	–DTR0	O
48	ADR < 8 >	O	100	–TIMER_OVF	O	152	VSS	—	204	TRNDT0	O
49	ADR < 9 >	O	101	VDD	—	153	VDD	—	205	TXEMP0	O
50	VSS	—	102	VSS	—	154	D < 15 >	I/O	206	TxRDY0	O
51	VDD	—	103	VDD	—	155	D < 14 >	I/O	207	RxRDY0	O
52	ADR < 10 >	O	104	XTAL2	O	156	D < 13 >	I/O	208	VDD	—

* TEST0 - TEST2 (pins 86-89) are test pins that are intended for factory use only and *must* be tied to VSS for proper operation.

PIN ASSIGNMENT — 256-PIN SQFP (Continued)

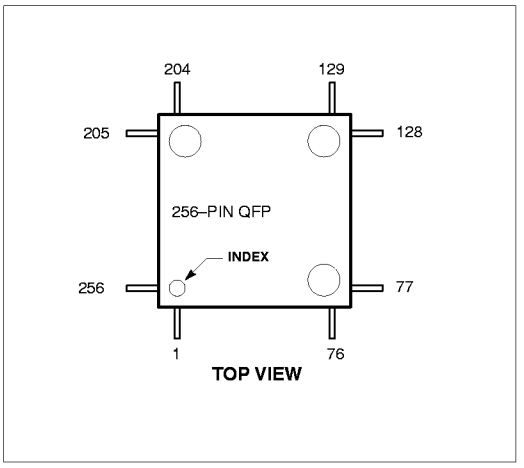
PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
209	VSS	—	221	IRQ1	I	233	IRQ11	I	245	ACK1	I
210	PRSCK0	O	222	IRQ2	I	234	VSS	—	246	IN1	I
211	OUT0	O	223	IRQ3	I	235	IRQ12	I	247	OUT3	O
212	OUT2	O	224	VSS	—	236	IRQ13	I	248	OUT1	O
213	IN0	I	225	IRQ4	I	237	IRQ14	I	249	PRSCK1	O
214	ACK0	I	226	IRQ5	I	238	IRQ15	I	250	VSS	—
215	CLK0	I	227	IRQ6	I	239	VSS	—	251	VDD	—
216	CLK2	I	228	IRQ7	I	240	VSS	—	252	RxRDY1	O
217	IN2	I	229	VDD	—	241	VDD	—	253	TxRDY1	O
218	VDD	—	230	IRQ8	I	242	IN3	I	254	TxEMP1	O
219	VSS	—	231	IRQ9	I	243	CLK3	I	255	TRNDT1	O
220	VSS	—	232	IRQ10	I	244	CLK1	I	256	–DTR1	O

ORDERING CODE

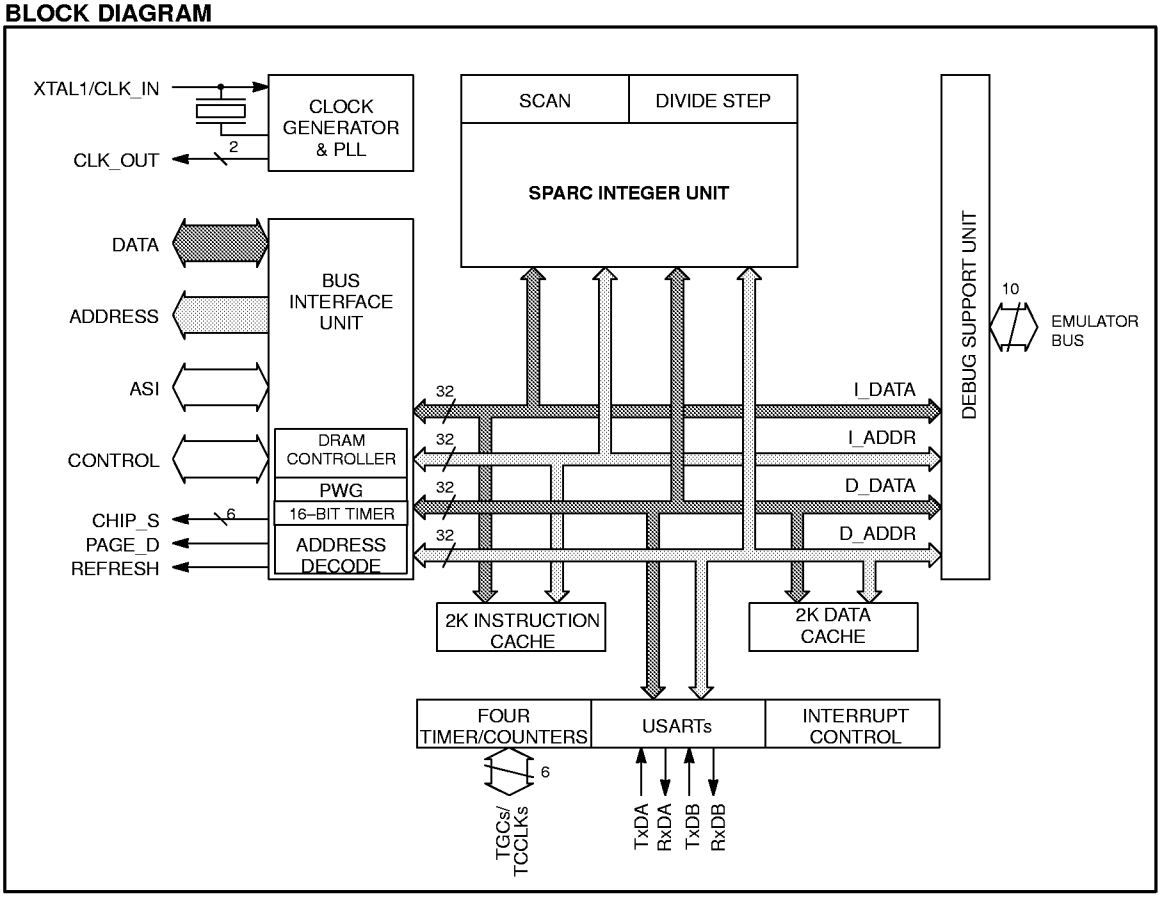
Clock Frequency (MHz)	Ordering Code	Package Type	Package Marking
20	MB86931–20ZF–G	Ceramic QFP 256	MB86931–20
40	MB86931–40ZF–G	Ceramic QFP 256 with heatsink	MB86931–40

Note: The ordering code is for production level product. Early shipments of this device may be marked with "ES" to indicate that the part is not yet at full production status. Contact your local Fujitsu representative for additional information on "ES" level products.

PIN CONFIGURATION



BLOCK DIAGRAM



SIGNAL DESCRIPTIONS [1]

SYMBOL	TYPE	DESCRIPTION
–RESET	I A (L)	**SYSTEM RESET:** Asserting reset for at least 20 processor cycles after the clock has stabilized, causes the MB86931 to be initialized.
XTAL1, (CLK_IN) XTAL2	I/O O G (Q) I (Q)	**EXTERNAL OSCILLATOR:** The crystal inputs determine execution rate and timing of the MB86931 processor. Connecting a crystal to these pins forms a complete crystal oscillator circuit. The crystal oscillator frequency is the same as the processor operating frequency. When driving the processor with an external clock, XTAL2 pin should be left floating.
CLKOUT1	O G (Q) I (Q)	**CLOCK OUTPUT 1:** This is an output signal against which MB86931 bus transactions can be referenced. The CLKOUT1 frequency is the same as the frequency applied to XTAL1 and is the same as the processor operating frequency. CLKOUT1 is in phase with CLK_IN.
CLKOUT2	O G (Q) I (Q)	**CLOCK OUTPUT 2:** This is an output signal against which MB86931 bus transactions can be referenced. The CLKOUT2 frequency is the same as the frequency applied to XTAL1 and is the same as the processor operating frequency. CLKOUT2 is out of phase with CLK_IN.
–LOCK	O S (L) G (Z) I (1)	**BUS LOCK:** This is a control signal asserted by the processor to indicate to the system that the current bus transaction requires more than one transfer on the bus. The Atomic Load Store instruction for example requires contiguous bus transactions which cause the assertion of the bus lock signal. The bus may not be granted to another bus owner as long as –LOCK is active. –LOCK is asserted with the assertion of –AS and remains active until –READY is asserted at the end of the locked transaction.
–BREQ	I S (L)	**BUS REQUEST:** Asserted by another device on the bus to indicate that it wants ownership of the bus. The request must be answered with a bus grant (–BGRNT) from the MB86931 before the device can proceed by driving the bus. Once the bus has been granted, the device has ownership of the bus until it de–asserts –BREQ. The user should ensure that devices on the bus cannot monopolize the bus to the exclusion of the CPU. Inputs to –BREQ while –RESET is active are valid and cause Bus Grant to be asserted.
–BGRNT	O S (L) G (0) I (Q)	**BUS GRANT:** Asserted by the CPU in response to a request from a device wanting ownership of the bus. The CPU grants the bus to other devices only after all transfers for the current transaction are completed. See the "Notes" section at the end of this table and the "Type" column for other signals to determine the effect due to the assertion of –BGRNT.
–ERROR	O A (L) G (Q) I (Q)	**ERROR SIGNAL:** Asserted by the CPU to indicate that it has halted in an error state as a result of encountering a synchronous trap while traps are disabled. In this situation the CPU saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state and asserts the –ERROR signal. The system can monitor the –ERROR pin and initiate a reset under the error condition. This pin is high on reset.
–MEXC	I S (L)	**MEMORY EXCEPTION:** Asserted by the memory system to indicate a memory error on either a data or instruction access. Assertion of this signal initiates either a data or instruction access exception trap in the IU. The current bus access is invalidated by asserting the –MEXC in the same cycle as the –READY signal. Assertion in any other bus cycle gives indeterminate results. The IU ignores the contents of the data bus in cycles where –MEXC is asserted.

SYMBOL	TYPE	DESCRIPTION
–TIMER_OVF	O S (L) G (Q) I (Q)	**TIMER UNDERFLOW:** Asserted by the processor to indicate that the internal 16–bit timer has underflowed. This signal can be used to initiate a DRAM refresh cycle or a one cycle periodic waveform. On reset, the timer is turned off and –TIMER_OVF is high.
–SAME_PAGE	O S (L) G (1) I (1)	**SAME–PAGE DETECT:** The –SAME_PAGE is used to take advantage of fast consecutive accesses within Fast Page Mode DRAM page boundaries. This signal is an output asserted by the processor when the current address is within the same page as the previous memory access. The –SAME_PAGE signal is asserted with –AS and remains active for one processor cycle. –SAME_PAGE is never asserted in the first transaction following a transaction by another device on the bus. The page size is specified by writing the SAME–PAGE MASK register.
–CS0, –CS1, –CS2, –CS3, –CS4, –CS5	O S (L) G (1) I (1)	**CHIP SELECTS:** These outputs are asserted when the value on the address bus matches the address range in one of the corresponding ADDRESS RANGE registers. The signals are used to decode the current address into one of six address ranges. Address ranges should not overlap. Each address range has a corresponding wait specifier which is used to automatically assert the –READY signal after a user defined number of processor clock cycles. This allows a variety of memory and I/O devices with different access times to be connected to the MB86931 without the need for additional logic.
ADR < 31:2 >	O S (L) G (Z) I (1)	**ADDRESS BUS:** The 30–bit ADDRESS BUS (A31–A2) is an output which identifies the data or instruction address of a 32–bit word. Reads are always one word in size while byte, half–word, or word transaction sizes for writes is identified by separate byte–enable signals (–BE0–3). The address bus is valid for the duration of the bus transaction.

SIGNAL DESCRIPTIONS (Continued)

<table>
<tr><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>ASI < 7:0 ></td><td>O
S (L)
G (Z)
I (1)</td><td>ADDRESS SPACE IDENTIFIERS: The ADDRESS SPACE IDENTIFIERS are outputs which indicate to which of 256 available spaces the current ADDRESS BUS value corresponds. The ASI values are defined as follows:

<table>
<tr><th>ASI < 7:0 ></th><th>ADDRESS SPACE</th></tr>
<tr><td>0x1</td><td>Control Registers</td></tr>
<tr><td>0x2</td><td>Instruction Cache Lock</td></tr>
<tr><td>0x3</td><td>Data Cache Lock</td></tr>
<tr><td>0x4 – 0x7</td><td>Application Definable</td></tr>
<tr><td>0x8</td><td>User Instruction Space</td></tr>
<tr><td>0x9</td><td>Supervisor Instruction Space</td></tr>
<tr><td>0xA</td><td>User Data Space</td></tr>
<tr><td>0xB</td><td>Supervisor Data Space</td></tr>
<tr><td>0xC</td><td>Instruction Cache Tag RAM</td></tr>
<tr><td>0xD</td><td>Instruction Cache Data RAM</td></tr>
<tr><td>0xE</td><td>Data Cache Tag RAM</td></tr>
<tr><td>0xF</td><td>Data Cache Data RAM</td></tr>
<tr><td>0x10 – 0xFD</td><td>Application Definable</td></tr>
<tr><td>0xFE – 0xFF</td><td>Reserved for Debug Hardware</td></tr>
</table>

The ASI values specified as “application definable” can be used by supervisor mode instructions such as Load Alternate and Store Alternate. The ASI value is available in the same cycle in which the corresponding address value is asserted on the address bus. The ASI pins are valid for the duration of the bus transaction. ASI values 0x8, 0x9, 0xA, and 0xB are cacheable.</td></tr>
<tr><td>–BE3–0</td><td>O
S (L)
G (Z)
I (O)</td><td>BYTE ENABLES (0): Indicate whether the current load or store transaction is a byte, halfword or word transaction. The BYTE ENABLE value is available in the same cycle is which the corresponding address value is asserted on the address bus. The values on the byte enable pins are valid for load and store operations and for the duration of the bus transaction. Since the processor extracts the appropriate byte of halfword from the word being read, the byte enable signals can be ignored during load operations.
Possible values for –BE3–0 are as follows:

<table>
<tr><th></th><th>Byte 0
31 24</th><th>Byte 1
23 16</th><th>Byte 2
15 8</th><th>Byte 3
7 0</th></tr>
<tr><td>Byte Writes</td><td>1 1 1 0</td><td>1 1 0 1</td><td>1 0 1 1</td><td>0 1 1 1</td></tr>
<tr><td>Half–Word Writes</td><td colspan="2">1 1 0 0</td><td colspan="2">0 0 1 1</td></tr>
<tr><td>Word Writes</td><td colspan="4">0 0 0 0</td></tr>
</table>
</td></tr>
</table>

SIGNAL DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
D < 31:0 >	I/O S (L) G (Z) I (Z)	**DATA BUS:** The bus interface has 32 bidirectional data pins (D31–D0) to transfer data in thirty–two bit quantities. D (31) corresponds to the most significant bit of the least significant byte of the 32–bit word. A double word is aligned on an 8–byte boundary, a word is aligned on a 4–byte boundary, and a half–word is aligned on a 2–byte boundary. If a load or store of any of these quantities is not properly aligned, a Not Aligned Trap will occur in the processor. In write bus cycles, the point at which data is driven onto the bus depends on the type of the preceding cycle. If the preceding cycle was a write, data is driven in the cycle immediately following the cycle in which –READY was asserted. If the preceding cycle was a read, data is driven one cycle after the cycle in which –READY was asserted to minimize bus contention between the processor and the system. All bits of the data bus are driven regardless of word size. The values on the pins not corresponding to the byte or half–word being written are undefined.
–AS	O S (L) G (Z) I (1)	**ADDRESS STROBE:** A control signal asserted by the MB86931 or other bus master to indicate the start of a new bus transaction. A bus transaction begins with the assertion of –AS and ends with the assertion of –READY. –AS remains asserted for 1 clock cycle. During cycles in which neither the processor nor another bus master is driving the bus the bus is idle, and –AS remains de–asserted.
RD/–WR	O S (L) G (Z) I (1)	**READ/BUS TRANSACTION:** This signal specifies whether the current bus transaction is a read or a write operation. When –AS is asserted and RD/–WR is low, then the current transaction is a write. With –AS asserted and RD/–WR high, the current transaction is a read. RD/–WR remains active for the duration of the bus transaction and is de–asserted with the assertion of –READY.
–READY	I S (L)	**READY:** This is a control signal asserted by the external memory system to indicate that the current bus transaction is being completed and that it is ready to start with the next bus transaction in the following cycle. In case of a fetch from memory, the processor will strobe the value on the data bus at the rising edge of CLK_IN following the assertion of –READY. For the case of a write, the memory system will assert –READY when the appropriate access time has been met. In most cases, no additional logic is required to generate the –READY signal. On–chip circuitry can be programmed to assert –READY based on the address of the current transaction. The external system can override the internal ready generator to terminate the current bus cycle early. Up to 6 address ranges each with different transaction times can be programmed.
CLK_ECB	I	**EXTERNAL CLOCK BYPASS:** Tying this signal high causes the CLK_IN signal to bypass the Phases Lock Loop (PLL). This signal is used for testing of the chip.
EMU_SD < 3:0 >	I/O	**EMULATOR STATUS/DATA BITS:** Bi–directional pins used by a hardware emulator to control and monitor MB86931 execution. These pins should be left unconnected.
EMU_D < 3:0 >	I/O	**EMULATOR DATA BITS:** Bi–directional pins used by a hardware emulator to control and monitor MB86931 execution. These pins should be left unconnected.
EMU_BRK	I	**EMULATOR BREAK REQUEST LINE:** Input used by a hardware emulator to request a trap when emulation is enabled. This pin should be left unconnected.
–EMU_ENB	I	**EMULATOR ENABLE:** Tied low while the MB86931 is being reset to enable hardware emulator mode on the chip. This pin should be left unconnected.
TCK	I	**TEST CLOCK:** JTAG compatible test clock input.

SIGNAL DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
TMS	I	**TEST MODE:** JTAG compatible test mode select pin.
TDI	I	**TEST DATA IN:** JTAG compatible test data input.
TDO	O	**TEST DATA OUT:** JTAG compatible test data output.
–TRST	I	**TEST RESET:** Asynchronous reset for JTAG logic. If not using JTAG, this signal must be pulled low.

NOTE:

I = Input Only Pin
O = Output Only Pin
I/O = Either Input or Output Pin
– = Pins "must be" connected as described
A (L) = Asynchronous: Inputs may be asynchronous to CLKOUT.
S (L) = Synchronous: Inputs must meet setup and hold times relative to CLK_IN Outputs are Synchronous to CLK_IN

G (...) = While the bus is granted to another bus master (–BGRNT=asserted), the pin is
G (1) is driven to V_{CC}
G (0) is driven to V_{SS}
G (Z) floats
G (Q) is a valid output

I (...) = While the bus is between bus cycles (or being reset) and is not granted to another bus master, the pin is
I (1) is driven to V_{CC}
I (0) is driven to V_{SS}
I (Z) floats
I (Q) is a valid output

INTERRUPT REQUEST SIGNAL DESCRIPTIONS

NAME	TYPE	DESCRIPTION
IRQ < 15:1 >	I	Interrupt Request. These are prioritized system interrupt requests. IRQ15 has the highest priority, and IRQ1 the lowest. The trigger for each interrupt can be programmed for a high level, a low level, a rising edge, or a falling edge. The level–trigger interrupt request signals are sampled during three successive internal clock periods to minimize false interrupts.

TIMER SIGNAL DESCRIPTIONS

NAME	TYPE	DESCRIPTION
CLK < 3:0 >	I	Timer external clock input. In the external clock mode, this signal is synchronized with the internal clock before use. These pins should be tied high or low when not used.
OUT < 3:0 >	O	Timer output pin. According to the mode, the output wave functions as (1) periodic interrupt signal output; (2) square wave output; (3) one–shot pulse output. These pins are low during reset.
IN < 3:0 >	I	Count control input. These inputs are used as gate signals in Modes 0 to 3, and as external triggers in Mode 4.
ACK0 ACK1	I	Asynchronous clock. These are prescaler input clocks that are used when selected in the Prescaler registers. The clocks are synchronized with the internal clock and are divided and output to the PRSCKx pin. When not used, they should be tied low.
PRSCK0 PRSCK1	O	Prescaler output.

SDTR SIGNAL DESCRIPTIONS

NAME	TYPE	DESCRIPTION
–DSR0 –DSR1	I	Modem Data Set Ready signal. The status of these pins is loaded into bit 7 of the corresponding SDTR status register.
–RTS0 –RTS1	O	Modem Request to Send signal. When bit 5 of the command register is set to 1, these signals are driven low.
–DTR0 –DTR1	O	Modem Data Terminal Ready or Rate Select signal. When bit 1 of the command register is set to 1, these signals are driven low.
–CTS0 –CTS1	I	Modem Clear to Send signal. A transmitter is enabled only when its corresponding –CTSx signal is low.
TRNDT0 TRNDT1	O	Serial transmit data. Parallel data written in the data register is converted into serial data, then transmitted through these pins. In the asynchronous mode, start and stop bits are added to data, and a parity bit can be added. If there is no data to be transmitted, the SDTR transmits synchronous characters in the synchronous mode, and enters the mark state in the asynchronous mode. The mark state also occurs after a transmit disable command is specified (bit 0 of the command register is set to 0) or when –CTS is High. Note that the mark state occurs during transmission after: (1) One byte is transmitted if a transmit disable command is specified during transmission; (2) the second synchronous character is transmitted if the first synchronous character was transmitted (with the synchronous state held) in the BISYNC mode.
TxEMP0 TxEMP1	O	These signals are driven high if there is no data to be transmitted in the SDTR. These signals are driven low at the falling edge of the write signal when the processor writes a byte to be transmitted.
TxRDY0 TxRDY1	O	These signals are driven low if the transmit data buffer register becomes empty with the –CTS pin low and the transmitter is enabled.
–TCLK0 –TCLK1	I	Clock for determining the transmission baud rate. In the synchronous mode, since the baud rate is fixed at transmit clock x 1, the frequency of the clock to be input to the –TCLK pin is the transmission baud rate. In the asynchronous mode, the transmit clock x 1/16 and x 1/64 frequencies will be the transmission baud rate in accordance with the baud rate set in the mode register. For example, if a clock of 19.2 kHz is input to the –TCLK pin, the transmission baud rate is 1200 bauds at x 1/16, and 300 bauds at x 1/64. The transmit data is synchronized with the falling edge of this transmit clock.
RCVDT0 RCVDT1	I	Serial receive data input. The input data is converted to parallel data in the SDTR and can be read via the system data bus.
RCLK0 RCLK1	I	Clock for determining the receive baud rate. In the synchronous mode, since the baud rate is fixed at receive clock x 1, the frequency of the clock to be input to the RCLK pin is the receive baud rate. In the asynchronous mode, the receive clock x 1/16 and x 1/64 frequencies will be the receive baud rate in accordance with the baud rate set in the mode register. For example, if a clock of 19.2 kHz is input to the RCLK pin, the receive baud rate is 1200 bauds at x 1/16, and 300 bauds at x 1/64. The receive data is sampled at the falling edge of this receive clock.

SDTR SIGNAL DESCRIPTIONS

NAME	TYPE	DESCRIPTION
SYBRK0 SYBRK1	I/O	SYBRK0/SYBRK1. When the external synchronous mode is set in the mode register, synchronous signals are output from these pins. If H–level signals are input to these pins when RCLK is high during hunt, the data sampled at the rising edge of the next RCLK will be the start bit of the received data. When the internal synchronous mode is selected, these pins are used as synchronous character detection pins. If the received data coincides with the data loaded in the synchronous character register (in the BISYNC mode, data for two characters coincide with each other), these are driven high. Then, when the MPU reads data out of the status register, these pins are driven low at the end of the read–out signal strobe. When used in the asynchronous mode, these signals function as break code detection signals. If the received data (including start, stop, and parity bits) is all 0s immediately after a framing error occurs, these signals are driven high. The signals are released when reset is executed or when 1 data is received.
RxRDY0 RxRDY1	O	These pins are driven high when the serial data received at the RCVDT pin is converted to parallel data in the SDTR, allowing the processor to read the data. The signals are driven low when the processor reads the data.

OVERVIEW

The Fujitsu MB86931 features a high performance 32–bit RISC processor that executes at 40 MIPs peak and 37 MIPs sustained performance at 40 MHz, an interrupt controller, five 16–bit timers, and two independent serial data transmitter/receiver units.

The processor core is a fourth generation version of Fujitsu's popular MB86900, MB86901, and MB86902 processors. Like its predecessors, the MB86931 processor is based on the SPARC architecture, and is upward code compatible with previous processor implementations.

The MB86931 instruction set is streamlined and hardwired for fast execution with most instructions executing in a single cycle. The Integer Unit (IU) features a 5–stage pipeline that is designed to handle data interlocks, an optimized branch handler for efficient control transfers, and a bus interface that handles single–cycle bus accesses to on–chip memory.

An internal register file consisting of 136 registers organized into eight overlapping windows speeds interrupt response time and context switches. The register file minimizes accesses to memory during procedure linkages and facilitates passing of parameters and assignment of variables.

On–chip 2 Kbyte data and instruction caches decouple the processor from external memory. These caches have been designed for maximum flexibility, and allow entries to be locked for improved system performance.

Separate 32–bit on–chip instruction and data paths provide a high bandwidth interface between the IU and the on–chip caches. This bus architecture supports both single–cycle instruction execution and single–cycle data transfers, and will be compatible with future enhancements of the MB86931.

The MB86931 also includes hardware for integer multiplication and division that allows 5–cycle 32–bit integer multiplication, 3–cycle 16–bit integer multiplication, 2 cycle 8–bit integer multiplication, and single–cycle multiplication by zero.

The on–chip interrupt controller supports 15 maskable, prioritized interrupts. Four of the five MB86931 timers can generate periodic interrupts and square waves, and feature two watchdog modes. A fifth timer generates an underflow signal, and is typically used for memory refresh timing.

The two Serial Data Transmitter and Receiver (SDTR) units operate independently and support both synchronous and asynchronous modes. They can be clocked with the internal clock, with external clocks, or with clocks generated by the on–chip timers, and support the communication protocol and handshaking signals necessary for modem interface and control.

KEY PROCESSOR FEATURES

Fast Instruction Execution: Simple functions make up the bulk of instructions in most programs so that execution speed can be greatly improved by designing these instructions to execute in as short a time as possible. The majority of instructions execute in one cycle with only a few of the more complex, such as integer multiply, taking additional cycles.

Large Register Set: The large register set reduces the number of required accesses to data memory. The registers are organized in overlapping groups called register windows which allows registers to be reserved for high priority tasks, such as interrupts, or for recurring requirements such as operating system working registers. The overlapping windows also simplify parameter passing during procedure linkage and reduce code in most programs.

On–Chip Caches: To decouple the speed of the processor from the memory sub–system, data and instructions caches have been added. The caches are organized as two–way set–associative for improved hit rates. In addition, the set–associative caches allow entries to be locked, individually or as a bank, without significantly degrading the cache performance.

Cache Locking: Both data and instruction entries can be locked into their respective caches to ensure deterministic response and highest performance for critical or frequently recurring routines. Maximum flexibility has been designed into the cache to allow all or selected portions to be locked.

Bus Interface: The requirement for glue logic between the MB86931 and the system is minimized by providing programmable chip selects, programmable wait state circuitry, and support for connection to fast page–mode DRAM. Multiple bus masters are supported through a simple handshake protocol.

Clock Generator: To simplify the clock design a crystal can be connected directly to the on–chip oscillator or an external clock source can be used. A built in phase–locked loop minimizes the skew between on and off–chip clocks.

Enhanced Instruction Set: The MB86931 incorporates a fast integer multiply instruction which executes in a fast 5, 3 or 2 cycles for 32–bit, 16–bit or 8–bit multiplicands. An integer divide–step instruction cuts divide times by a factor of 10 over previous SPARC implementations. A scan instruction supports a single cycle search for the most significant 1 or 0 in a word.**Fully Static Circuit Design:** Embedded applications that need a means to reduce power consumption can take advantage of the MB86931's fully static design. The processor clock can be slowed or stopped for arbitrary periods of time to reduce operating current with no loss of internal state. Noise immunity is improved as well. (note: stopping the clock will result in the Phase–Lock Loop losing lock. Lock must be re–established before normal operation can be resumed.)

Test and Debug Interface: The MB86931 supports production test through industry standard JTAG boundary scan. Hardware emulation is supported with on–chip breakpoint and single step logic. A dedicated emulator bus provides a means to trace transactions between the integer unit and on–chip cache.

CPU

The MB86931 core is a high performance fully custom implementation of the SPARC architecture. The core is compact to leave room for peripheral integration and yet is designed in a way to allow the major blocks to be customized for varying application requirements. The core is made up of three functional units: the Instruction block, the Address block and the Execute block. (see *Figure 1*)

TABLE 1. MB86931 Instruction Set

LOGICAL	ARITHMETIC/SHIFT	DATA MOVEMENT
CONDITION CODES UNCHANGED AND OR XOR AND NOT OR NOT XNOR	**CONDITION CODES UNCHANGED** ADD SUBTRACT MULTIPLY (SIGNED/UNSIGNED) SCAN SETHI SHIFT LEFT LOGICAL SHIFT RIGHT LOGICAL SHIFT RIGHT ARITHMETIC	**TO USER/SUPERVISOR SPACE SIGNED** LOAD BYTE LOAD HALF–WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF–WORD STORE WORD STORE DOUBLE WORD
CONDITION CODES SET AND OR XOR AND NOT OR NOT XNOR	**CONDITION CODES SET** ADD SUBTRACT MULTIPLY (SIGNED/UNSIGNED) MULTIPLY STEP DIVIDE STEP	**TO USER SPACE UNSIGNED** LOAD BYTE LOAD HALF–WORD
CONTROL TRANSFER	**EXTENDED AND CONDITION CODES UNCHANGED** ADD SUBTRACT	**TO ALTERNATE SPACE SIGNED** LOAD BYTE LOAD HALF–WORD LOAD WORD LOAD DOUBLE WORD STORE BYTE STORE HALF–WORD STORE WORD STORE DOUBLEWORD
CONDITIONAL BRANCH CONDITIONAL TRAP CALL RETURN SAVE RESTORE JUMP AND LINK	**EXTENDED AND CONDITION CODES SET** ADD SUBTRACT **TAGGED AND CONDITION CODES SET (WITH AND WITHOUT TRAP ON OVERFLOW)** ADD SUBTRACT	**TO ALTERNATE SPACE UNSIGNED** LOAD BYTE LOAD HALF–WORD **ATOMIC OPERATION IN USER SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE **ATOMIC OPERATION IN ALTERNATE SPACE** SWAP WORD LOAD/STORE UNSIGNED BYTE
READ/WRITE CONTROL REGISTER		
READ PSR WRITE PSR READ TBR WRITE TBR	READ WIM WRITE WIM READ Y WRITE Y	RDASR WRASR

A five stage instruction pipeline is responsible for decoding all instructions and generating the control signals to the other blocks. The 5–stage pipeline consists of Fetch (F), Decode (D), Execute (E), Memory (M) and Writeback (W). Instruction memory is addressed and returns instructions in the (F) stage, the register file is addressed and returns operands in the (D) stage, the ALU computes results in the (E) stage, external memory is addressed in the (M) stage, and the register file is written back in the (W) stage.

ADDRESS SPACE

The MB86931 offers a large addressing range and allows separate user and supervisor spaces to be defined. In addition to 32 address lines, 4 alternate address space identifiers (ASIs) distinguish between protected and unprotected space. Of the 256 possible ASI values, two define accesses to user data and user instruction space while the remaining ASI values define supervisor space.

Anytime a reset, synchronous trap or asynchronous trap occurs, the processor is placed into the supervisor mode. In this mode, the processor executes instructions and moves data out of supervisor space. While in supervisor mode, the processor also has access to the remaining ASI values. Except for those mentioned and those reserved for control register space, the remaining ASI values can be used to access other alternate data spaces defined by the application.

The distinction of user versus supervisor space allows the hardware to protect against accidental or un–authorized access to system resources. For real time operating system (RTOS) development for example, the separate spaces provide a mechanism for effectively partitioning RTOS space from user space.

REGISTERS

The MB86931 register set is divided into those used for general purpose functions and those used for control and status.

The 136 general purpose registers are divided into 8 global registers and 8 overlapping blocks or “windows”. Each window contains 24 registers. Of these, 8 are local to the window, 8 “out” registers overlap with the next window and 8 “in” registers overlap with the previous window (see *Figure 2*).

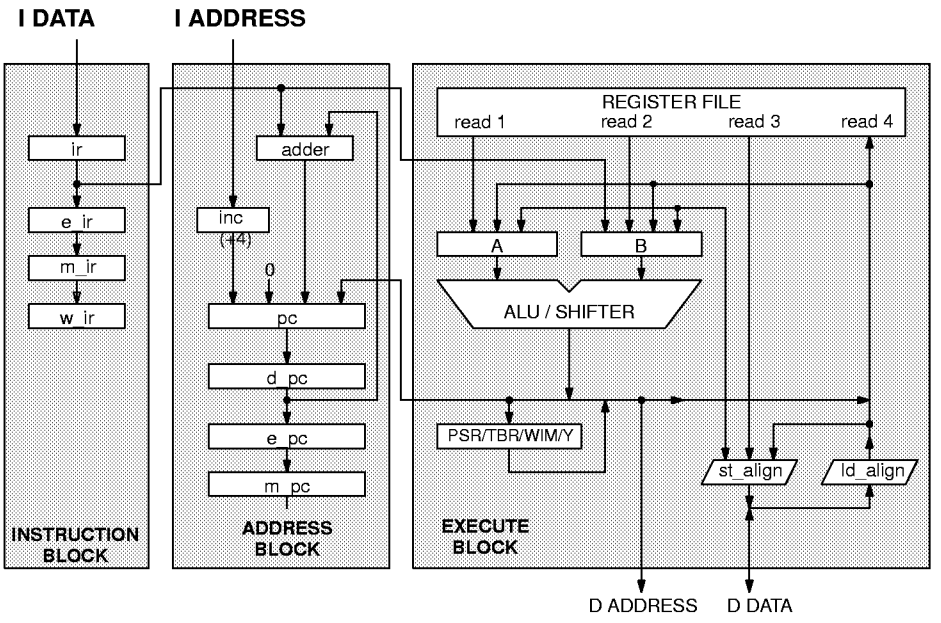


Figure 1. MB86931 Integer Unit Data Path

This organization makes it easy to pass parameters to subroutines. Parameters that are to be passed along are written to the "out" registers and the subsequent procedure call decrements the window pointer to make a new set of registers available. The passed parameters are now available to the subroutine in the current window's "in" registers.

Register windows improve performance in embedded applications because they function as local variable caches which retain either interrupt, subroutine, context or operating system variables with no additional overhead. In addition, code can be reduced by exploiting the efficient execution of procedure linkage by preventing in–lining compiler optimizations.

The registers that make up the register file each have three read–only and one write–only port. The use of a four port register file allows even store instructions, which may require that three operands be read out of the register file, to proceed at one instruction per cycle.

The control and status registers include those defined by the SPARC architecture (See *Table 1*) and those mapped into alternate address space to control peripheral functions (See *Table 2*).

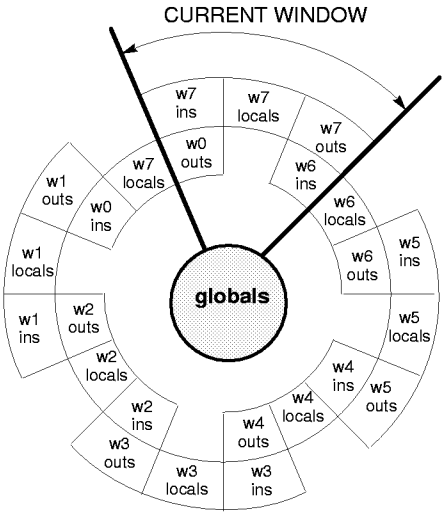


Figure 2. General Purpose Register Organization

INSTRUCTION SET

The MB86931 is upward code compatible with other SPARC processors. Additional instructions, previously not directly supported, have been added to improve performance in embedded applications. Integer multiply, integer divide step, and scan for first changed bit have been added to the already powerful SPARC instruction set. See *Table 1* for a list of supported instructions.

INTERRUPTS

A key measure of a processor's suitability for use in embedded application is in its ability to handle interrupts with a minimum of delay and in a deterministic fashion. The MB86931 implementation has been tailored to insure not only low average latency but low maximum latency as well.

Interrupt response time is made up of the sum of the times it takes the processor to finish its current task after recognizing an interrupt, and the time it takes to begin executing interrupt service routine instructions. The MB86931 implements numerous features to minimize both factors.

To minimize the time it takes to finish the current task, the MB86931 is designed so that tasks can either be interrupted or completed in a minimum of cycles. Implementation details that accomplish this aim include cache line misses that are filled one word at a time through a pre–fetch buffer, integer divide that is interruptible through the use of a divide step instruction, fast multiply and a 1 word write buffer to limit pending bus transactions.

To minimize the time required to start executing the interrupt service routine the processor switches to a new register window when an interrupt is detected. This feature allows the service routine to be executed without first requiring that the current registers be saved. The user can also elect to lock the service routine into the cache. This makes the routine available for immediate access. The on–chip data cache can also serve the service routine as a fast local stack for minimum delay in accessing routine variables.

The MB86931 provides for up to 15 different interrupt levels and direct support for 15 separate interrupt sources. The highest interrupt level is non–maskable.

CACHE

The MB86931 has separate on–chip data and instruction caches. This allows the user to build a high performance system without incurring the cost of requiring fast external memory and the associated control logic.

The data and instruction caches are each organized as two banks of sixty–four 16–byte lines (see *Figure 3*). The lines are organized as two–way set–associative for good performance even when cache locking is in effect. Lines are divided into four sub–blocks each four bytes wide. On a cache miss, the cache is updated in sub–block increments for efficient re–fill of typical code segments and to avoid interrupt latency incurred by long cache line replacements. An instruction pre–fetch buffer fetches the next sequential instruction anticipating that it will be needed to fill the next instruction cache miss.

The caches can be used in either normal or one of two lock modes. In normal mode, the caches use an LRU (least recently used) algorithm to replace one of the two appropriate entries. Alternately, the two locking modes allow the entire cache or just selected entries to be locked. The lock modes allow time critical routines to be locked in cache.

Global locking allows the entire content of either the instruction or data cache to be frozen. Two control bits in the cache control register enable or disable locking for either cache. With the entire cache locked, no valid entry can be replaced. To insure best possible performance however, invalid entries will be updated if they are accessed. This is done automatically and incurs no time penalty.

Local cache locking makes it possible to dynamically lock selected instructions or data entries into the appropriate cache. This feature gives the flexibility, for example, to assure deterministic response for certain critical interrupt routines by locking the routine's code into the cache. Entries can also be locked where it is desirable to give performance priority to certain often used routines which might otherwise be removed from cache. The 2–way set–associativity allows the cache to perform effectively even with some locked entries.

In local lock mode, each entry can either be locked individually by software or automatically with hardware assist. For individual locking, software writes the lock bit in the appropriate cache tag line. For automatic locking, a bit in each cache control register enables or disables the feature. The enable bit is set at the beginning of a routine for which the entries are to be locked. This causes the location of any cache access occurring while the bit is enabled to be locked into the cache. In addition to requiring just one initial cycle to enable, automatic entry locking incurs no overhead while in effect.

In unlocked operation, the data cache uses a write–through update policy and allocates a cache entry only on a load. Writes are buffered so that the processor can continue executing while data is written back to memory. In contrast, writes to locked data cache locations are not written through to main memory. Besides reducing external bus activity, this design supports configuring a portion of data cache as on–chip RAM which does not map to external memory.

The data and instruction caches are designed to be accessed independently over separate data and instruction buses to allow data to be loaded from and stored to cache at peak rates of 1 CPI.

INTERRUPT CONTROLLER

The Interrupt Request Controller (IRC) is a 15–channel, programmable–trigger interrupt controller that arbitrates pending unmasked interrupt requests, encodes the highest–priority interrupt, and interrupts the processor. The system processor responds by servicing the interrupt and clearing the latched interrupt request in the IRC.

Figure 4 shows a block diagram of the IRC.

The Trigger Mode Control logic selects one of four trigger modes for each channel: high level, low level, rising edge, or falling edge. The processor controls the triggers by writing to the Trigger Mode registers.

The IRQ Latch captures each interrupt request. The system processor reads the latch via the Request Sense register, and clears the latch by writing to the Request Clear register.

The IRQ Mask logic allows selective masking of the interrupts. The processor controls masking by writing to the Mask register.

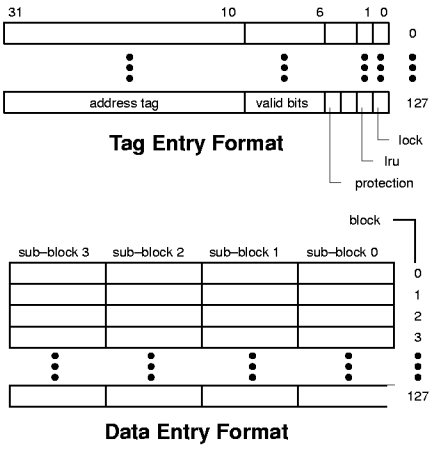


Figure 3. Instruction and Data Cache Organization

The Priority Encoder prioritizes the interrupt requests and encodes the highest–priority pending interrupt that is not masked. IRQ15 has the highest priority, and IRQ1 the lowest.

The IRL Latch captures the coded interrupt level number that is generated by the Priority Encoder.

The IRL Mask logic allows masking of all interrupt requests by forcing the encoded interrupt level asserted to the CPU to 0. The processor can still poll for pending interrupts by reading the Request Sense register even if the interrupt level is masked. The processor controls interrupt level masking by writing to the Mask register.

TIMERS

The MB86931 features four independent general–purpose 16–bit timers that can be independently programmed to operate in one of the following five modes:

- Mode 0 – Periodic Interrupt Mode
- Mode 1 – Time–out Interrupt Mode
- Mode 2 – Square Wave Generator Mode
- Mode 3 – Software Trigger Watchdog Mode
- Mode 4 – External Trigger Watchdog Mode.

Timer 0 and Timer 1 have clock prescalers that can be independently clocked by the internal clock, or by asynchronous external clocks (ACKx). The timers themselves can be independently clocked by the prescaler clock (PRSCKx), by an external asynchronous clock (CLKx), or by the internal clock.

Timer 2 and Timer 3 have no clock prescalers but can be clocked by external asynchronous clocks (CLKx), or by the internal clock.

Figure 5 shows a block diagram of the timers and prescalers, and their clock options. The external prescaler clocks are labeled ACKx, the prescaler output clocks are labeled PRSCKx, and the external timer clocks are labeled CLKx. Note that the asynchronous external clocks are synchronized internally with the internal clock.

SERIAL PORTS

The MB86931 features two independent serial communication units designated SDTR0 and SDTR1. The SDTRs support synchronous and asynchronous data transfer modes, and are program–compatible with existing industry–standard serial communication devices.

Each SDTR supports the following synchronous mode features:

- 5 to 8 bit data character lengths
- Parity option
- One (MONOSYNC) or two (BYSYNC) synchronizing characters

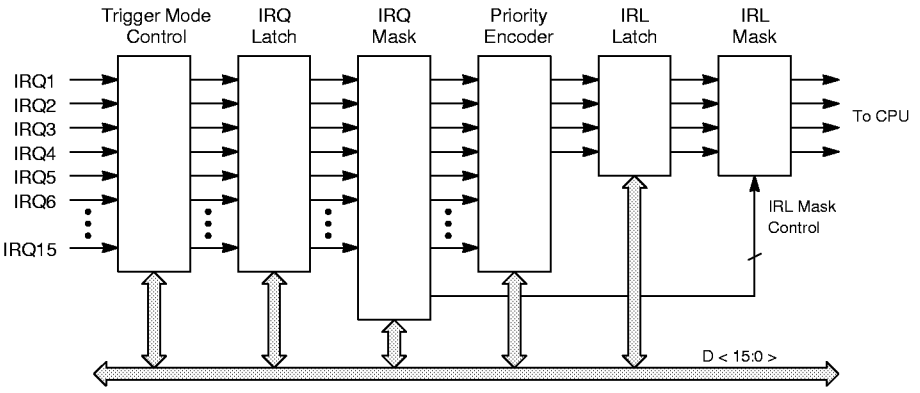


Figure 4. IRC Block Diagram

Each SDTR supports the following asynchronous mode features:

- 5 to 8 bit data character lengths
- Parity and stop bit options
- Parity, overrun, and framing error detection
- Divide by 16 or 64 clock options.
- 1, 1.5, or 2 bit length option for stop bit
- Break detection.

The SDTR transmitters and receivers are double buffered and operate independently to allow full–duplex operation. The transmit/receive clock can be externally generated, or internally generated by an MB86931 timer. Each SDTR features handshaking signals for modem control.

Figure 6 shows a block diagram of an SDTR.

BUS INTERFACE

The Bus Interface Unit (BIU) is designed to simplify the interface between the MB86931 and the rest of the system. Separate address and data buses make it easy to build fast systems. At the same time, on–chip circuitry allows these systems to be built with a minimum of external hardware.

The bus interface supports fully programmable wait state generation, address decoding with chip select outputs, same page detection to support page–mode DRAM, and an auto–reload timer to support a refresh counter.

CLOCK GENERATOR

The on–chip clock generator provides a means to directly connect the MB86931 to either a crystal oscillator or an external clock source. For either case, the external frequency is the same as the chip operating frequency.

A clock output signal provides the system with a reference by which external timing can be synchronized when not using an external clock source. The skew between the internal clock and an external input clock source is minimized by the inclusion of an on–chip phase lock loop circuit.

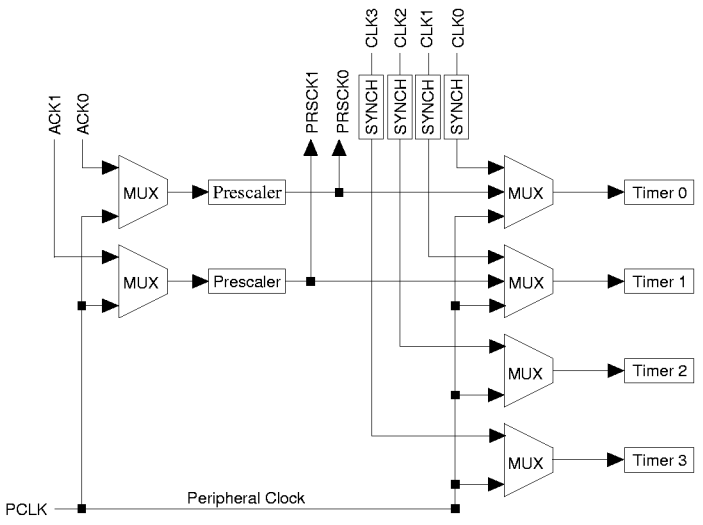


Figure 5. Timer / Prescaler Block Diagram

Note: If one wants to use the prescaler output clock for the timer input clock when the prescaler is in external clock mode, he should set the timer to external clock mode and connect PRSCK and CLKx pins externally.

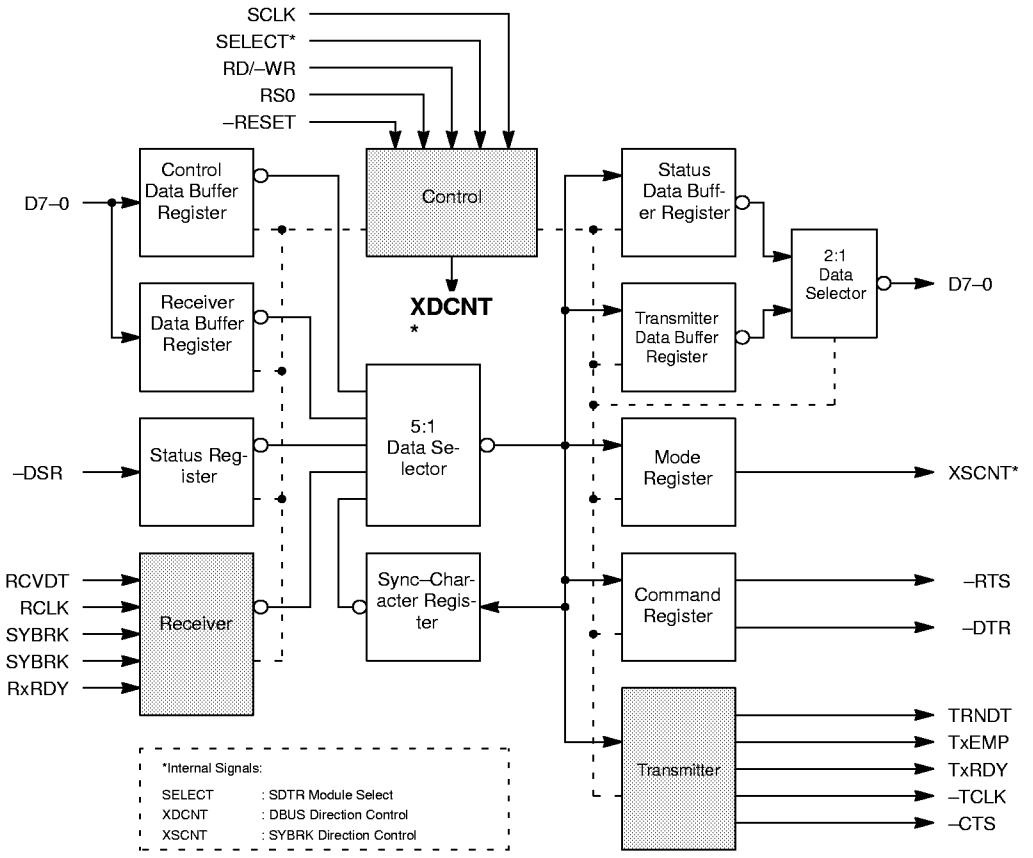


Figure 6. SDTR Block Diagram

TABLE 1. MB86931 Control and Status Registers (All registers are read/write)

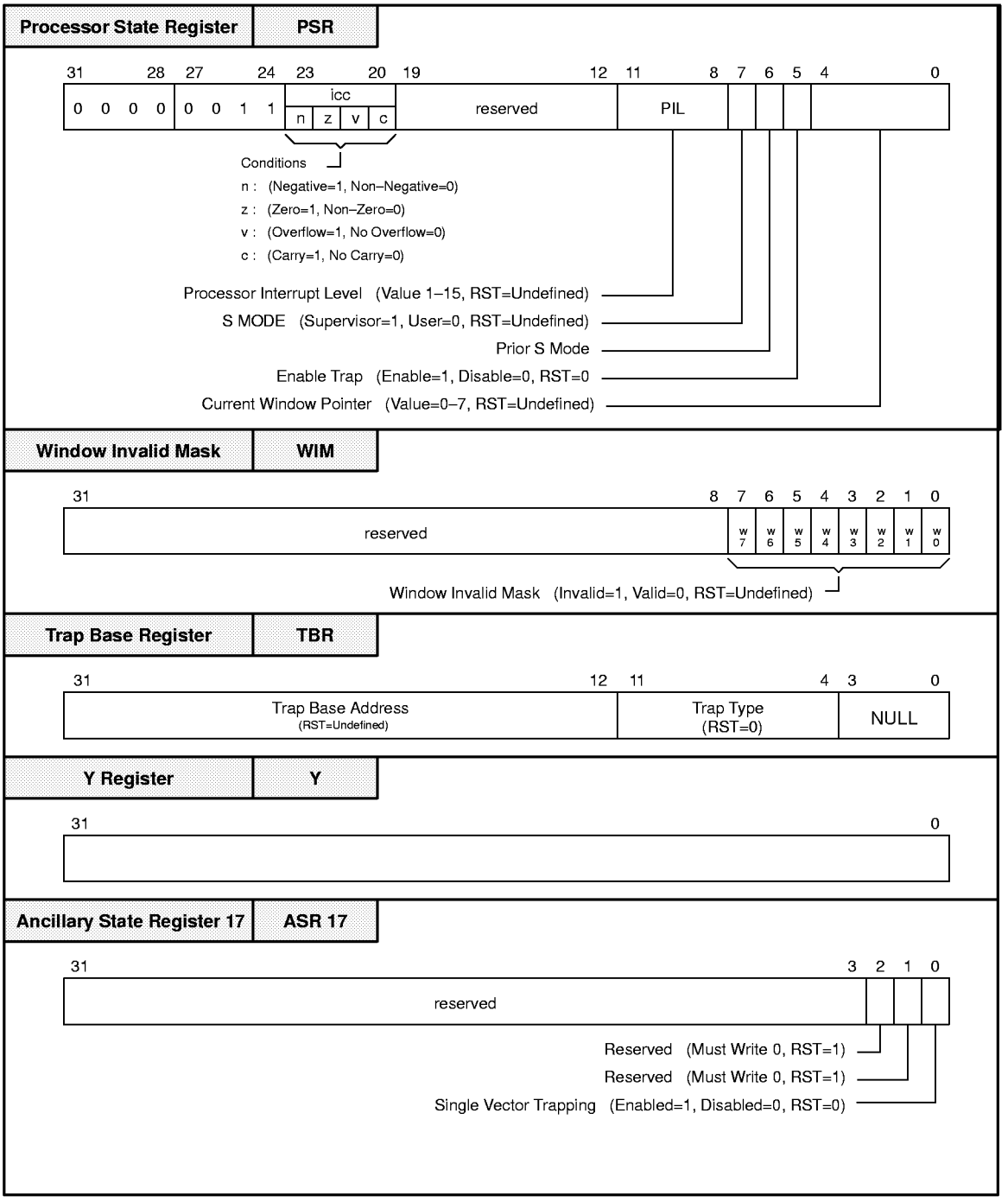
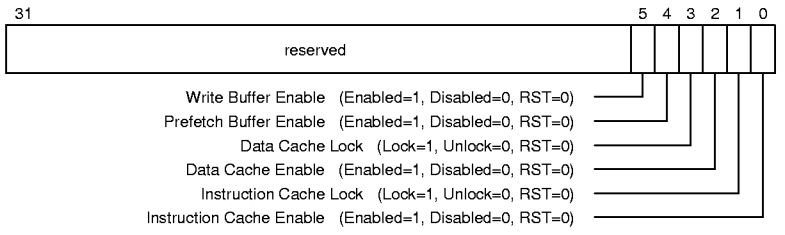
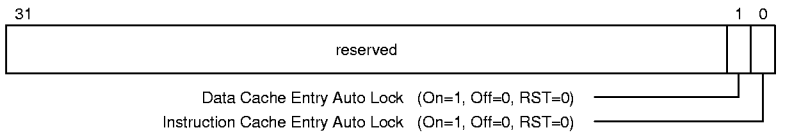


TABLE 2. MB86931 Memory Mapped Control registers (Continued)

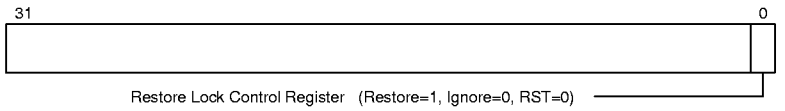
	ASI	ADDRESS
Cache/BIU Control	0x 1	0x 0000 0000



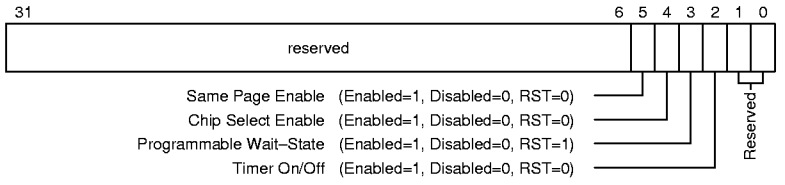
	ASI	ADDRESS
Lock Control	0x 1	0x 0000 0004



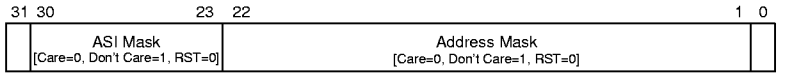
	ASI	ADDRESS
Restore Lock Control	0x 1	0x 0000 0010



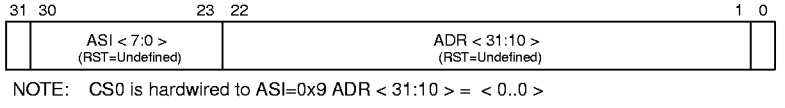
	ASI	ADDRESS
System Support Control	0x 1	0x 0000 0080



	ASI	ADDRESS
Same Page Mask	0x 1	0x 0000 0120

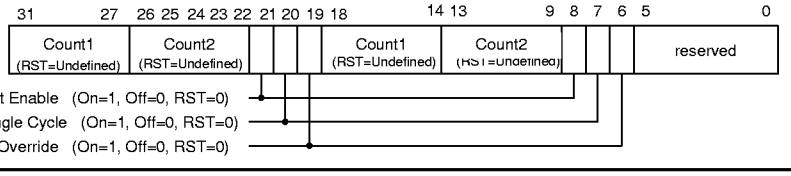


	ASI	ADDRESS
Address Range[1]	0x 1	CS1 0x 0000 0124 CS2 0x 0000 0128 CS3 0x 0000 012C CS4 0x 0000 0130 CS5 0x 0000 0134



NOTE: CS0 is hardwired to ASI=0x9 ADR < 31:10 > = < 0..0 >

	ASI	ADDRESS
Wait State Specifier	0x 1	CS1,CS0 0x 0000 0160 CS3,CS2 0x 0000 0164 CS5,CS4 0x 0000 0168

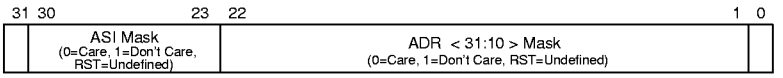


1. This register is Write Only

TABLE 2. MB86931 Memory Mapped Control Registers (Continued)

Address Mask

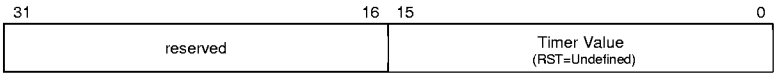
ASI	ADDRESS
0x 1	CS0 0x 0000 0140 CS1 0x 0000 0144 CS2 0x 0000 0148 CS3 0x 0000 014C CS4 0x 0000 0150 CS5 0x 0000 0154



NOTE: CS0 is hardwired to ASI=0x9; At Reset, ADR < 31:15 > = 0, ADR < 14:10 > = 1

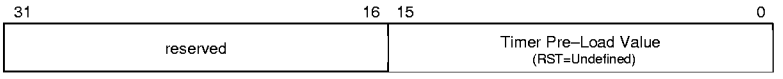
Timer

ASI	ADDRESS
0x 1	0x 0000 0174



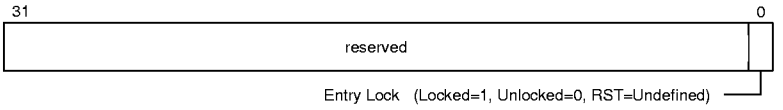
Timer Pre–Load

ASI	ADDRESS
0x 1	0x 0000 0178



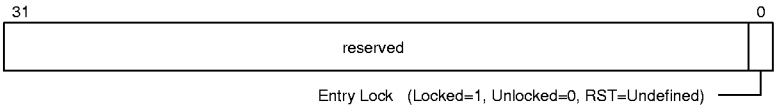
Instruction Tag Lock Bits

ASI	ADDRESS
0x 2	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400



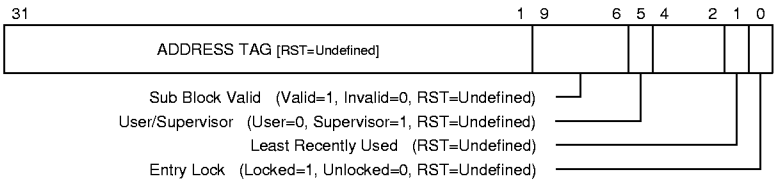
Data Tag Lock Bits

ASI	ADDRESS
0x 3	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400



Instruction Cache Tag

ASI	ADDRESS
0x C	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400



Data Cache Tag

ASI	ADDRESS
0x E	Bank 1 0x 0000 0000 ↓ by 4 0x 0000 0400 Bank 2 0x 8000 0000 ↓ by 4 0x 8000 0400

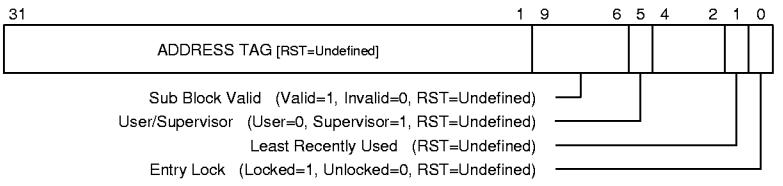


TABLE 2. MB86931 Memory Mapped Control Registers (Continued)

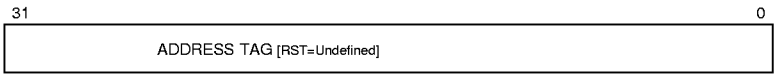
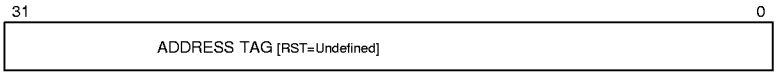
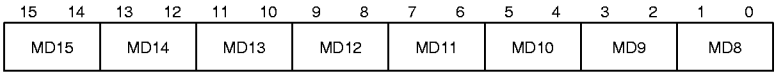
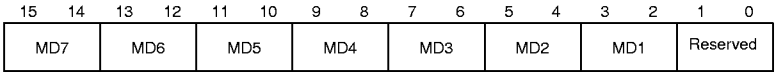
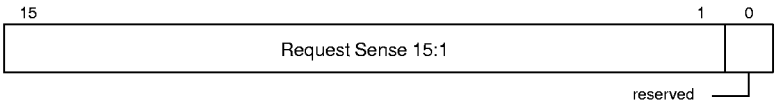
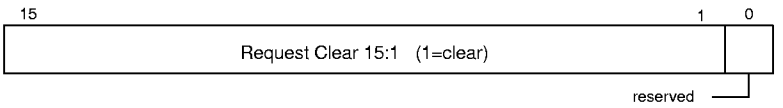
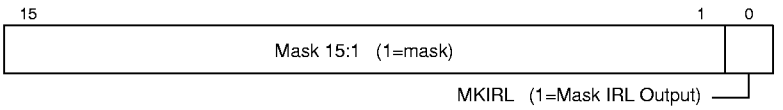
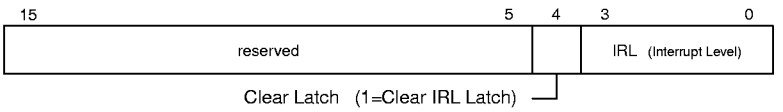
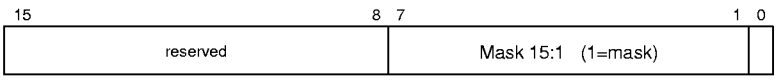
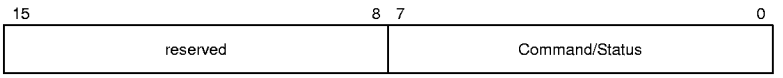
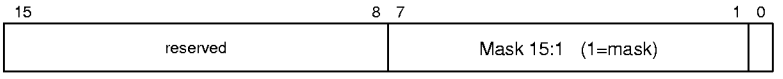
Instruction Cache Data **ASI**: 0x D **ADDRESS**: Bank 1 0x 0000 0000 ↓ by 1 word 0x 0000 0400; Bank 2 0x 8000 0000 ↓ by 1 word 0x 8000 0400	
Data Cache Data **ASI**: 0x F **ADDRESS**: Bank 1 0x 0000 0000 ↓ by 1 word 0x 0000 0400; Bank 2 0x 8000 0000 ↓ by 1 word 0x 8000 0400	
Trigger Mode 0 **ASI**: 0x 1 **ADDRESS**: 0x 0000 0200	
Trigger Mode 1 **ASI**: 0x 1 **ADDRESS**: 0x 0000 0204	
Request Sense[2] **ASI**: 0x 1 **ADDRESS**: 0x 0000 0208	
Request Clear[1] **ASI**: 0x 1 **ADDRESS**: 0x 0000 020C	
Mask **ASI**: 0x 1 **ADDRESS**: 0x 0000 0210	
Latch Clear **ASI**: 0x 1 **ADDRESS**: 0x 0000 0214	
SDTR Data 0 **ASI**: 0x 1 **ADDRESS**: 0x 0000 0220	

TABLE 2. MB86931 Memory Mapped Control Registers (Continued)

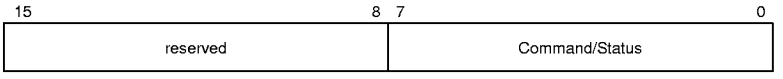
	ASI	ADDRESS
SDTR Command/Status 0	0x 1	0x 0000 0224



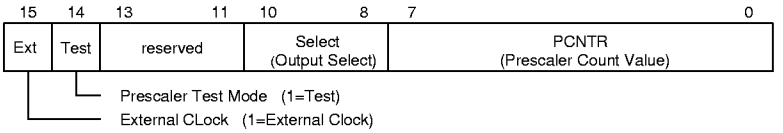
	ASI	ADDRESS
SDTR Data 1	0x 1	0x 0000 0230



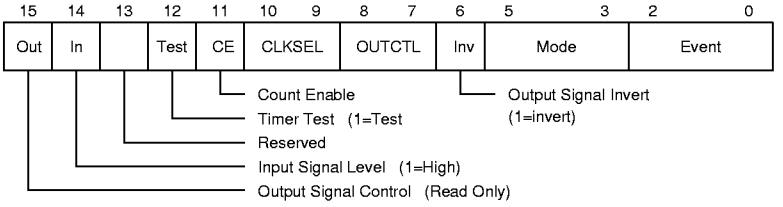
	ASI	ADDRESS
SDTR Command/Status 1	0x 1	0x 0000 0234



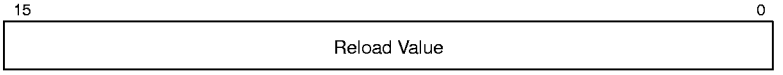
	ASI	ADDRESS
Prescaler 0	0x 1	0x 0000 0240



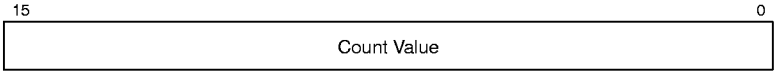
	ASI	ADDRESS
Timer Control 0	0x 1	0x 0000 0244



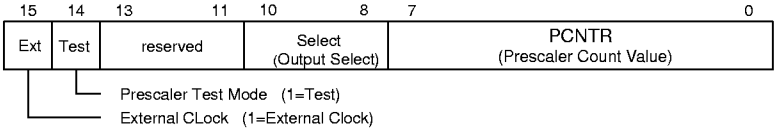
	ASI	ADDRESS
Reload 0	0x 1	0x 0000 0248



	ASI	ADDRESS
Count 0[1]	0x 1	0x 0000 024C



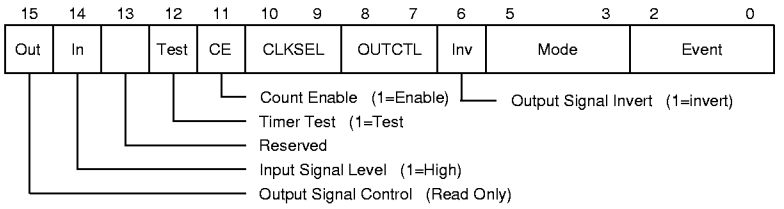
	ASI	ADDRESS
Prescaler 1	0x 1	0x 0000 0250



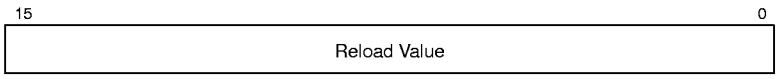
1. This register is Write Only.
2. This register is Read Only.

TABLE 2. MB86931 Memory Mapped Control Registers (Continued)

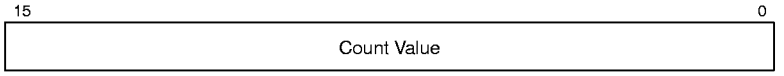
Timer Control 1	
ASI	**ADDRESS**
0x 1	0x 0000 0254



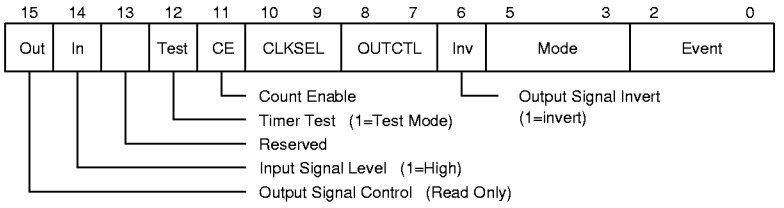
Reload 1	
ASI	**ADDRESS**
0x 1	0x 0000 0258



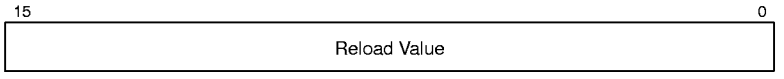
Count 1[1]	
ASI	**ADDRESS**
0x 1	0x 0000 025C



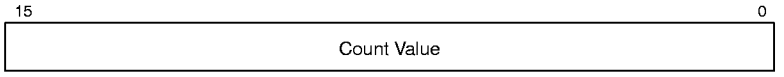
Timer Control 2	
ASI	**ADDRESS**
0x 1	0x 0000 0264



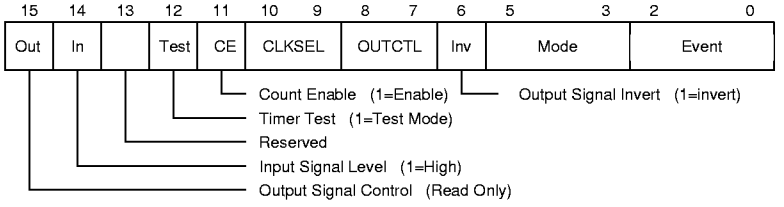
Reload 2	
ASI	**ADDRESS**
0x 1	0x 0000 0268



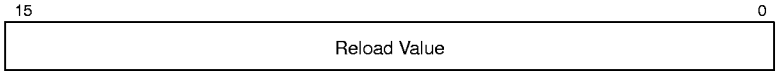
Count 2[1]	
ASI	**ADDRESS**
0x 1	0x 0000 026C



Timer Control 3	
ASI	**ADDRESS**
0x 1	0x 0000 0274



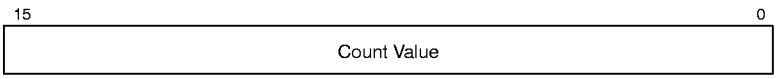
Reload 3	
ASI	**ADDRESS**
0x 1	0x 0000 0278



1. This register is Read Only.

TABLE 2. MB86931 Memory Mapped Control Registers (Continued)

Count 3[1]	
ASI	**ADDRESS**
0x 1	0x 0000 027C



1. This register is Read Only.

BUS OPERATION

The Bus Interface Unit (BIU) has the logic which allows the MB86931 to interface with the system. The system interface is made up of the address and data buses, the interrupt request bus and various control signals. The BIU is either handling requests for external memory operations, arbitrating for bus access, or idle.

Operation of the BIU

The BIU receives requests for external memory operations from the Cache Control Logic (CCL). In the case of reads from external memory, it performs the read operation and returns the data to the Cache and IU. A parallel path is used to make the data available to the IU in the same cycle that it is written to the cache.

In the case of a write to external memory, the BIU makes use of a write buffer which can hold a one word write transaction. When the BIU receives a request for a write transaction it stores the write data and address in the write buffer allowing the IU to continue operating out of on–chip cache and/or its register file. The BIU then proceeds to complete the write to external memory. In most cases the write buffer will hide external memory latency from the IU. The exceptions are in cases where the write buffer is still filled from a previous transaction or if the subsequent IU cycle results in an instruction cache miss. In these cases, IU execution is held until the write buffer is emptied.

The BIU includes a one stage prefetch buffer for instruction fetches. This buffer is used to fetch the next sequential instruction after an instruction cache miss. The instruction is prefetched only if the BIU does not have a request for a bus transaction from the IU nor is any external device requesting use of the bus. The prefetch buffer operation is suspended if the buffer is full. This occurs if the prefetched instruction is a hit in the instruction cache. The buffer restarts after another instruction cache miss. If an exception occurs during an instruction prefetch, the exception is not sent to the IU unless the instruction is actually requested by the IU. The prefetch buffer operates only when the instruction cache is on.

In any cycle the BIU can receive a request for accesses to either or both instruction and/or data memory. If it receives a request for both in the same cycle, it completes the data memory transaction first.

Exception Handling

The external memory system can indicate an exception during a memory operation. The BIU signals the appropriate data or instruction exception to the IU which will trap accordingly.

As mentioned above, the IU can continue operation after putting the data and address for a store in the write buffer. If an exception is detected while completing this buffered write, then the BIU indicates a data access exception to the IU.

Any system which needs to recover from this error should store the address and data of such write transactions in hardware. If the system can generate both read and write exceptions, then the system must also provide a status bit which indicates whether the exception was generated on a read or on a write transaction. With access to this information the data access exception service routine can determine the cause of the exception and recover accordingly.

Bus Cycles

Timings 1 through 9 illustrate representative combinations of bus cycles.

Load

Whenever an instruction fetch or a load from data memory has a miss in the cache, the BIU performs a read from external memory.

A read transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one cycle. At the same time the ADR < 31:2 > and ASI < 7:0 > bits are driven with the location to be read. The BIU drives the RD/–WR signal high to indicate a read transaction.

The external memory system responds with the read data on pins D < 31:0 >. It also asserts the –READY signal when the data is ready. For slow memory, the –READY signal can be delayed until data is valid.

A load double operation is treated as back–to–back reads.

Load with Exception

If the external memory system sees a memory exception it can terminate the current memory transaction by asserting the –MEXC and –READY signals. The data on the data bus is ignored by the MB86931.

Store

A write transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one phase. At the same time the ADR < 31:2 > and ASI < 7:0 > pins are driven with the location to be written while the D < 31:0 > pins has corresponding write data. The –BE0–3 pins indicate byte, half–word or word transaction width. The BIU drives the RD/–WR signal low to indicate a write transaction.

The external memory system responds by asserting the –READY signal when it has stored the data.

A store double operation is treated as back–to–back writes.

Store with Exception

If an access exception occurs on a write, the external memory system can terminate the current memory transaction by asserting the –MEXC and –READY signals. The external memory system is expected to ignore the data on the data bus in this situation.

Atomic Load Store

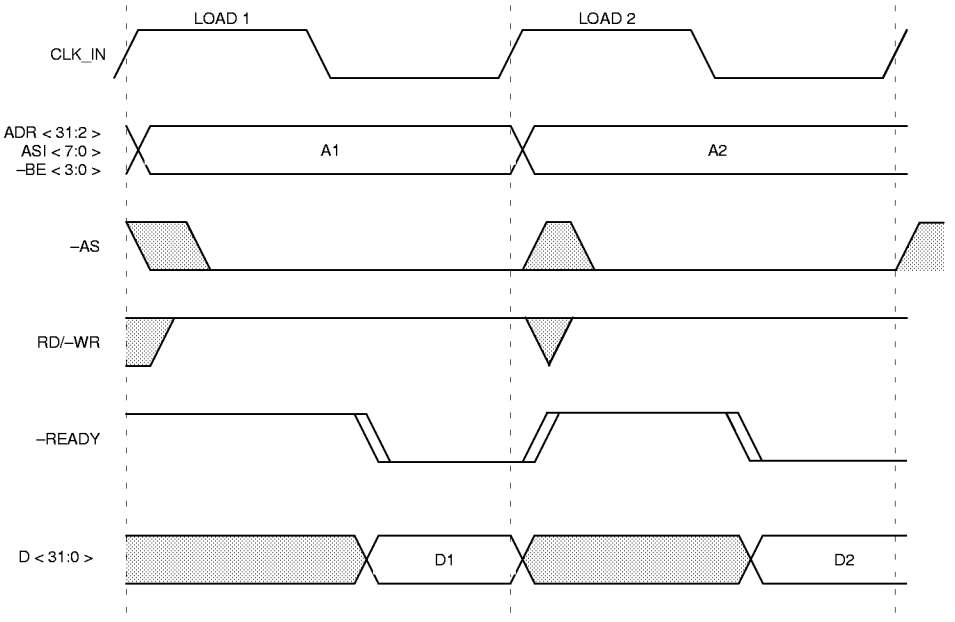
An atomic load store executes as a load followed by a store with no operation allowed in between. The –LOCK signal is asserted to indicate that the bus is being used for more than one external memory operation.

There is one cycle between the termination of the read and the beginning of the write to provide time for the switching of the data bus drivers.

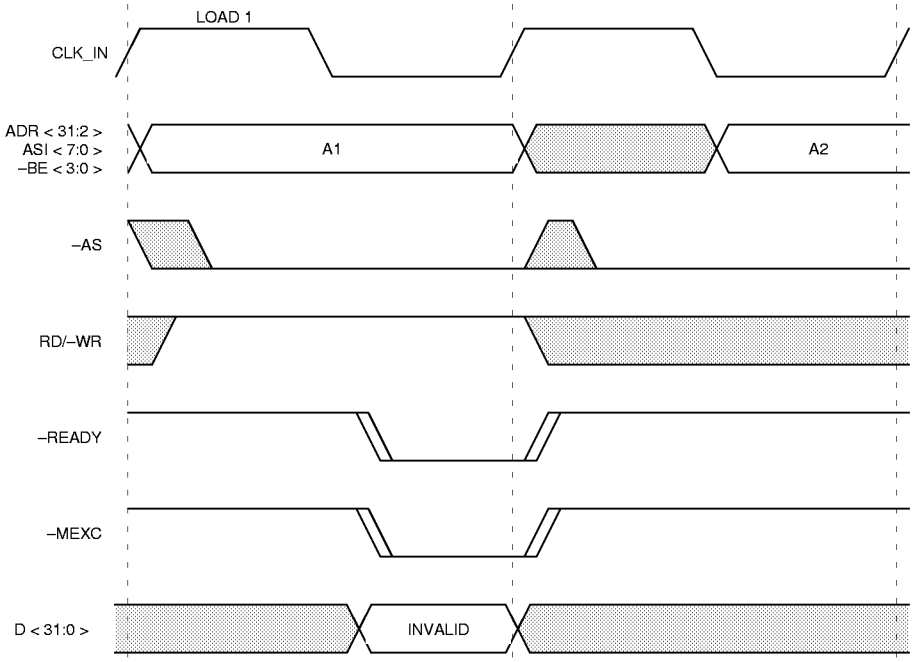
External Bus Request and Grant

Any external device can request ownership of the bus by asserting the –BREQ signal. The BIU asserts the –BGRNT signal to indicate that it is relinquishing control of the bus and also three–states all of its bus drivers. In the following cycle, the external device can complete its transaction. On completion of its transaction the external device de–asserts the –BREQ signal. The BIU responds by de–asserting the –BGRNT signal in the following cycle.

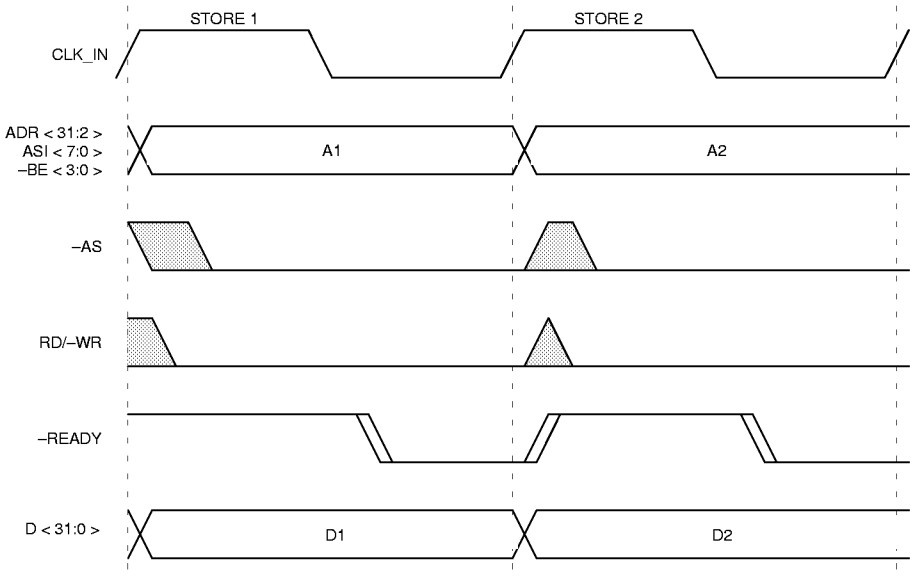
The MB86931 is the default owner of the bus.



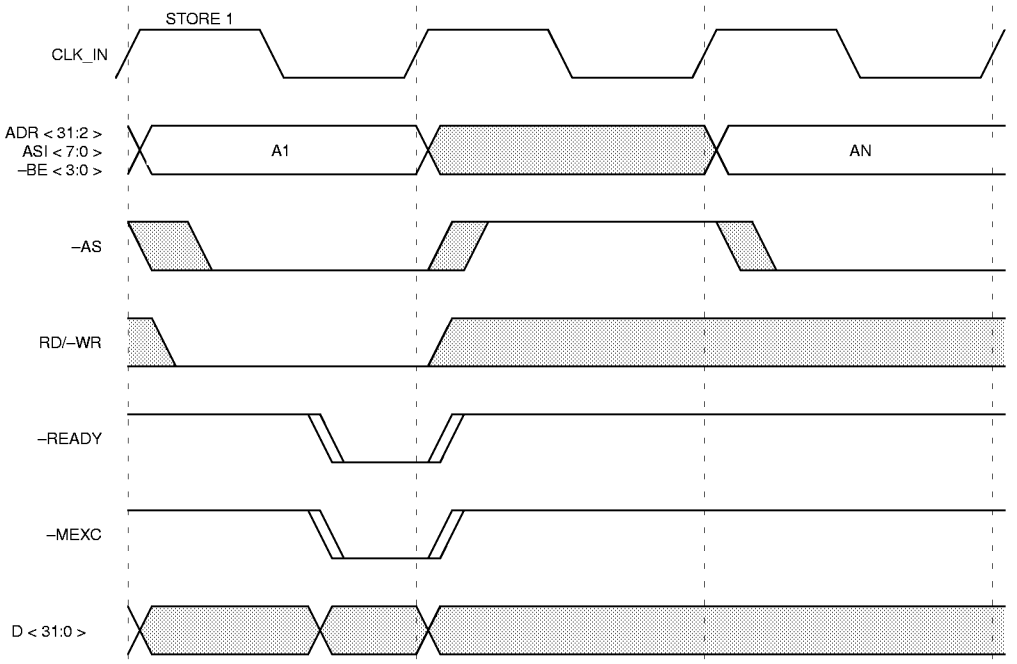
Timing 1. Typical Back-to-Back Loads (Same as Load Double)



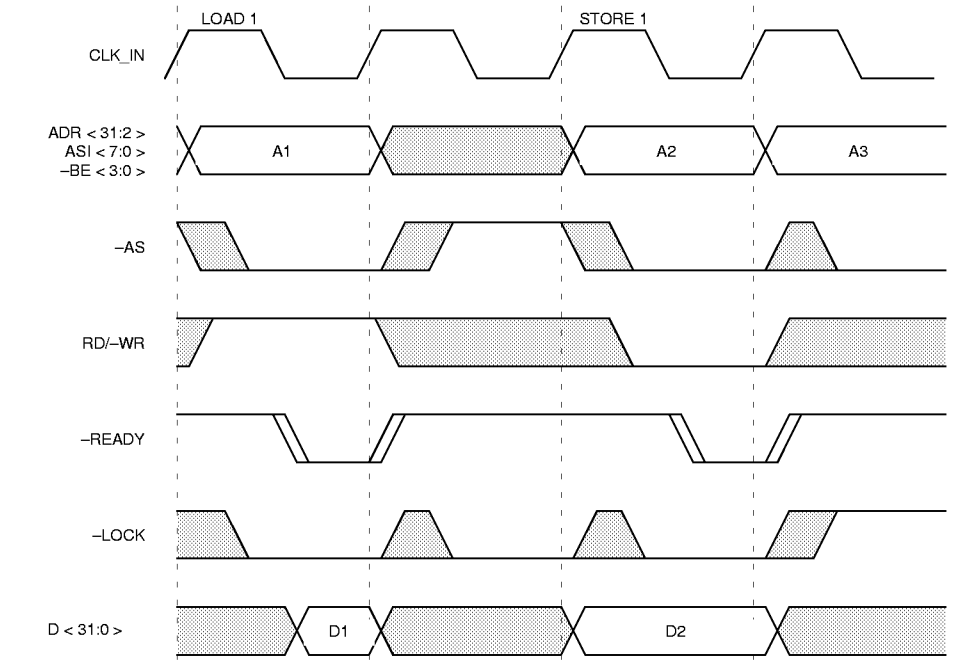
Timing 2. Load with Exception



Timing 3. Typical Back–to–Back Stores (Same as Store Double)

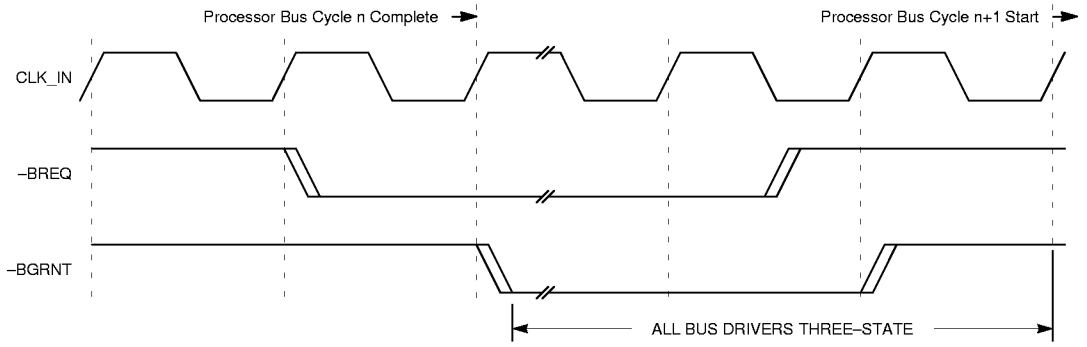


Timing 4. Store with Exception



Note: A load followed by a store requires an intervening clock cycle on the bus while a store followed by a load can occur in consecutive clock cycles.

Timing 5. Atomic Operation



Timing 6. Bus Request and Grant Cycle

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		–0.3	6	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	V
T_J	Operating junction temperature			125	°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

Recommended Connections:

1. Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every MB86931 based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "N.C." must not be connected in the system.
2. Liberal decoupling capacitance should be placed near the MB86931. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.
3. Low inductance capacitors and interconnections are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA and QFP packages will offer the lowest possible inductance.
4. For reliable operation, alternate bus masters must drive any pins that are three–stated by the MB86931 when it has granted the bus, in particular –LOCK, ADR < 31:2 >, ASI < 7:0 >, –BE0–3, D < 31:0 >, –AS, and RD/–WR must be driven by alternate bus masters. These pins are normally driven by the processor during active and idle bus states and don't require external pullups. N.C. pins must always remain unconnected.

PACKAGE THERMAL CHARACTERISTICS

Symbol	Parameter	Package	Value			Units
$\varnothing_{JC}$	Thermal resistance junction to case	256 Ceramic QFP 256 Ceramic QFP with heatsink	1.5 1.3			°C/W
			0 m/s	**1 m/s**	**3 m/s**	
$\varnothing_{JA}$	Thermal resistance junction to ambient	256 Ceramic QFP 256 Ceramic QFP with heatsink	15 12	13 9	10 5	°C/W

Note: All numbers for package thermal characteristics assume multilayer PCB.

DC SPECIFICATIONS[3] V_{CC} = 5V ± 5%

Symbol	Parameter	Conditions	Freq.	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage		–	0	–	0.8	V
V_{IH}	Input high voltage (All pins except XTAL1)		–	2.0	–	V_{CC}	V
	Input high voltage (Pin XTAL1)		–	2.8	–	V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 3.2mA	–	0	–	0.45	V
V_{OH}	Output high voltage	I_{OH} = –0.4mA	–	2.4	–	V_{CC}	V
I_{LI}	Input leakage current	V_{IN} = 0 or V_{CC}	–	–10	–	10	µA
I_{LZ}	3–state output leakage current	V_{OUT} = 0 or V_{CC}	–	–10	–	10	µA
I_{CC} *1	Operating power supply current *1 Note: Use I_{CC} (typ) values to calculate maximum case and ambient temperature allowed. Note that maximum junction temperature of die is 125°C. For example, allowed ambient temp =125°C.–(I_{CC}) · (5.25V)· $\varnothing_{JA}$		20 MHz	–	397	576	mA
			40 MHz	–	550	732	mA
C_{PIN}	Pin capacitance (All pins except XTAL2)	V_{CC} = V_I = 0 f = 1 MHz	–	–	–	13	pF
	Pin capacitance (Pin XTAL2)		–	–	–	16	pF

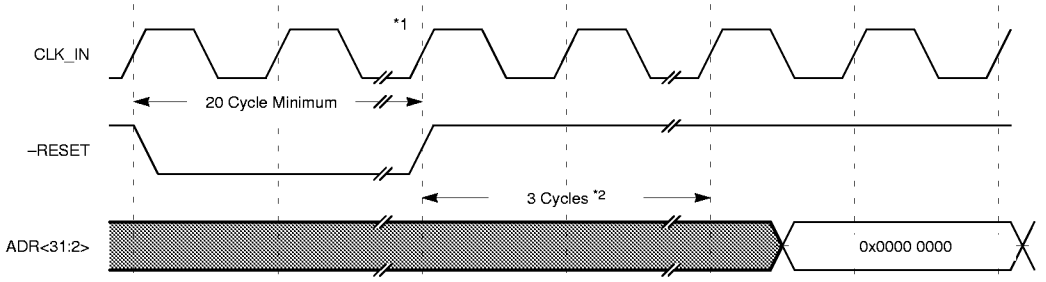
AC CHARACTERISTICS[1,2,4] V_{CC} = 5V ± 5% (Preliminary)

Symbol	Parameter Description		20 MHz		40 MHz		Units
			Min.	Max.	Min.	Max.	
t1, t_{CLK}	CLKIN period		50	100	25	100	ns
t2	CLKIN high Time		10	–	6	–	ns
t3	CLKIN low time		14	–	10	–	ns
t4	CLKIN rise time		–	4	–	2	ns
t5	CLKIN fall time		–	4	–	2	ns
t6	CLKIN to CLKOUT delay [7]		0	8	0	7	ns
t7	CLKIN to CLKOUT2 delay [7]		25	33	13	20	ns
t8	CLKOUT1, CLKOUT2 high time [7]		0.35xPeriod	–	0.25xPeriod	–	ns
t9	CLKOUT1, CLKOUT2 low time [7]		0.4xPeriod	–	0.4xPeriod	–	ns
t10	CLKOUT1, CLKOUT2 fall time [7]		–	3	–	3	ns
t11	CLKOUT1, CLKOUT2 rise time [7]		–	4	–	3	ns
t12	D < 31:0 >	Output valid delay	–	21	–	18	ns
		Output hold	2	–	2	–	
	ADR < 31:2 >	Output valid delay	–	24	–	21	ns
		Output hold	2	–	2	–	
	–BE0–3	Output valid delay	–	19	–	17	ns
		Output hold	2	–	2	–	
	ASI < 7:0 >	Output valid delay	–	22	–	18	ns
		Output hold	2	–	2	–	
t13	–CS	Output valid delay	–	24	–	21	ns
		Output hold	2	–	2	–	
t14	–SAME_PAGE	Output valid delay	–	23	–	21	ns
		Output hold	2	–	2	–	
t15	RD/–WR	Output valid delay	–	18	–	15	ns
		Output hold	2	–	2	–	
t16	–LOCK	Output valid delay	–	19	–	17	ns
		Output hold	2	–	2	–	
t17	–AS	Output valid delay	–	21	–	18	ns
		Output hold	2	–	2	–	
t18	–TIMER_OVF	Output valid delay	–	20	–	18	ns
		Output hold	2	–	2	–	

AC CHARACTERISTICS[1,2,4] V_{CC} = 5V ± 5% (Preliminary)

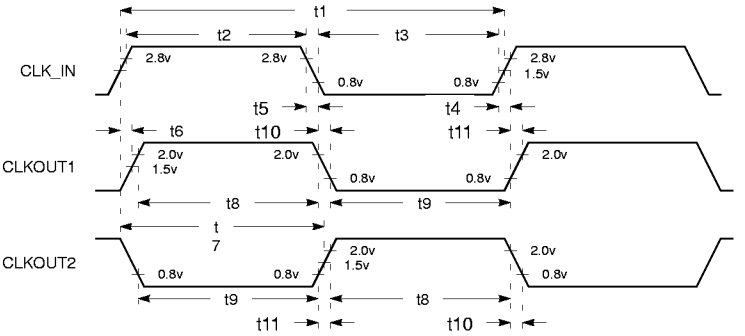
Symbol	Parameter Description		20 MHz		40 MHz		Units
			Min.	Max.	Min.	Max.	
t19	–BGRNT	Output valid delay	–	20	–	15	ns
		Output hold	2	–	2	–	ns
t20	–MEXC input setup time		14	–	12	–	ns
t21	–READY input setup time		15	–	12	–	ns
t22	D < 31:0 > input setup time		13	–	12	–	ns
t23	–BREQ input setup time		8	–	6	–	ns
t24	–MEXC input hold time		2	–	1	–	ns
t25	–READY input hold time		2	–	1	–	ns
t26	D < 31:0 > input hold time		3	–	2	–	ns
t27	–BREQ input hold time		3	–	2	–	ns

1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V (Except XTAL1 which swings from 0.4V to 3.0V). input rise and fall times are 2ns or less.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. Timing specifications apply to frequency of operation listed at top of column.
5. All output timings are based on a 50pF load.
6. Data bus output driver control is same as for RD/–WR so timing is similar.



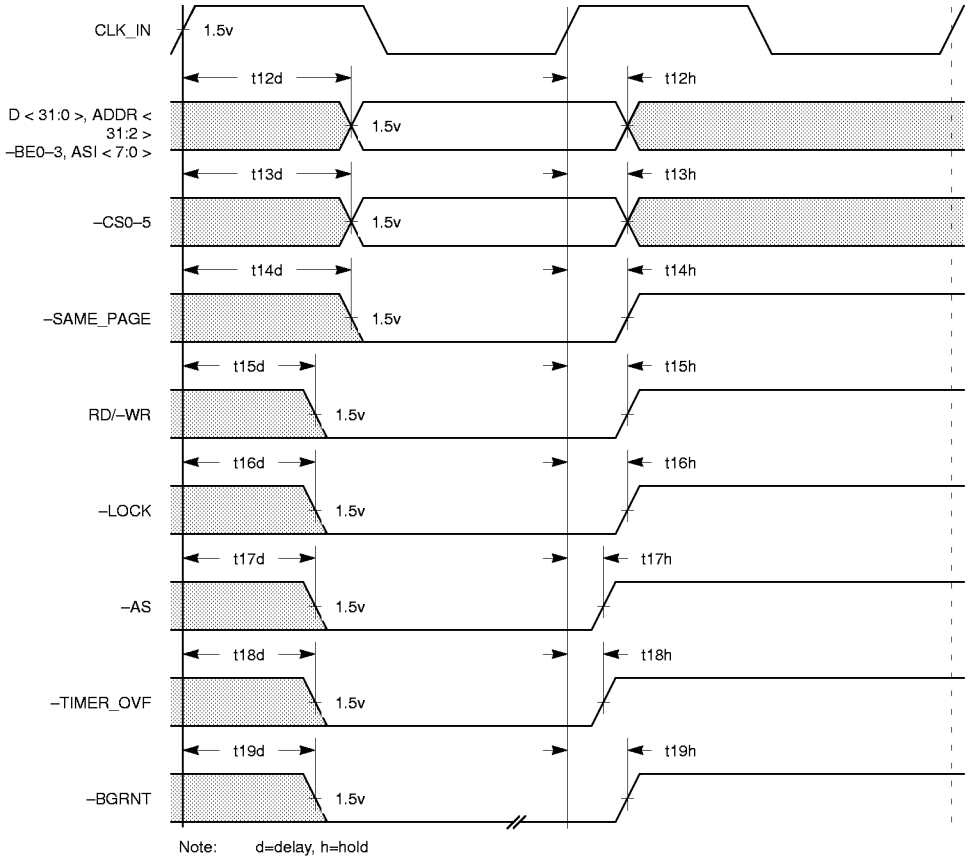
*1. CLK_IN must be stable for at least 100µs before RESET is de–asserted.
*2. When RESET hold time (3ns) is met.

Timing 7. Reset Timing



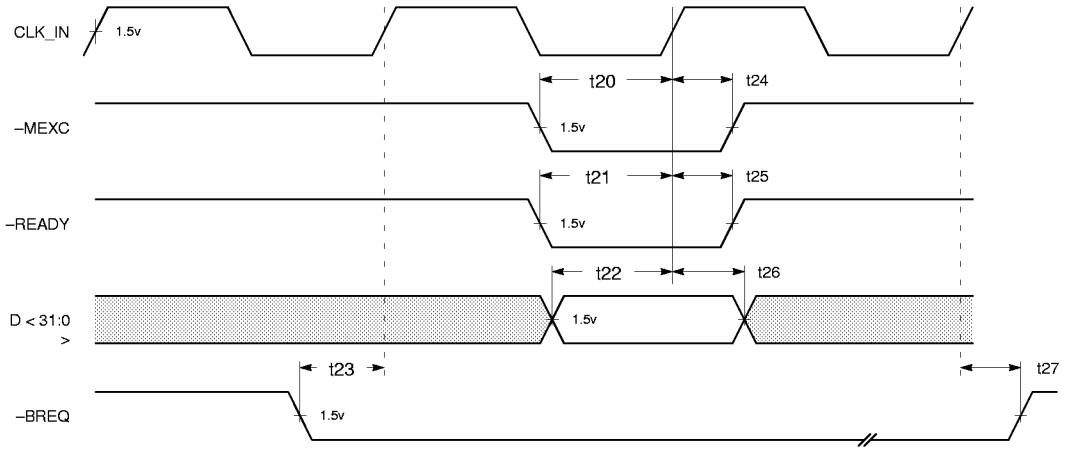
Note: CLKOUT1 and CLKOUT2 are derived from non–overlapping internal clocks, however, the relative timing of these signals is not tested.

Timing 8. Clock Timing

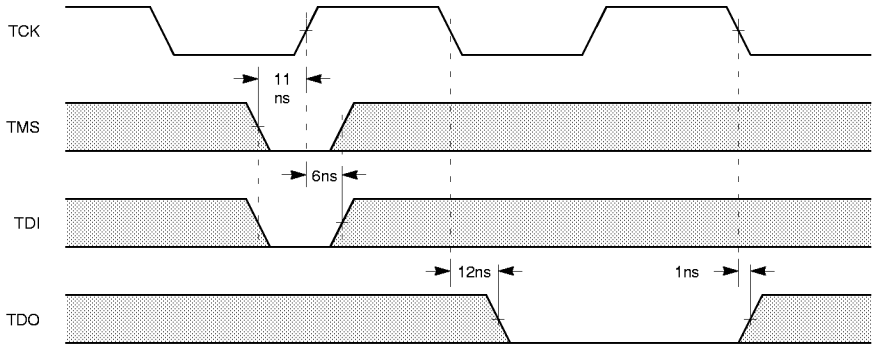


Note: d=delay, h=hold

Timing 9. I/O Output Timing



Timing 10. I/O Output Timing



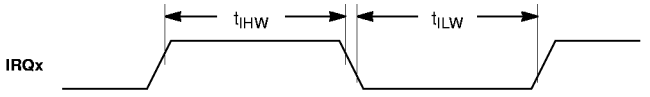
NOTE: These specifications are based on sample characterization and should be considered as typical values.

Timing 11. JTAG Timing

Interrupt Signal, Interrupt Input Width

Symbol	Description	20 MHz, 40 MHz		Unit
		Min.	Max.	
T_{IHW}	IRQ input High level duration [1]	6 t_{CLK}+10	–	ns
T_{ILW}	IRQ input Low level duration [2]	6 t_{CLK}+10	–	ns

1. In HIGH Level or RISING–EDGE trigger mode, if this width is satisfied, the interrupt request FLIP–FLOP is set.
2. In LOW Level or FALLING–EDGE trigger mode, if this width is satisfied, the interrupt request FLIP–FLOP is set.

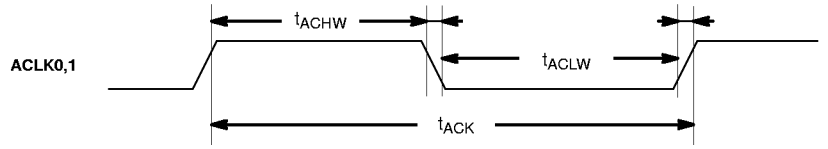


Timing 12. Interrupt Request Timing Diagram

Prescaler Inputs

Symbol	Item	20MHz, 40MHz		Unit
		Min	Max	ns
tACK	Prescaler input clock cycle	50	—	ns
tACHW	Prescaler input clock H duration	22	—	ns
tACLW	Prescaler input clock L duration	22	—	ns
tACR	Prescaler input clock rise time	—	5	ns
tACF	Prescaler input clock fall time	—	5	ns

1. Applicable when the prescaler is in the external clock mode.



Timing 13. Prescaler Input Clock Timing Diagram

Prescaler Outputs

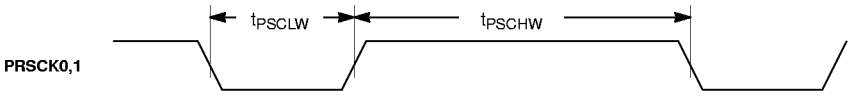
Symbol	Item	20MHz, 40MHz		Unit
		Min	Max	
tPSCLW	Prescaler output "L" Width *1, *3, *4	1		tPCK
tPSCHW	Prescaler output "H" Width *1, *3, *4	N–1		tPCK
tPSCLW	Prescaler output "L" Width *2, *3, *4	$N \cdot 2^{M-1}$		tPCK
tPSCHW	Prescaler output "H" Width *2, *3, *4	$N \cdot 2^{M-1}$		tPCK

*1. When the SELECT field of prescaler registers is "0".

*2. When the SELECT field of prescaler registers is "non–0" M is the value programmed on SELECT field of prescaler register. N is the value programmed on PRESCALE VALUE field of prescaler register.

*3. PRSCKx outputs are fixed to "L" when PRESCALE VALUE field is programmed as "1".

*4. tPCK is the input clock cycle of prescaler.
tPCK = 2 tCLK in internal clock mode.
tPCK = tACK in external clock mode.

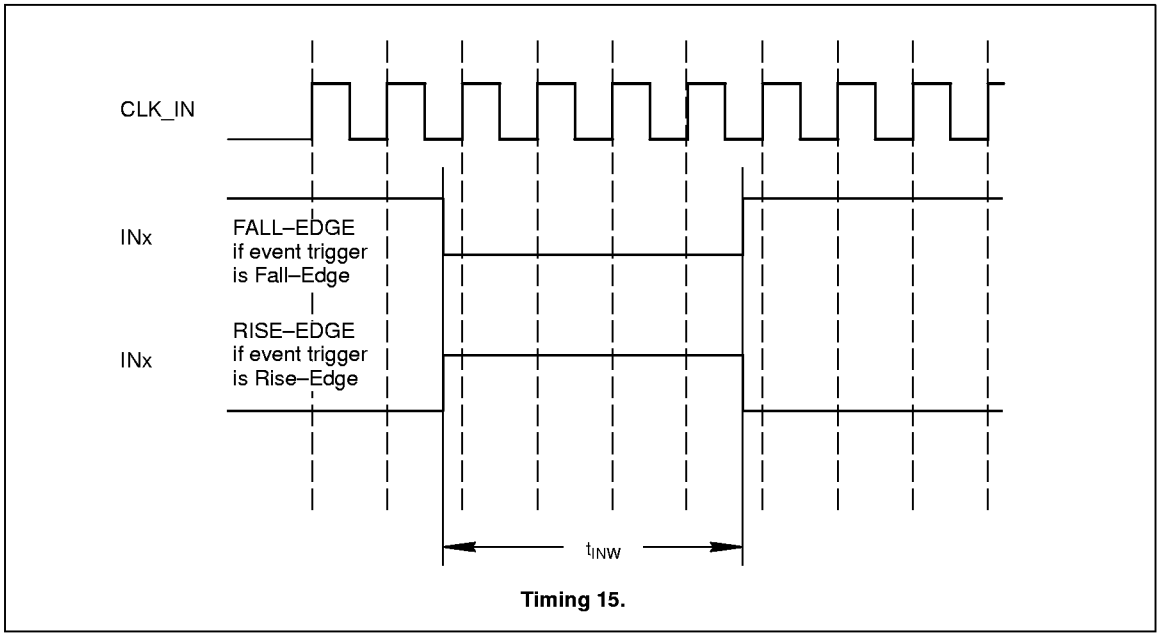


Timing 14. Prescaler Output Clock Timing Diagram

Timer: External Trigger Input

Symbol	Description	20 MHz, 40 MHz		Unit
		Min.	Max.	
T_{INW}		4	–	tCLK

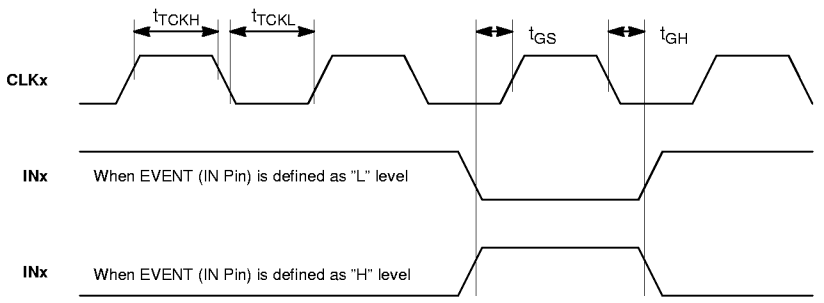
* MODE 4



Timing 15.

Timer: External Clock Mode

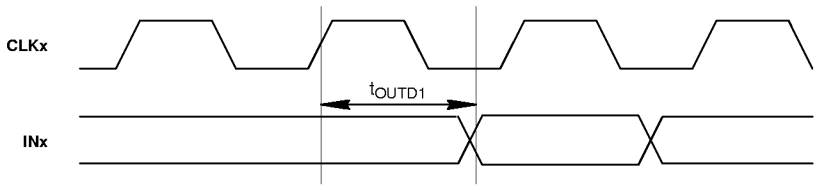
Symbol	Item	20MHz, 40MHz		Unit
		Min.	Max,	
t_{TCKH}	Width of "H" level of timer input	3	–	tCLK
t_{TCKL}	Width of "L" level of timer input	3	–	tCLK
t_{GS}	Setup time of GATE signal (IN Pin) against CLKx	10	–	ns
t_{GH}	Hold time of GATE signal (IN Pin) against CLKx	0	–	ns



Timing 16. External Clock Mode

Timer Outputs

Symbol	Item	20MHz, 40MHz		Unit
		Min.	Max,	
t_{OUTD1}	OUT Output delay against CLK_IN	–	30	ns



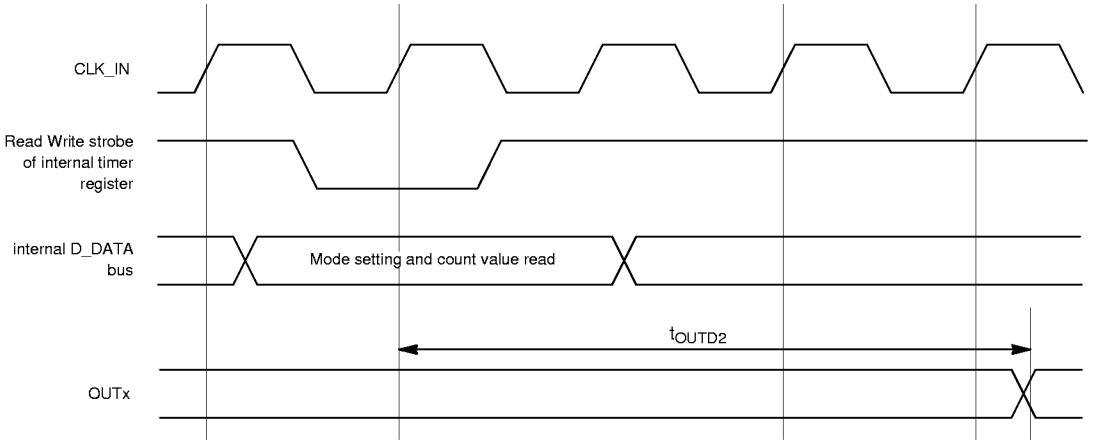
Timing 17. Timer Output

Timer Input

Symbol	Item	20MHz, 40MHz		Unit
		Min.	Max,	
t_{OUTD2}	OUT output delay	–	3 tCLK+30	ns

For the following modes:

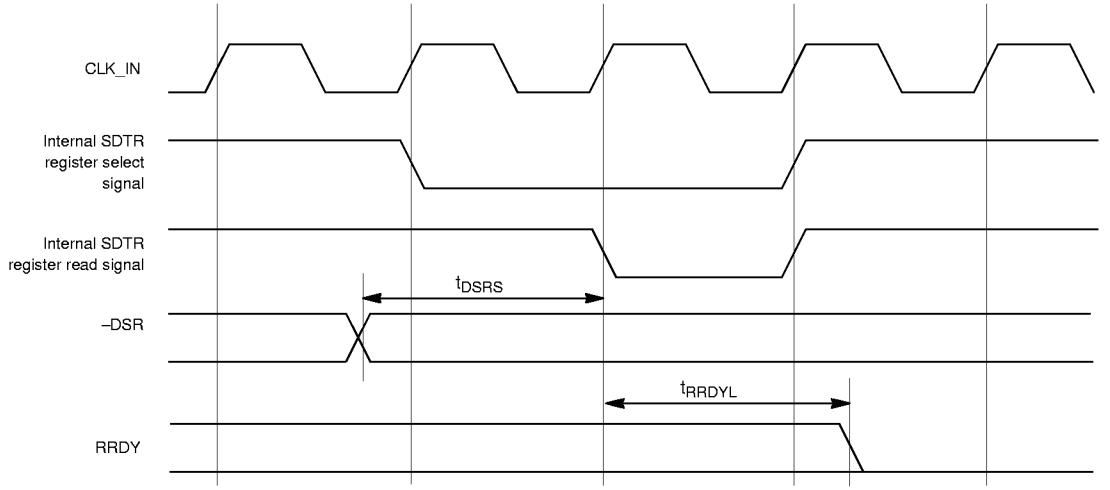
- Mode setting (write to TCR)
- After set mode 0, write "RELOAD" register / read count
- After set mode 1, write "RELOAD" register / read count
- After set mode 3, write "RELOAD" register / read count



Timing 18.

STDR Portion (–DSR, RRDY)

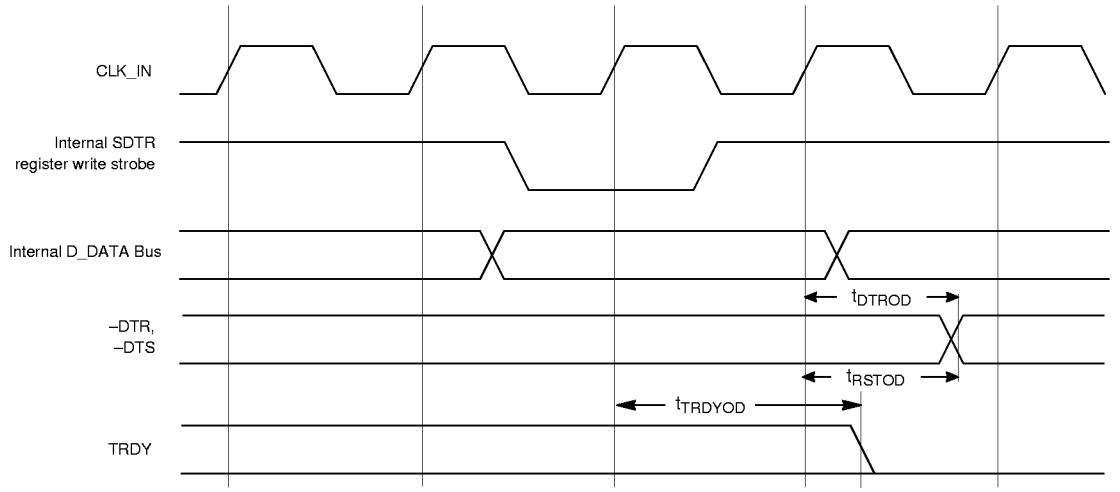
Symbol	Item	20MHz, 40MHz		Unit
		Min.	Max,	
t_{DSRS}	DSR setup time for register read	28	–	t_{CLK}
t_{RRDYL}	Time from register read to "RDDY" off	0	100	ns



Timing 19.

–DTR, –RTS, TRDY

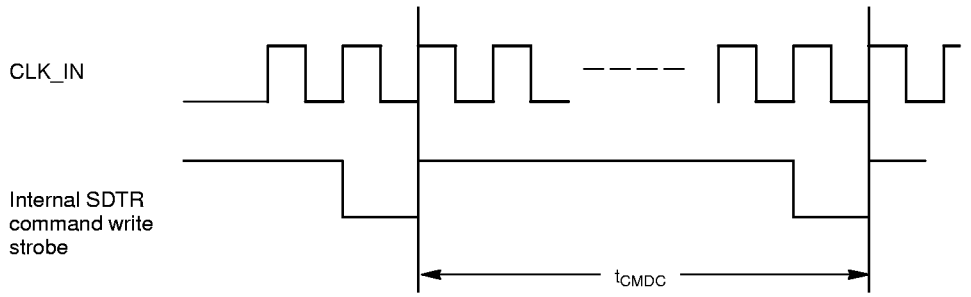
Symbol	Item	20MHz, 40MHz		Unit
		Min.	Max,	
t_{DTROD}	Delay time from register write to DTR_output	0	40	t_{CLK}
t_{RTSOD}	Delay time from register write to RTS_output	0	40	t_{CLK}
t_{TRDYOD}	Delay time from register write to TRDY output	0	100	ns



Timing 20.

Command Write cycle

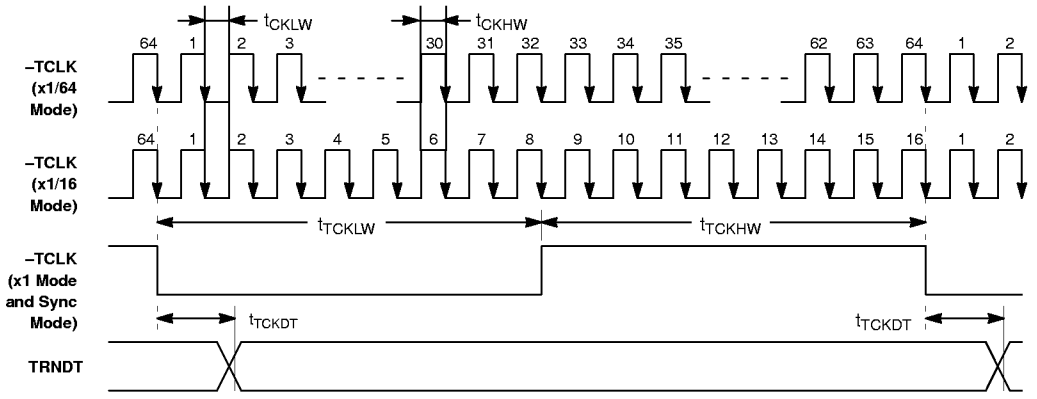
Symbol	Description	20 MHz, 40 MHz		Unit
		Min.	Max.	
T_{CMDC}	Command Write cycle time (initial setting)	14	–	tCLK
	Command Write cycle time (Asynch. Mode)	20	–	tCLK
	Command Write cycle time (Synch. Mode)	40	–	tCLK



Timing 21.

STDR Transmit Clock and Data Timing Parameters

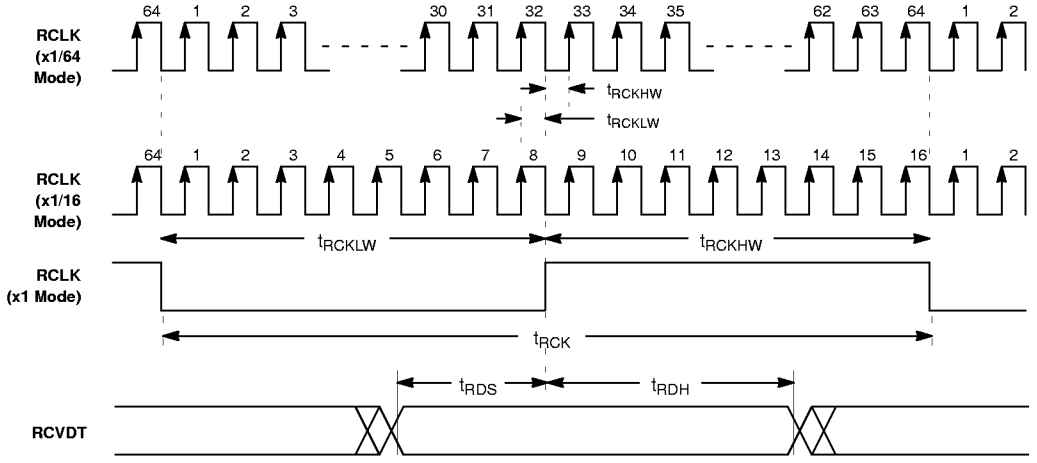
Symbol	Item	Sync Mode, 1x Mode		x1/16, x1/64 Mode		Unit
		Min.	Max.	Min.	Max	
t_{TCKHW}	Transmit clock high duration	32	–	4	–	t_{CLK}
t_{TCKLW}	Transmit clock low duration	14	–	4	–	t_{CLK}
t_{TCKDT}	Transmit clock falling to output data	0	100	0	100	ns



Timing 22. SDTR Transmit Clock and Data Timing Diagram

STDR Receive Clock and Data Timing Parameters

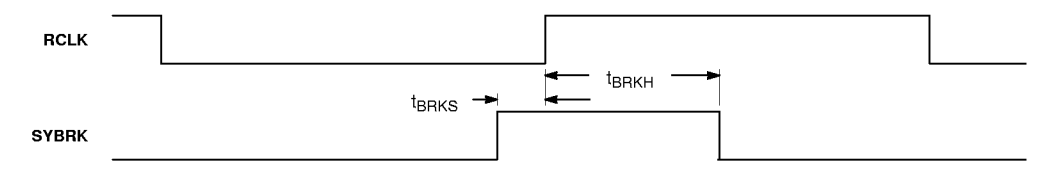
Symbol	Item	Sync Mode, 1x Mode		x1/16, x1/64 Mode		Unit
		Min.	Max.	Min.	Max.	
t_{RCK}	Receive clock cycle	62	—	8	—	t_{CLK}
t_{RCKHW}	Receive clock high duration	12	—	4	—	t_{CLK}
t_{RCKLW}	Receive clock low duration	7	—	4	—	t_{CLK}
t_{RDS}	Receive data setup time	6	—	6	—	t_{CLK}
t_{RDH}	Receive data hold time	6	—	6	—	t_{CLK}



Timing 23. STDR Receive Clock and Data Timing Diagram

SYBRK Signals Timing in the External Sync. Mode

Symbol	Item	20 MHz, 40 MHz		Unit
		Min.	Max.	
t_{BRKS}	SYBRK setup time	0	—	t_{CLK}
t_{BRKH}	SYBRK hold time	10	—	t_{CLK}



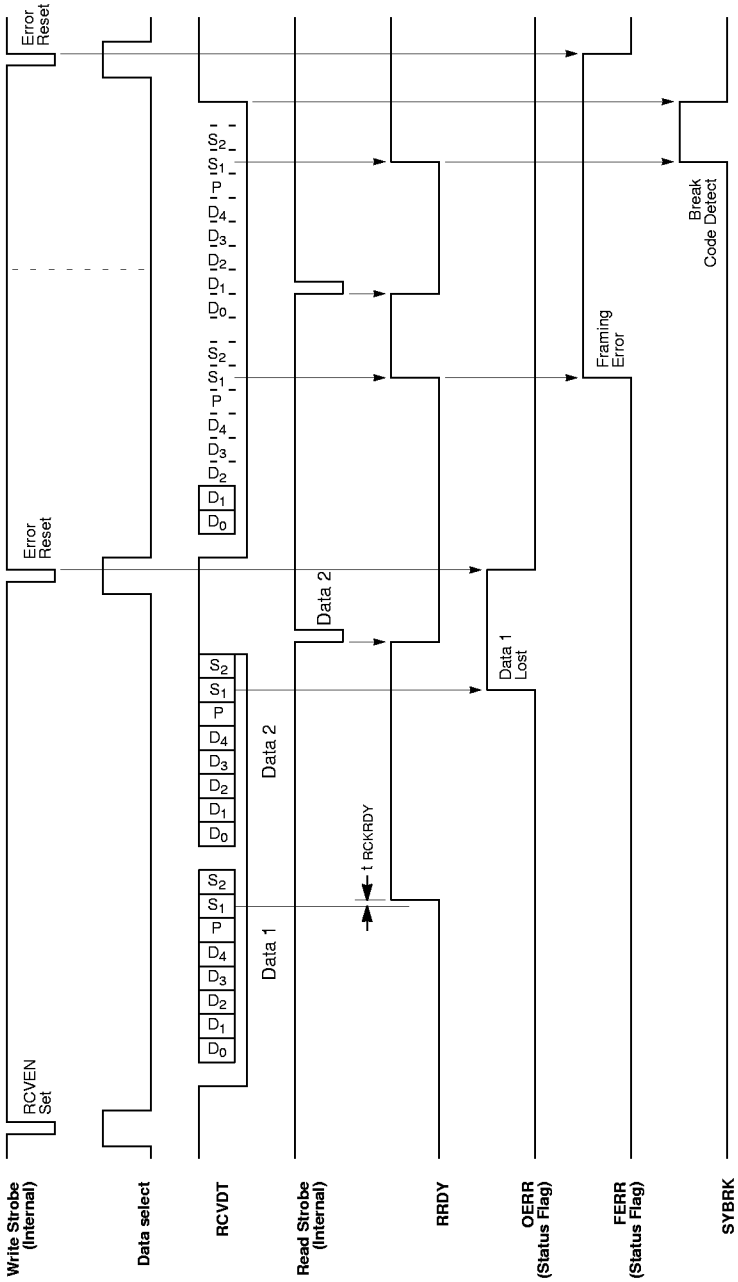
Timing 24. Break Timing Diagram

SYBRK Signals Timing in the External Sync. Mode

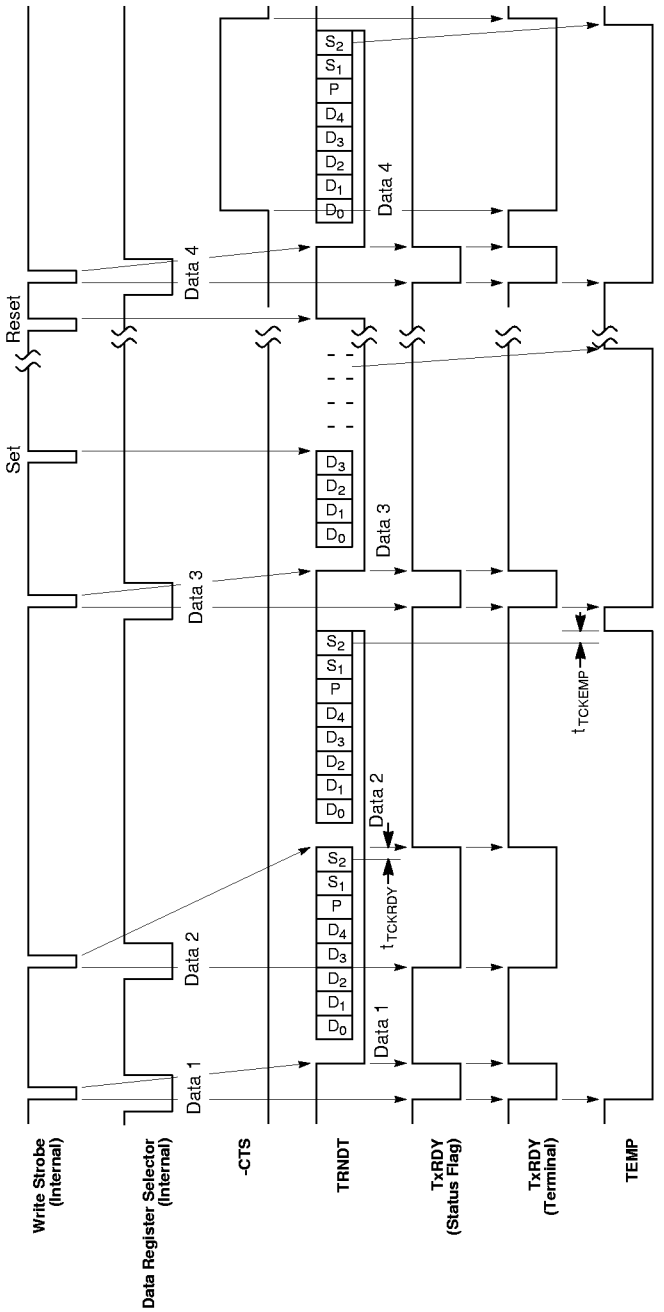
Symbol	Item	20 MHz, 40 MHz		Unit
		Min.	Max.	
t_{TCKRDY}	Delay time between TCLK rising edge (last bit) to TRDY rising edge.	—	36	t_{CLK}
t_{TCKEMP}	Delay time between TCLK rising edge (last bit) to TEMP rising edge.	—	24	t_{CLK}
t_{RCKRDY}	Delay time between RCLK rising edge (last bit) to RRDY rising edge.	—	35	t_{CLK}
t_{SYCD1}	Time from RCLK rising edge (last bit) to internal SYNC detection (SYBRK pin)	—	62	t_{CLK}
t_{SYCD2}	Time from RCLK rising edge (last bit) to internal SYNC detection (Status data buffer register)	—	70	t_{CLK}

NOTE:

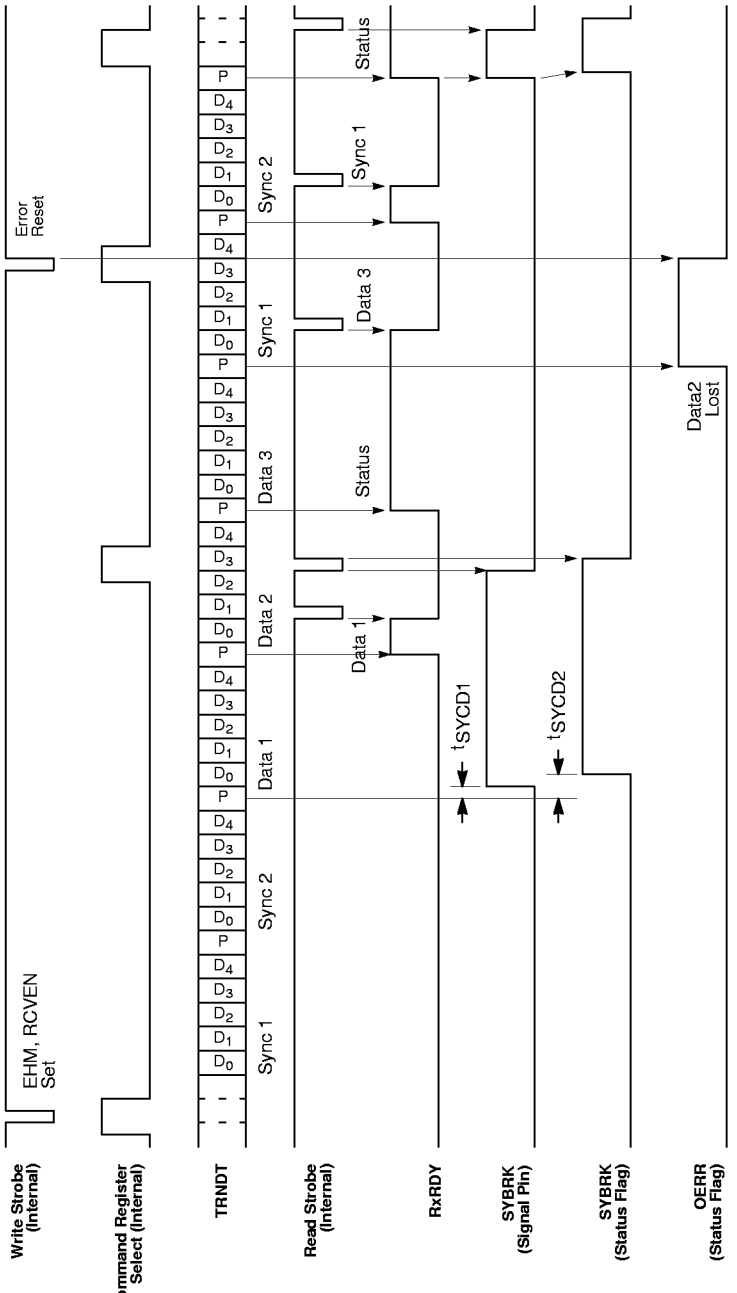
- All parameters are valid in temperature and voltage ranges if not specified.
- All voltage values are related to GND level. Timing measuring point is 1.5V, input levels are 0.4V~2.4V (XTAL1 only 0.4V~3.0V). Input rising and falling time are less than 2ns.
- Do not short the multiplier output pins for longer than 1 second.
- All AC parameters are measured in the frequencies showing on the top row.
- External loading capacitance is 50pF.



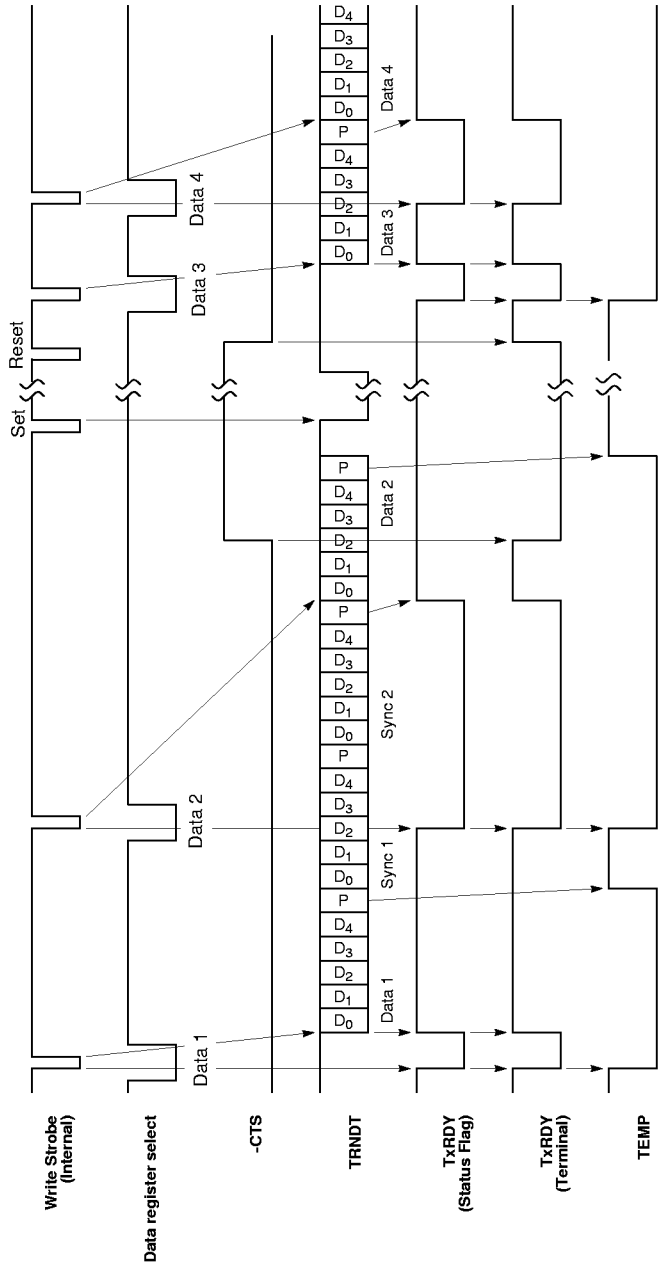
Timing 25. Receive Timing, Asynchronous Mode: data bits length 5 bit, with parity, stop bits length 2 bits



Timing 26. Transmit Timing, Asynchronous mode: data bits length 6 bits, w/o parity, stop bits length 2 bits.

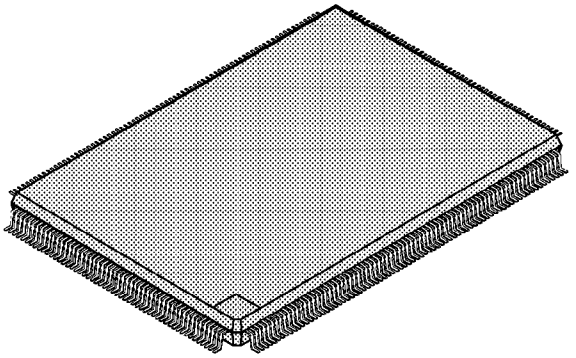


Timing 27. Receiver Timing (Internal synch. mode, 5–bit char., bi–synch. mode)



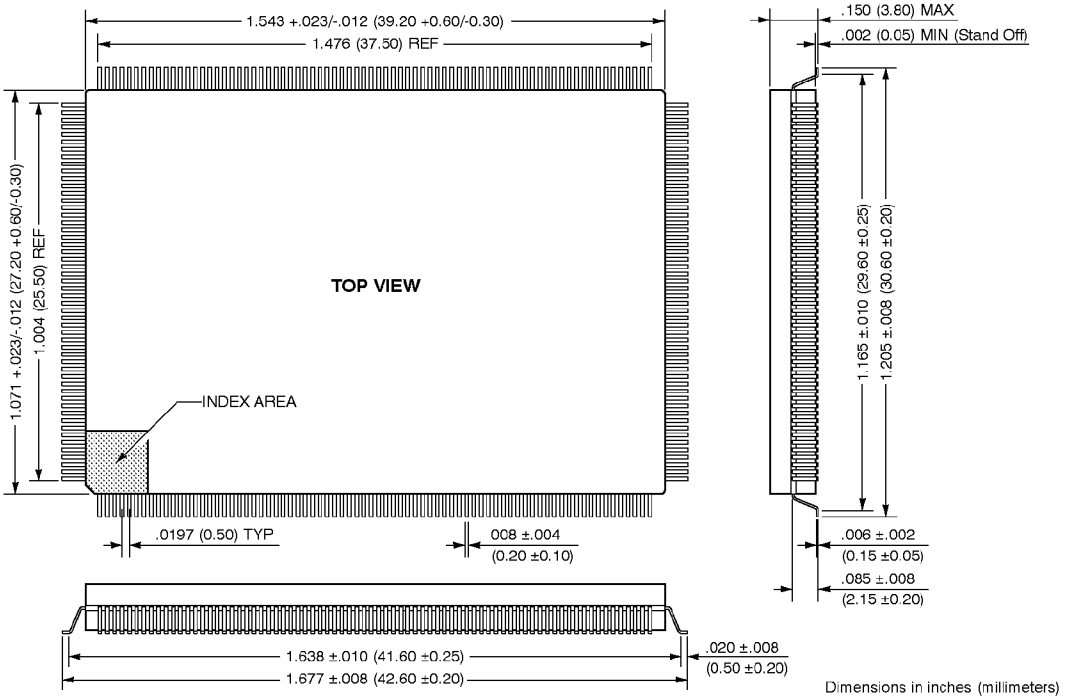
Timing 28. Transmitter Timing 2 (Asynch. mode: 5–bit char., parity, bisynch. mode)

256-PIN FLAT PACKAGE

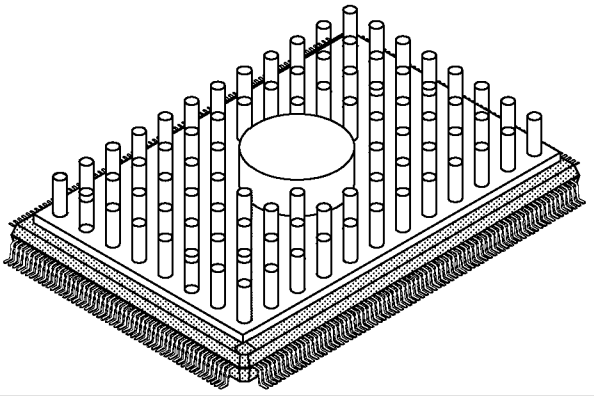


Ordering Info: MB86931-20ZF-G

256-LEAD FLAT PACKAGE (CQFP)

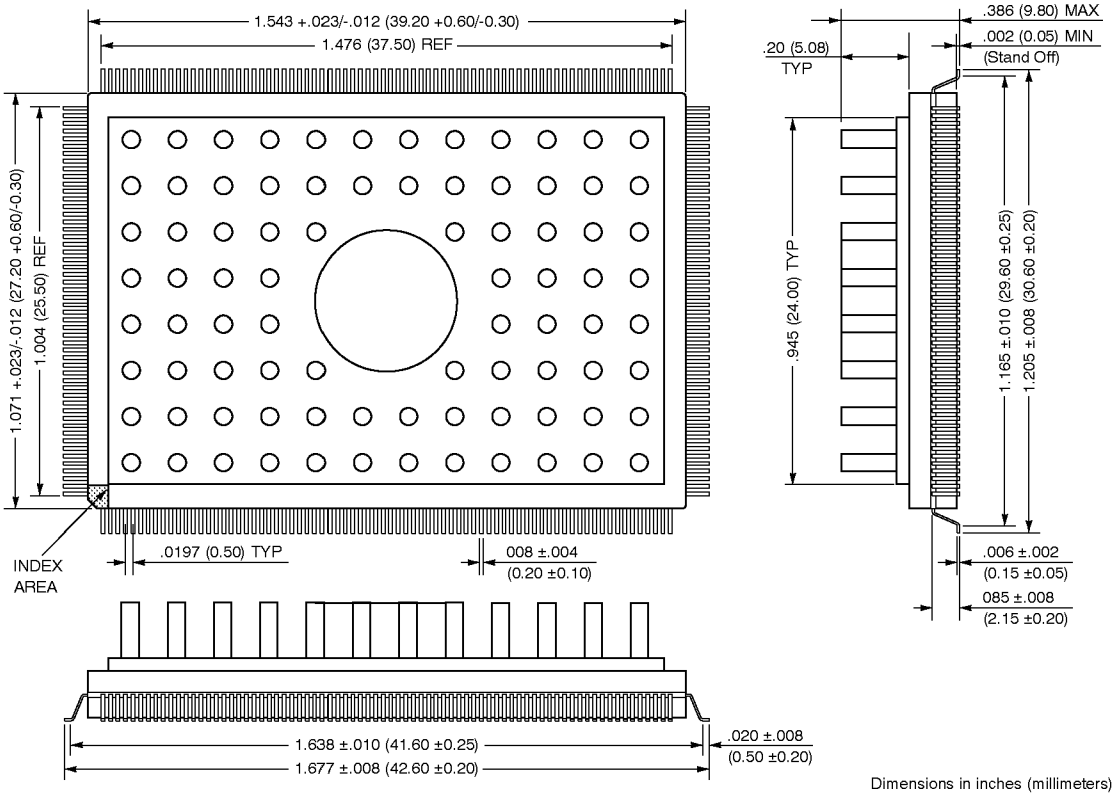


256-PIN FLAT PACKAGE(CQFP)



Ordering Info: MB86931–40ZF–G

256-LEAD FLAT PACKAGE (CQFP)



Dimensions in inches (millimeters)